UniDAQ2 Application Note Power Grid Monitoring

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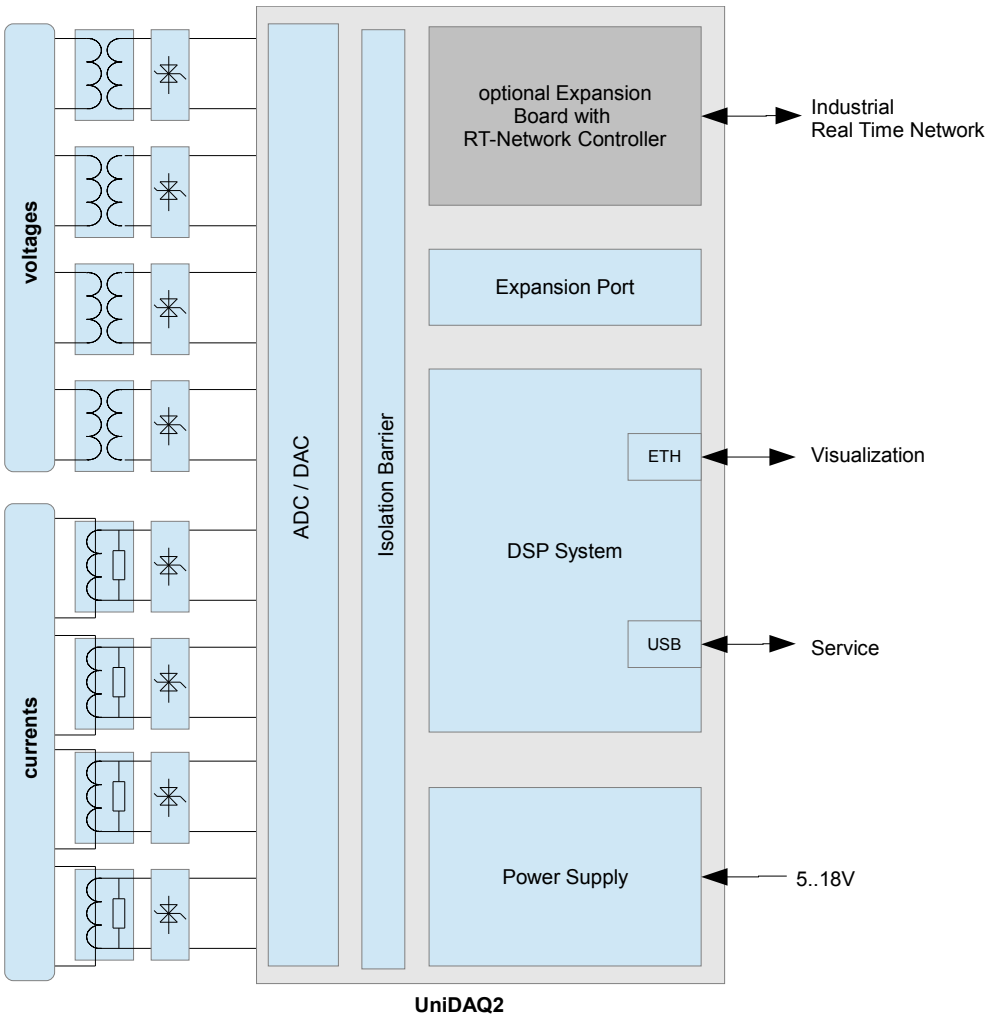
Background

The challenges of smart grids, renewable energy sources and vehicle electrification make monitoring an essential tool to sustain power grid quality and reliability. This paper discusses the UniDAQ2 data acquisition and processing system as a key component for such a monitoring system.

Dealing with high voltages and currents requires comprehensive safety mechanisms to protect users and equipment. The analog inputs of the UniDAQ2 provide a basic 350VAC isolation from the digital circuits and the power supply. Additional protective circuits are required to guarantee operational safety, especially in case of a component failure. We will not discuss these safety considerations as this is not only beyond the scope of this document, but admittedly also beyond our area of expertise.

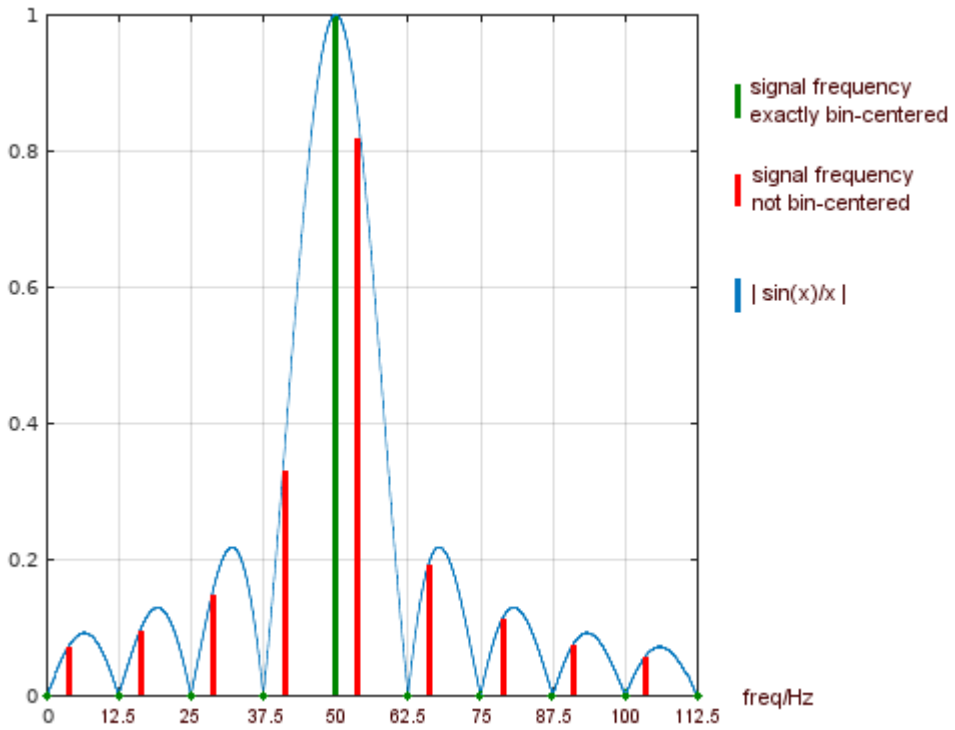
A 3-phase grid installation requires to monitor up to four voltages and four currents, occupying eight of the 16 analog inputs of the UniDAQ2. If differential sensors are used the resolution can be increased by 3dB, utilizing all 16 ADC channels and calculating the difference in the digital domain. UniDAQ2 samples all input channels simultaneously, accurately preserving the phase relations between the signals.



A key feature of a grid monitoring system is the spectral analysis of the voltages and currents to determine the harmonic content. This is done by fast fourier transformations (FFT). But an FFT may suffer from spectral leakage, making accurate measurements of closely spaced frequency components impossible.

Spectral Leakage

An FFT processes a finite number of input samples, corresponding to a rectangular window in the time domain. A time-domain window results in a convolution with the transform of this window in frequency domain. The transform of a rectangular window is the sinc function sin(x)/x. If a signal frequency is exactly bin-centered, this bin level exactly corresponds to the frequency component amplitude and the adjacent bins will be 0. If however the signal frequency deviates from the bin center frequency, this bin will show a lower amplitude value and the neighbouring bins will be nonzero, as defined by the sinc function. This is called spectral leakage.



Spectral leakage must be minimized to a level which does not mask any other important neighbouring frequency component. Windowing in the time domain may be used, but this technique requires large FFTs to resolve closely spaced low frequency components. A better approach is the use of coherent sampling.

In power-line monitoring we want to evaluate the harmonics of the grid frequency up to several kHz. Since harmonics are integer multiples of the fundamental frequency, these are automatically bin-centered if the fundamental grid frequency itself is bin-centered. Back to time domain, this requires the FFT to process an integer number of complete fundamental frequency cycles. Since the power grid frequency varies with load conditions, the sampling frequency must track the grid frequency to ensure the fundamental and all harmonics remain bin-centered.

Sampling Frequency Selection

The sampling frequency is chosen to acquire 256 samples per grid frequency period. For an FFT size of 256 or higher the FFT will always process an integer number of complete fundamental frequency cycles. 256 samples per grid cycle result in a sampling frequency of 12800 Hz for a 50Hz grid, 15360 Hz for a 60Hz grid, and allows to evaluate the spectrum up to the 127th harmonic.

Coherent Sampling - tracking the fundamental signal frequency

A PLL can be used to track the grid frequency and generate the sampling clock. The PLL needs to suppress signal noise sufficiently to avoid tracking errors, accomplished by low loop bandwidth at the expense of frequency agility. The PLL can be implemented in the analog or in the digital domain.

A zero-crossing detector is another popular procedure to measure the signal frequency. Accuracy also depends on good noise suppression by a narrow bandpass filter.

This application note discusses a different approach:

Once a spectrum is calculated, the exact fundamental signal frequency can be derived with high accuracy from the resulting leakage into the adjacent frequency bins. Since only three frequency bins are used for the calculation, the bandwidth is extremely small, providing excellent noise rejection. This computation is used to adjust a high resolution timer generating the sampling clock. The system will lock to the grid frequency after one measurement cycle.

Sampling Clock Generation

The TMS320C6747 DSP features two accompanying RISC processors, operating completely independent of the DSP core: the Programmable Real Time Unit Subsystem PRUSS. The PRU is clocked at 228MHz and can generate the sampling clock with 4.4ns resolution [1)].

50Hz grid: clock divider = 228MHz/12800Hz = 17812.5 -> 17812 or 17813

60Hz grid: clock divider = 228MHz/15360Hz = 14843.75 -> 14844

The error in a 50Hz grid, caused by the finite frequency resolution, is +/- 0.5/17812.5 = +/-28ppm, which is the same order of magnitude as the accuracy of a typical crystal oscillator timebase.

Taking this error into account the actual bin spacing of a 1024pt FFT is 12.49965 or 12.50004 Hz. A precise 50Hz signal will deviate by 0.0014Hz from the 4th bin center, causing -79dB leakage into the neighbour bins 3 and 5. The next harmonic (100Hz at bin 8) will get -91dB leakage. A 500Hz signal (the 10th harmonic) will deviate by 0.014Hz from the bin center, causing -59dB leakage into the adjacent frequency bins, and -71dB into the 9th and 11th harmonics. But since harmonics are much lower in amplitude the resolution is totally adequate for power grid monitoring: the errors caused by spectral leakage will be buried in the noise floor.

Other applications with higher sampling frequencies may require better frequency resolution than achievable by the PRU. This can be accomplished with an on-the-fly programmable oscillator like the Silicon Labs Si514, followed by a post-divider. This circuit can be mounted on a UniDAQ2 expansion board. The expansion port TRIGOUT signal is then used as the ADC sampling clock.

Algorithms

The Texas Instruments dsplib provides highly optimized FFT functions. A 1024pt, single-precision floating point, radix-2, decimation in time FFT completes in less than 21000 processor cycles (46us). The dsplib functions make use of software pipelining optimizations which disable interrupts on the DSP core during the function runtime. Although this would still allow to sample the ADC channels at up to 20kHz using interrupt processing, it is much more efficient to use background DMA transfers. The optimum setup uses one of the C6747 PRU processors to service the McASP serial port, to which the ADCs are connected. The PRU reads all 16 input channels, stores them sorted in ascending order in the PRU data RAM and also monitors each channel for clipping. With each sampling period the PRU generates an event signal which is used to trigger the DMA to move the data from the PRU buffer to the destination buffers. The DMA parameters are configured to sort the data according to the channel number into ping-pong buffers.

Following the DMA complete event the data is converted to floating point format and normalized in place. The ping- and pong buffers are flipped and the readily prepared buffer is processed by the FFT function. The FFT results are finally bit-reversed to normal frequency order.

To track the grid frequency a frequency estimation algorithm by Eric Jacobsen and Peter Kootsookos is used [2)]. This algorithm calculates the deviation from a frequency bin based on the spectral leakage into the adjacent bins and provides accurate results even in the presence of high noise levels. The result is used to adjust the sampling frequency generator implemented in the other PRU processor.

Processing Time

Calculating eight 1024pt complex FFTs and bit-reversing the output to normal order takes 1.034ms on the TMS320C6747 processor. This time includes the fixed to floating point conversion and normalization of the input data. Estimating the instantaneous fundamental frequency and the sampling frequency adaptation takes only 8us. The available time is 1024 sampling periods = 80ms. The CPU utilization is just a mere 1.3%, leaving ample time for sensor equalization, comprehensive data analysis, communications and housekeeping tasks.

System Integration

The computation results need to be communicated to a process control system. The UniDAQ2 Expansion Port provides a high speed SPI port and a parallel bus interface to connect an industrial real-time network controller for EtherCAT, Sercos III, ProfiNet, CAN, etc.

The standard Ethernet Port of the UniDAQ2 may be used for less real-time critical transfers, data visualization and parameterization. Likewise the eight DAC outputs can be used as analog control outputs.

The entire system can be rack-mounted in a single 19" 3U 4HP slot or rail-mounted.

Example Program

The UniDAQ2 support software contains the fft_coherent demo project which demonstrates the techniques and algorithms described in this application note.

Conclusion

UniDAQ2 is a convenient platform to implement power grid monitoring, with voltage and current transformers and protective circuits being the only external components required. The versatile expansion port facilitates multiple system integration options.

References

1. D.SignT UniDAQ2 Application Note PRU (an_unidaq2_pru.pdf)
2. Eric Jacobsen and Peter Kootsookos: Fast, Accurate Frequency Estimators, IEEE Signal Processing Magazine, June 2007

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