LXD30K0 Low latency wideband FMC module

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1 General Description

Demanding markets like the military, aerospace/space, telecommunications and science are always looking for ways to push the boundaries of what is possible. At the front end this requires very fast analog to digital and digital to analog converters and in some applications, these need to offer the lowest possible latency. The European based Teledyne E2V and Logic-X recognize this challenge and have joined to bring to market a High speed, high bandwidth low latency ADC/DAC Commercial of the shelve product. Teledyne E2V semiconductors has a unique offering of ADC and DAC devices specifically designed for this purpose and Logic-X is the company of choice for integrating these devices into a commercial of the shelve product.

With an analog input stage that has a very wide input bandwidth from 0.5MHz up-to 6000 GHz and the low latency 5.4Gsps ADC from E2V (EV12AS350A) the LXD30K0 delivers unmatched performance with regards to SFDR, close in phase noise and latency on its analog input channel. Likewise the analog output offers an even lower latency DAC device from E2V (EV12DS460) and the same width for its output bandwidth. Both the ADC and DAC offer 12-bits resolution further contributing to achieve best in class signal to noise ratios.

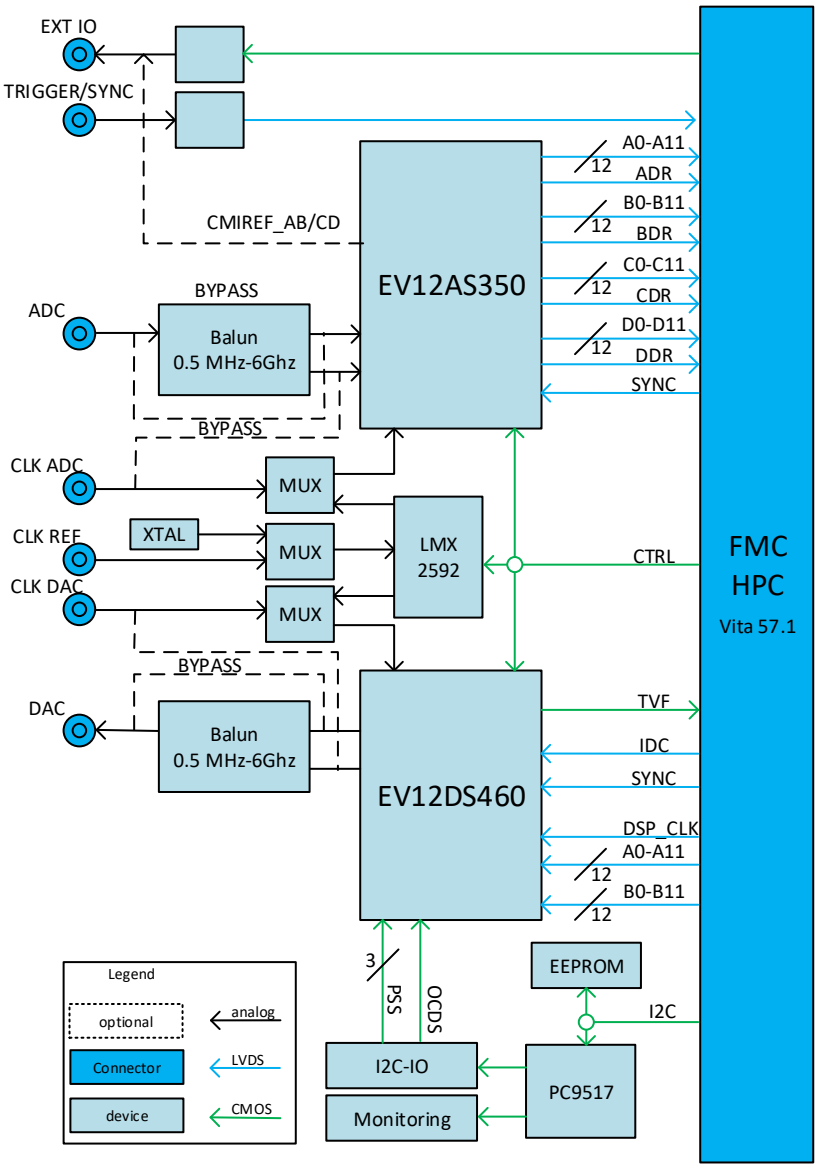

Figure 1: LXD30K0 block diagram

Systems that will benefit greatly from this product are amongst others, Electronic Warfare systems, Radar waveform generators and receivers, Advanced digital RD memory (RDFM) systems, Medical systems, Telecommunication systems and many more. Being a high pin count FMC allows the LXD30K0 to be used both as an upgrade for existing processing systems as well as new processing systems.

Due to the limited amount of LVDS pins available om the FMC high pin-count connector it is not possible to make full use of the DAC chipset capabilities. A total instantaneous bandwidth of 1.35 GHz is provided which is half of the device's capabilities. However, it will still be possible to place signals into the second, third and even 4th Nyquist zone thanks to the advanced and patented operating modes of the E2V chipset.

2 Mechanical design

The board design is mechanically compliant to the Vita 57.1 (FMC) specification.

2.1 Cooling

The board is delivered with a heatsink that is violating the maximum component height of 4.7mm. Most FMC carrier products on the market today won't have a conflict. Please contact Logic-X for custom heatsink and conduction cooling solutions.

2.2 Front panel design

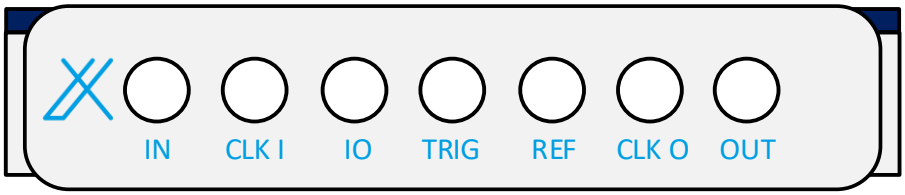

Figure 2: LXD30K0 front panel design

Table 1: Front panel signal description

Front panel name	Refdes	Connected to
IN	J9	Analog input (single ended - default) Positive Analog input (differential - option)
CLKI	J8	External ADC clock input (default) Negative analog input (option)
IO	J7	3V3 LVCMOS IO (default) ADC Common mode reference output CMIREF (option)
TRIG	J6	External trigger input
REF	J4	External reference clock input
CLKO	J3	External DAC clock input (default) Negative analog output (option)
OUT	J2	Analog output (single ended - default) Positive analog output (differential – option)

3 FMC connector

The LXD30K0 is an FMC card that targets a high pin count connector. As such it has the option to connect up-to 84 LVDS signals to the carrier card plus some additional CMOS control signals. Both the ADC and DAC device that are targeted for this design have four 12-bits wide data busses and additional control signals to communicate with the outside world. This means that there are not enough connections available on the FMC HPC connector to achieve full functionality of the two devices. The DAC device can position the output signal into higher order Nyquist zones, and you will not need to drive the full bandwidth at once. Therefore, the DAC connects only half the data signals lowering the instantaneous bandwidth of the output to 1.35GHz. The ADC has an instantaneous bandwidth of 2.7 GHz.
Furthermore, there are some FMC carrier boards around that offer not all the FMC connections. These products can still benefit from a low latency high sample rate ADC/DAC product. By smartly selecting the ADC and DAC data bus connections on the LXD30K0 it is possible to also use the ADC with only half the data signals. In this setup both ADC and DAC have a 1.35 GHz instantaneous bandwidth.

3.1 LA, HA and HB connections

The following table shows the signal connections on the FMC connector
A signal ending with _p or _n indicates the negative and positive signals part of a differential pair. All differential pairs are LVDS signals. The remaining single ended signals are LVCMOS with a voltage rating equal to the power supplied on VADJ.

AV57	Con. Pin	LXD30K00	AV57	Con. Pin	LXD30K00
CLK0_M2C_N	H5	ext_tri_to_fpga_n	DP8_M2C_P	B8	n.c.
CLK0_M2C_P	H4	ext_tri_to_fpga_p	DP9_C2M_N	B25	n.c.
CLK1_M2C_N	G3	sync_from_fpga_n	DP9_C2M_P	B24	n.c.
CLK1_M2C_P	G2	sync_from_fpga_p	DP9_M2C_N	B5	n.c.
CLK2_BIDIR_N	K5	n.c.	DP9_M2C_P	B4	n.c.
CLK2_BIDIR_P	K4	n.c.	GBTCLK0_M2C_N	D5	n.c.
CLK3_BIDIR_N	J3	I2C_INT_L	GBTCLK0_M2C_P	D4	n.c.
CLK3_BIDIR_P	J2	TRIGGER_OUT	GBTCLK1_M2C_N	B21	n.c.
DP0_C2M_N	C3	n.c.	GBTCLK1_M2C_P	B20	n.c.
DP0_C2M_P	C2	n.c.	HA00_N_CC	F5	dac_dataa_n<6>
DP0_M2C_N	C7	n.c.	HA00_P_CC	F4	dac_dataa_p<6>
DP0_M2C_P	C6	n.c.	HA01_N_CC	E3	dac_datab_n<1>
DP1_C2M_N	A23	n.c.	HA01_P_CC	E2	dac_datab_p<1>
DP1_C2M_P	A22	n.c.	HA02_N	K8	dac_dataa_n<7>
DP1_M2C_N	A3	n.c.	HA02_P	K7	dac_dataa_p<7>
DP1_M2C_P	A2	n.c.	HA03_N	J7	dac_dataa_n<10>
DP2_C2M_N	A27	n.c.	HA03_P	J6	dac_dataa_p<10>
DP2_C2M_P	A26	n.c.	HA04_N	F8	dac_dataa_n<9>
DP2_M2C_N	A7	n.c.	HA04_P	F7	dac_dataa_p<9>
DP2_M2C_P	A6	n.c.	HA05_N	E7	dac_dataa_n<8>
DP3_C2M_N	A31	n.c.	HA05_P	E6	dac_dataa_p<8>
DP3_C2M_P	A30	n.c.	HA06_N	K11	dac_datab_n<0>
DP3_M2C_N	A11	n.c.	HA06_P	K10	dac_datab_p<0>
DP3_M2C_P	A10	n.c.	HA07_N	J10	dac_dataa_n<11>
DP4_C2M_N	A35	n.c.	HA07_P	J9	dac_dataa_p<11>
DP4_C2M_P	A34	n.c.	HA08_N	F11	dac_datab_n<2>
DP4_M2C_N	A15	n.c.	HA08_P	F10	dac_datab_p<2>
DP4_M2C_P	A14	n.c.	HA09_N	E10	dac_datab_n<3>
DP5_C2M_N	A39	n.c.	HA09_P	E9	dac_datab_p<3>
DP5_C2M_P	A38	n.c.	HA10_N	K14	dac_datab_n<7>
DP5_M2C_N	A19	n.c.	HA10_P	K13	dac_datab_p<7>
DP5_M2C_P	A18	n.c.	HA11_N	J13	dac_datab_n<9>
DP6_C2M_N	B37	n.c.	HA11_P	J12	dac_datab_p<9>
DP6_C2M_P	B36	n.c.	HA12_N	F14	dac_datab_n<6>
DP6_M2C_N	B17	n.c.	HA12_P	F13	dac_datab_p<6>
DP6_M2C_P	B16	n.c.	HA13_N	E13	dac_datab_n<4>
DP7_C2M_N	B33	n.c.	HA13_P	E12	dac_datab_p<4>
DP7_C2M_P	B32	n.c.	HA14_N	J16	dac_datab_n<8>
DP7_M2C_N	B13	n.c.	HA14_P	J15	dac_datab_p<8>
DP7_M2C_P	B12	n.c.	HA15_N	F17	dac_datab_n<11>
DP8_C2M_N	B29	n.c.	HA15_P	F16	dac_datab_p<11>
DP8_C2M_P	B28	n.c.	HA16_N	E16	dac_datab_n<5>
DP8_M2C_N	B9	n.c.	HA16_P	E15	dac_datab_p<5>

HA17_N_CC	K17	dac_dsp_clk_n	HB15_N	J34	datad_n<2>
HA17_P_CC	K16	dac_dsp_clk_p	HB15_P	J33	datad_p<2>
HA18_N	J19	dac_datab_n<10>	HB16_N	F35	datad_n<6>
HA18_P	J18	dac_datab_p<10>	HB16_P	F34	datad_p<6>
HA19_N	F20	dac_idc_n	HB17_N_CC	K38	datad_n<9>
HA19_P	F19	dac_idc_p	HB17_P_CC	K37	datad_p<9>
HA20_N	E19	datac_n<1>	HB18_N	J37	datad_n<8>
HA20_P	E18	datac_p<1>	HB18_P	J36	datad_p<8>
HA21_N	K20	datac_n<3>	HB19_N	E34	datad_n<3>
HA21_P	K19	datac_p<3>	HB19_P	E33	datad_p<3>
HA22_N	J22	datac_n<10>	HB20_N	F38	datad_n<11>
HA22_P	J21	datac_p<10>	HB20_P	F37	datad_p<11>
HA23_N	K23	datac_n<11>	HB21_N	E37	datad_n<10>
HA23_P	K22	datac_p<11>	HB21_P	E36	datad_p<10>
HB00_N_CC	K26	datareadyd_n	LA00_N_CC	G7	datareadya_n
HB00_P_CC	K25	datareadyd_p	LA00_P_CC	G6	datareadya_p
HB01_N	J25	datac_n<9>	LA01_N_CC	D9	datareadyb_n
HB01_P	J24	datac_p<9>	LA01_P_CC	D8	datareadyb_p
HB02_N	F23	datac_n<7>	LA02_N	H8	dataa_n<0>
HB02_P	F22	datac_p<7>	LA02_P	H7	dataa_p<0>
HB03_N	E22	datac_n<5>	LA03_N	G10	dataa_n<6>
HB03_P	E21	datac_p<5>	LA03_P	G9	dataa_p<6>
HB04_N	F26	datac_n<6>	LA04_N	H11	dataa_n<1>
HB04_P	F25	datac_p<6>	LA04_P	H10	dataa_p<1>
HB05_N	E25	datac_n<8>	LA05_N	D12	dataa_n<2>
HB05_P	E24	datac_p<8>	LA05_P	D11	dataa_p<2>
HB06_N_CC	K29	datareadyc_n	LA06_N	C11	dataa_n<4>
HB06_P_CC	K28	datareadyc_p	LA06_P	C10	dataa_p<4>
HB07_N	J28	datac_n<2>	LA07_N	H14	dataa_n<7>
HB07_P	J27	datac_p<2>	LA07_P	H13	dataa_p<7>
HB08_N	F29	datac_n<0>	LA08_N	G13	dataa_n<3>
HB08_P	F28	datac_p<0>	LA08_P	G12	dataa_p<3>
HB09_N	E28	datac_n<4>	LA09_N	D15	dataa_n<5>
HB09_P	E27	datac_p<4>	LA09_P	D14	dataa_p<5>
HB10_N	K32	datad_n<0>	LA10_N	C15	dataa_n<8>
HB10_P	K31	datad_p<0>	LA10_P	C14	dataa_p<8>
HB11_N	J31	datad_n<5>	LA11_N	H17	dataa_n<10>
HB11_P	J30	datad_p<5>	LA11_P	H16	dataa_p<10>
HB12_N	F32	datad_n<1>	LA12_N	G16	dataa_n<9>
HB12_P	F31	datad_p<1>	LA12_P	G15	dataa_p<9>
HB13_N	E31	datad_n<7>	LA13_N	D18	dataa_n<11>
HB13_P	E30	datad_p<7>	LA13_P	D17	dataa_p<11>
HB14_N	K35	datad_n<4>	LA14_N	C19	datab_n<4>
HB14_P	K34	datad_p<4>	LA14_P	C18	datab_p<4>

LA15_N	H20	datab_n<5>	LA25_N	G28	datab_n<2>
LA15_P	H19	datab_p<5>	LA25_P	G27	datab_p<2>
LA16_N	G19	datab_n<7>	LA26_N	D27	TVF
LA16_P	G18	datab_p<7>	LA26_P	D26	SPI_CLK
LA17_N_CC	D21	datab_n<11>	LA27_N	C27	SPI_MISO
LA17_P_CC	D20	datab_p<11>	LA27_P	C26	SPI_MOSI
LA18_N_CC	C23	datab_n<10>	LA28_N	H32	dac_dataa_n<0>
LA18_P_CC	C22	datab_p<10>	LA28_P	H31	dac_dataa_p<0>
LA19_N	H23	datab_n<3>	LA29_N	G31	dac_dataa_n<2>
LA19_P	H22	datab_p<3>	LA29_P	G30	dac_dataa_p<2>
LA20_N	G22	datab_n<6>	LA30_N	H35	dac_dataa_n<4>
LA20_P	G21	datab_p<6>	LA30_P	H34	dac_dataa_p<4>
LA21_N	H26	datab_n<1>	LA31_N	G34	dac_dataa_n<5>
LA21_P	H25	datab_p<1>	LA31_P	G33	dac_dataa_p<5>
LA22_N	G25	datab_n<8>	LA32_N	H38	dac_dataa_n<1>
LA22_P	G24	datab_p<8>	LA32_P	H37	dac_dataa_p<1>
LA23_N	D24	datab_n<9>	LA33_N	G37	dac_dataa_n<3>
LA23_P	D23	datab_p<9>	LA33_P	G36	dac_dataa_p<3>
LA24_N	H29	datab_n<0>	SCL	C30	SCL
LA24_P	H28	datab_p<0>	SDA	C31	SDA

3.2 Utility connections

The following table shows how the utility connections signals are used on the LXD30K0.

Table 2: FMC utility signal usage

Signal name	Connected to
PRSNT_M2C	Tied to GND
PG_C2M	Used to start local sequencing
TCK	Not used
TDI	Connected to TDO
TDO	Connected to TDI
SCL	See chapter on I2C
SDA	See chapter on I2C
TMS	Not used
TRST_L	Not used
GA0	See chapter on I2C
GA1	See chapter on I2C
RES0	Not used
PG_M2C	Asserted directly when the carrier asserts PG_C2M

3.3 Gigabit transceiver connections

The LXD30K0 does not connect any of the Gigabit transceiver connections or reference clocks.

3.4 I/O Standard Support

Most of the signal connections to the FMC connector on the LXD30K0 are differential LVDS type of signals. The CMOS control signals are passed through level translators that are powered by VADJ on one the FMC side. This ensures proper operation with VADJ voltages between 1.2 and 3.3V. The VREF signal is not used and not connected

3.5 VIO_B_M2C Support

The LXD30K0 connects VIO_B_M2C directly to VADJ.

3.6 VREF Support

The LXD30K0 leaves VREF_A_M2C and VREF_B_M2C unconnected.

4 Analog input and output

At the analog input and output the LXD30K0 uses a balun coupling for single ended to differential conversion. In order to make maximum use of the ADC and DAC capabilities the balun (BAL-0006SMG) from Marki microwave is used. This balun offers a very wide bandwidth from 500Khz up to 6GHz.Typically the phase matching is within 3 degrees over the entire bandwidth. In addition, it has a very flat insertion loss. The nominal insertion loss is 6dB.
The Analog input and output are AC coupled at the connector to limit DC biasing of the transformer. For specific applications it is possible to provide a differential DC coupled input and output. However, this requires careful implementation of the receiving and transmitting analog front end. Please contact Logic-X for more information about the DC coupled option

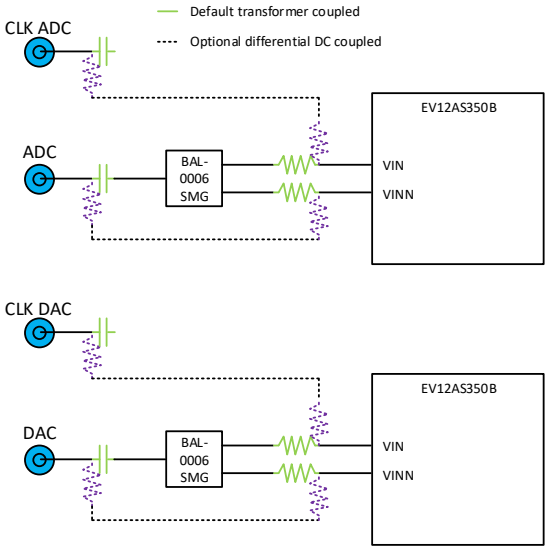

Figure 3: Analog input and output schematic

4.1 Input frequency response

Great care has been taken at the design of the LXD30K0 to provide flat insertion loss across a wide bandwidth. The Balun adds an almost constant insertion loss of 6dBm across the range and the PCB losses are minimal by design. The Following image shows the bandwidth of the analog input.

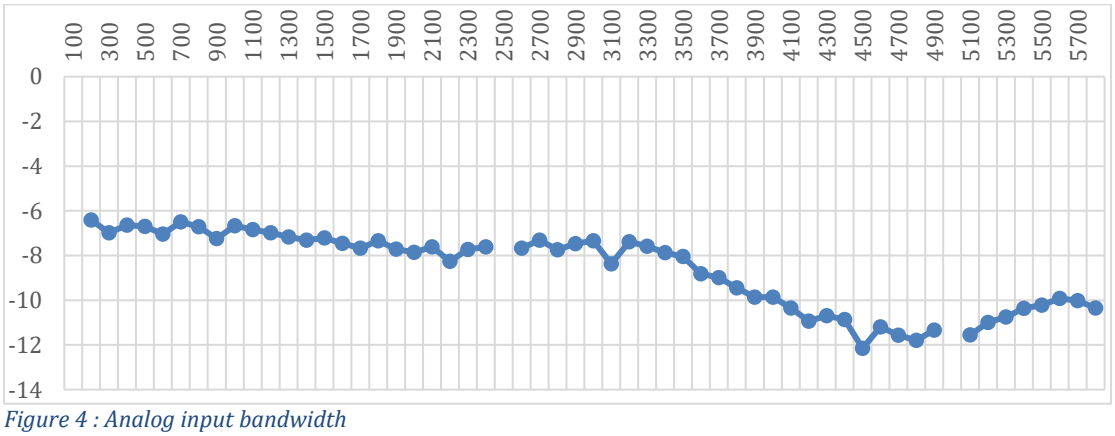

Figure 4 : Analog input bandwidth

4.2 Output frequency response

The DAC device has different behavior with regards to its output power depending on the mode of operation and the output frequency. The following Graph shows the output power of the DAC in the different modes.

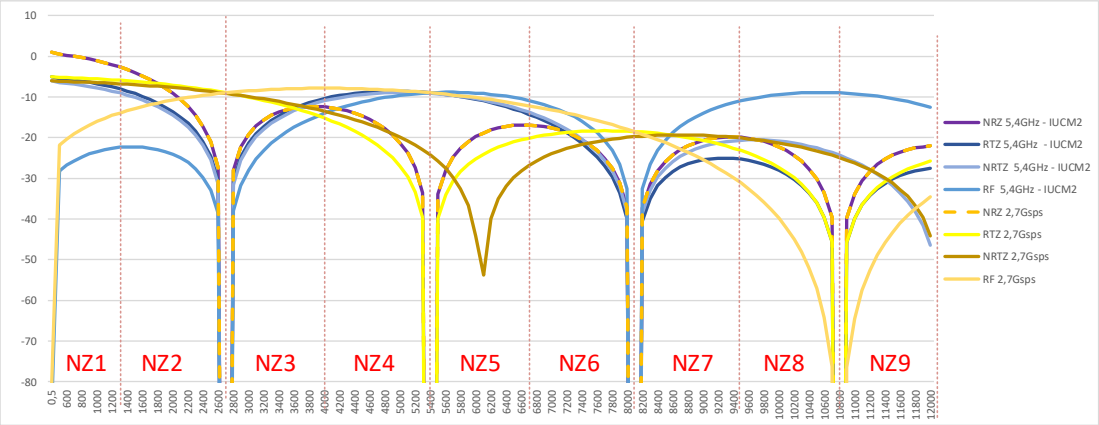

Figure 5: EV12DS460 output power

This graph clearly shows that it depends on the frequency band of interest in which mode the DAC should be operated. For operation below 8GHz there is no use for running the DAC at more than 2.7 Gsps. The next table shows for each Nyquist band the advised operating mode of the DAC and the typical attenuation compared to the full-scale DAC 1dBm output

Table 3:Advised operating mode of EV12DS460 and output power per Frequency band

Frequency band	Nyquist zone @ 2,7Gsps	EV12DS460 operating mode	Output power Start /end (dBm)	After Balun Start /end (dBm)	At the connector Start /end (dBm)
DC - 1.35 GHz	1	NRZ, IUCM1, 2.7 Gsps	1/-3	-5/-8	-5.5/-8.5
DC - 1.35 GHz	1	RTZ, IUCM1, 2.7 Gsps	-5/-6	-10/-11	-10.5/-11.5
1.35 - 2.7 GHz	2	RTZ, IUCM1, 2.7 Gsps	-6/-9	-11/-14	-11.5/-14.5
2.7 - 4.05	3	RF, IUCM1, 2.7 Gsps	-9/-8	-15/-14	-15.5/-14.5
4.05 - 5.4	4	RF, IUCM1, 2.7 Gsps	-8/-9	-14/-15	-14.5/-15.5

At the output the signal will receive a fixed attenuation of 6dB due to the insertion loss of the Balun that is used. The following image shows the bandwidth of the analog output.

Figure 6: Analog output bandwidth

4.3 DC coupled input and output

As a build option the balun of the analog input an analog output can be bypassed to provide a DC coupled interface to and from the ADC/DAC. The ADC driving circuitry will need to use the CMIREF_AB or CMIREF_CD signal to provide the right common mode voltage. This means repurposing the trigger output to common mode reference output. Contact Logic-X if you are interested in this build option.

5 I2C Interface

The FMC identification EEPROM is connected directly to the FMC I2C signals and is active with only the 3V3_AUX.
The other devices on the chain are the voltage monitoring devices and an I2C IO expander (PCAL6524HEAZ). The IO expander has 24 bits that can individually be set as input or output. Also, each bit can be configured to latch a state change and generate an interrupt if required. The IO expander signals are used in order to drive the different static control signals and to read back status signals. The Table 4 shows what signals connect to the IO expander.
The image below depicts the I2C schematic and the devices addresses.

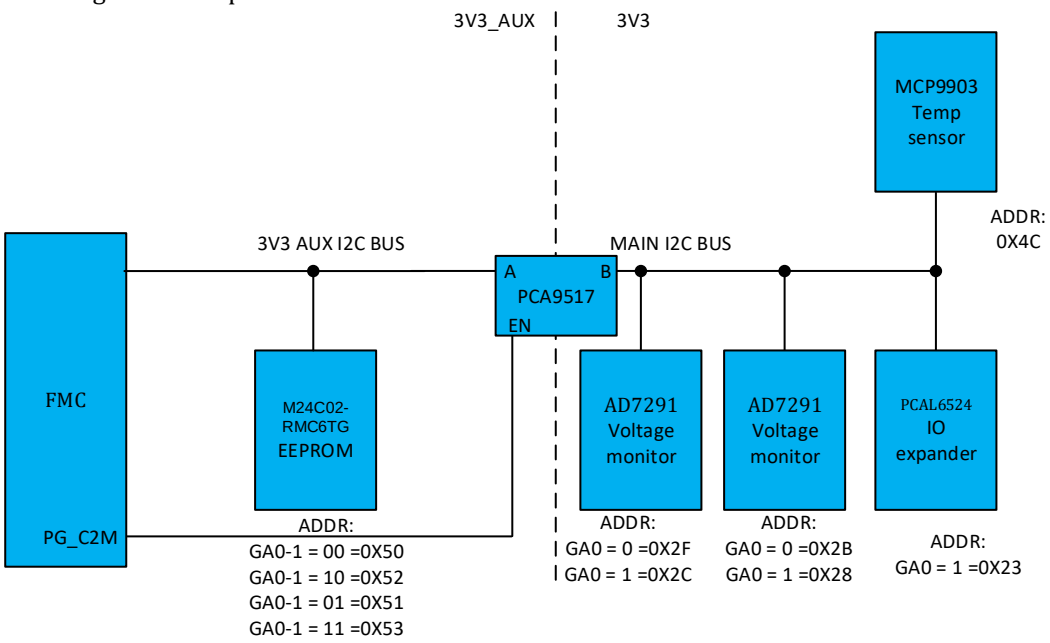

Figure 7:I2C schematic

Table 4: IO expander signal connections

IO pin	Direction	Signal name	Default	Connected to	Function
P0_0	O	PSS0	0	Connects to EV12DS460	Select clock/data phase
P0_1	O	PSS1	0	Connects to EV12DS460	Select clock/data phase
P0_2	O	PSS2	0	Connects to EV12DS460	Select clock/data phase
P0_3	O	OCDS	0	Connects to EV12DS460	Output clock division select
P0_4	O	CLK_ADC_MUX	0	Connects to RF switch	Select external (high) Clock or local (low) clock for the EV12AS350 ADC
P0_5	O	CLK_DAC_MUX	0	Connects to RF switch	Select external (high) Clock or local (low) clock for the EV12DS460 DAC
P0_6	O	CLK_REF_MUX	0	Connects to RF switch	Select external reference (low) or local reference (high) clock for the LMX2592
P0_7	O	PLL_EN	0	LMX2592	Drive the CE pin high to power on the LMX2592
P1_0	O	VCC_REF_EN	0	Connects to the Reference clock power supply.	Drive high to enable the reference clock power supply. Disable the reference clock when not used to avoid interference from this clock.
P1_1	O	VCC_PLL_EN	0	Connects to the LMX2592 power supply.	Drive high to enable the PLL power supply. Disable the clock PLL when not used to avoid interference from this clock.
P1_2	O	VCC_DAC_EN	0	Connects to the EV12DS460 power supplies	Drive high to enable the DAC power supply. This allows the DAC to be powered down separately from the ADC if required.
P1_3	O	VCC_ADC_EN	0	Connects to the EV12AS350 power supplies	Drive high to enable the ADC power supply. This allows the ADC to be powered down separately from the ADC if required.
P1_4	O	VCC_SWITCH_EN	0	LTM8074 switching power supplies	Allows sequencing of power rails and independent control over the regulators
P1_5	I	TRIG_IO_DIR			Select the direction of the Trigger IO signal towards the TRIG IO SSMC. Drive high to make this an output.
P1_6	I	SYNC_SEL0			Select between external trigger and FPGA SYNC for ADC SYNC
P1_7	I	SYNC_SEL1			Select between external trigger and FPGA SYNC for DAC SYNC
P2_0	I	PG_SWITCH		LTM8074 switching power supplies	If asserted high both switching regulators are powers are OK
P2_1	I	PG_PLL		LMX2592	PLL power is good
P2_2	I	PG_REF		Reference Clock XO	REF clock power is good
P2_3	O	PLL_CS_N	0	LMX2592	SPI interface not chip select for configuring the PLL through SPI
P2_4	O	ADC_CS_N	0	AV12AS350	SPI interface not chip select for configuring the ADC through SPI
P2_5	O	DAC_CS_N	0	AV12DS460	3WSI interface chip select for configuring the DAC through SPI
P2_6	O	DAC_RESET_N	0	AV12DS460	Drive the DAC reset low to initialize its 3WSI to default values
P2_7	O	ADC_RESET_N	0	AV12AS350	Drive the ADC reset low to initialize its 3WSI to default values

6 SPI Interface

A direct SPI connection is available on the FMC LA connector that connects to the EV12DS560, EV12AS350 and the LMX2592. They all share the MISO, MOSI and CLK signal, but they have independent CS signals that are driven by the IO expander. The EV12DS460 has no output data and its registers can only be written.

EV12DS460 maximum SPI clock frequency is 1 MHz.
EV12AS350 maximum SPI clock frequency is 50 MHz.
LMX2592 maximum SPI clock frequency is 50 MHz.

It is required to set the CSN signals of the two devices that are not targeted to a high value and the CSN of the device that is targeted to a low value.

Typically to access one of the three SPI devices the following sequence should be followed:

- Assume that the IO expander ports are correctly configured and all three CSN signals are high. Perform a SPI access to the ADC
- Read the IO expander P2 output register (offset address 0x6)
- Set bit 4 in the register value low
- Write back the new value to IO expander P2 output register
    - The ADC_CSN is now low
- Perform the SPI write or read using a SPI master in the FPGA
- Reuse the P2 register value and set bit 4 high
- Write the value to the IO expander P2 output register
    - The ADC_CSN is now high

7 External trigger and SYNC

It is possible to connect an external trigger to the EXT_TRIG SSMC connector. This input supports LVCMOS signalling by default but can support LVPECL or custom threshold levels. Contact Logic-X for non-default trigger threshold levels.
The external trigger is routed directly to the FMC connector and to a 2x2 Cross point switch. The cross-point switch also receives an LVDS signal from the FMC connector. The two outputs go to the SYNC inputs on the EV12DS460 and EV12AS350 devices. In this setup it is possible to support multi board synchronisation either from the FPGA or directly from the SSMC connector. Using the external trigger to FPGA and SYNC from FPGA it is possible to delay the SYNC signal using the IDELAY and ODELAY elements in the FPGA.

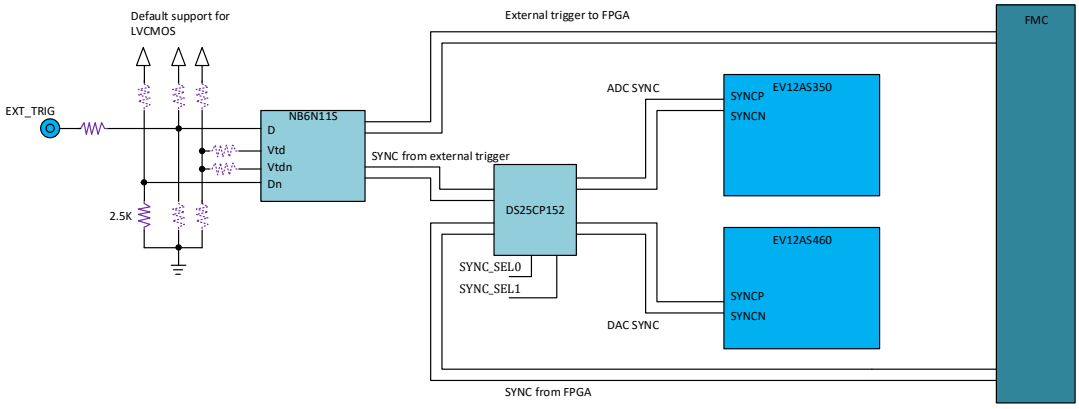

Figure 8: Input trigger schematic

8 Clock tree

Providing a very clean and stable clock is important for ADC and DAC devices. Therefore, special care is taken on the LXD30K0 to generate a very clean low jitter and low phase noise clock that is distributed to the ADC and DAC. The next image shows the LXD30K0 clock tree architecture.

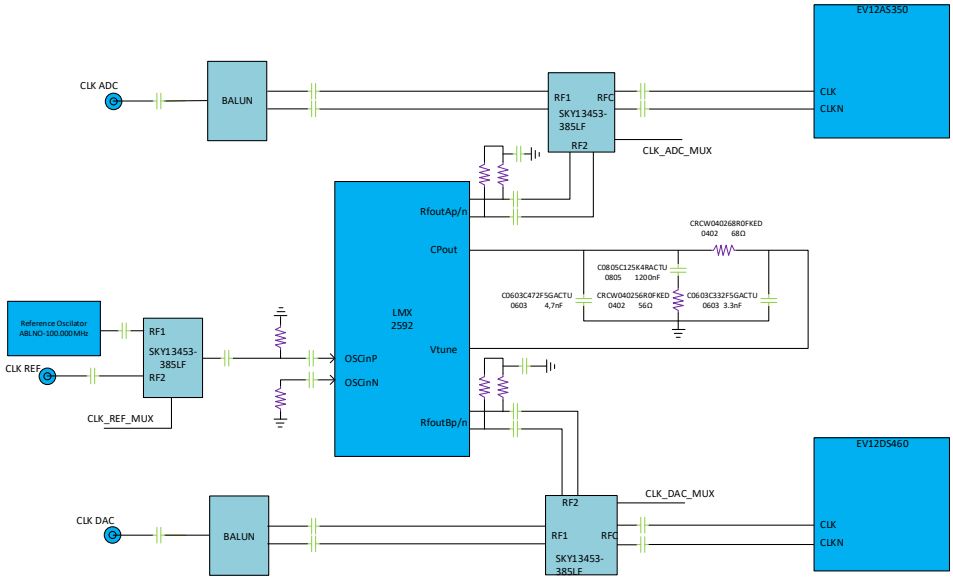

Figure 9: LXD30K0 clock tree architecture

8.1 Local clock generator

For the local clock a the LMX2592 device is used. This is a low-noise, wideband RF PLL with integrated VCO that supports a frequency range from 20 MHz to 9.8 GHz. The device supports both fractional-N and integer-N modes, with a 32-bit fractional divider allowing fine frequency selection. Integrated noise of 49 fs for 6-GHz output makes it an ideal low-noise clock source for the LXD30K0.

8.1.1 Local reference clock

For maximum stability a low phase noise reference oscillator from Abracon is used (ABLNO-100.000MHz). This oscillator has a phase noise performance that outperforms the LMX2592.

8.1.2 External reference clock

A wide band RF switch (SKY13453-385LF) with low insertion loss is used to select between the local reference oscillator and a user provided reference clock. The reference clock can be provided on the SSMC input connector.
The input reference clock can have a frequency between 5 MHz and 1400 MHz and should have a power between -3 dBm and 10dBm

8.1.3 PLL loop filter design

The default loop filter for the LMX2592 on the LXD30K0 is optimized for a phase detector frequency of 100MHz and a loop filter bandwidth of 141KHz and a phase margin of 48 degrees. This gives an estimated jitter of ~56fs at 5400MHz output clock frequency.

8.2 External clock

Both the ADC and DAC device receive their external clock from an SSMC connector. The received single ended clock signal is made differential using a balun from mini circuits (TCM1-83X+). This balun has an excellent wide range to support all the clock frequencies from 800 MHz up to 8000 MHz.
A double configuration of the wide band RF switch (SKY13453-385LF) is used to select between the external clock or the local clock.

9 External IO

By default there will be an external input/output available on the FMC front panel SSMC connector. This trigger is driven directly from the FMC CLK3_BIDIR_P pin through a level translating IO buffer (SN74AVC1T45YZPR). The signal level is 3V3 LVTTL. Driving bit P1-5 on the IO expander high makes the signal an output and driving it low makes it an output. By default the signal is configured as input and as such it is driving towards the FPGA. The FPGA designer should take care to only drive CLK3_BIDIR_P only after the P1-5 is set to high.

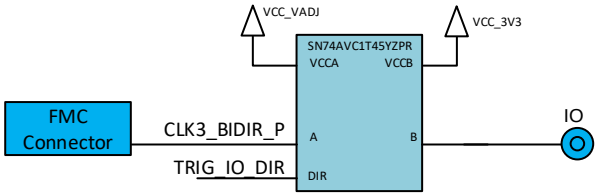

Figure 10: External IO

Another build option allows the ADC's common mode reference output CMIREF_AB or CMIREF_CD to be routed to this SSMC connector instead of the trigger output. This option combined with the ADC input balun bypass allows a differential DC coupled input to the ADC. The Common mode reference voltage is required for the analog circuitry driving the differential input signals.

10 Power Consumption

An FMC board receives several voltages from the FMC connector. These are 12V, 3V3, VADJ and 3V3_AUX. The LXD30K0 uses all these supplies. The following table shows the typical power consumption and current draw of the LXD30K0 on the different voltage rails. The total power consumption is typically around 14 Watts.

Table 5: LXD30K0 power consumption

Voltage Rail	Typical Current (A)	Typical Power (W)
VADJ	0.01	0,018 @ 1.8V
3P3V	0.67	2.2
12P0V	0.95	11.4
3P3VAUX (Operating) 3P3VAUX (Standby)	0.010 0.000001	0.033 0.0000033

11 Health monitoring

The LXD30K0 uses two AD7291 '8-channel I²C 12-bit SAR ADCs with temperature monitor' devices for monitoring power supply voltages. The device can be programmed and read through the I²C bus at the address defined in chapter 0. For monitoring the temperature of the ADC and DAC device the MCP9903T-AE/9Q is used.

11.1 Monitor 1

The first device, is configured to monitor the voltages shown in the table below. To convert the ADC reading to voltage multiply the ADC value by the scaling factor listed in the table.

Parameter:	Voltage	Formula
Channel 0	GND	
Channel 1	GND	
Channel 2	VCC_12V	Measured value*6*(2.5/4096) V
Channel 3	VCC_3V3	Measured value*2*(2.5/4096) V
Channel 4	VCC_3V2_D	Measured value*2*(2.5/4096) V
Channel 5	VCC_2V0	Measured value*1*(2.5/4096) V
Channel 6	VCC_3V3_CLK	Measured value*2*(2.5/4096) V
Channel 7	VCC_5V5	Measured value*3*(2.5/4096) V
Temperature	(internally generated)	AD7921 ADC TEMP * .0625 Degrees C

Table 6: first AD7291 Voltage Parameters

11.2 Monitor 2

The second device is configured to monitor the voltages are shown in the table below. To convert the ADC reading to a voltage or temperature multiply the ADC value by the scaling factor listed in the table.

Parameter:	Voltage	Formula
Channel 0	GND	
Channel 1	GND	
Channel 2	VCC_3V8	Measured value*2*(2.5/4096) V
Channel 3	VCC_5V_A	Measured value*3*(2.5/4096) V
Channel 4	VCC_4V8_A	Measured value*3*(2.5/4096) V
Channel 5	VCC_3V3_A	Measured value*2*(2.5/4096) V
Channel 6	VCC_3V3_D	Measured value*2*(2.5/4096) V
Channel 7	VCC_3V3_REF	Measured value*2*(2.5/4096) V
Temperature	(internally generated)	AD7921 ADC TEMP * 0.0625 °C

Table 7: second AD7291 Voltage Parameters

Temperature monitor

Parameter:	Voltage	Formula
DP1/ DN1	ADC Diode A/ ADC Diode C	Measured value °C
DP2/ DN2	DAC diode/ DAC DGND	Measured value °C

Table 8: Temperature diode connections

Appendix A: Enable LXD30K0 powers

Through the I2C IO expander the carrier board FPGA can independently enable the power for the EV12DS460, EV12AS350, clock tree and reference clocks. By default all the powers are disabled at power-up.

Typically to power up the FMC board the following steps should be taken:

- Write 0x40 to IOexpander P0 output register
  - Select local reference and local clock with PLL disabled
- Write 0x00 to IO expander P1 output register
  - external IO is set to input and all power disabled
- Write 0x38 to IO expander P2 output register
  - All SPI CSN signals to 1 and DAC and ADC reset to 0
- Write 0x00 to IOexpander P0 control to set all outputs
- Write 0x00 to IOexpander P1 control to set all outputs
- Write 0x07 to IOexpander P0 control to set [2..0] to inputs and [7..3] to outputs
- Write 0x14 to IO expander P1 output register
  - Enable Switching regulators and DAC power supplies
- Write 0x1C to IO expander P1 output register
  - ADC power enabled
- Write 0x1E to IO expander P1 output register
  - PLL power supply enabled
- Write 0x1F to IO expander P1 output register
  - Reference power supply enabled

Appendix B: PLL configuration

Below is a table with the register values to write to the PLL that shows configures the PLL to 5Ghz based on the local 100 MHz reference clock. For this configuration to work the ADC clock mux, DAC clock mux and the reference clock mux should be set to Local. Also, the PLL and reference power supplies should be enabled and the PLL enable should be high. The registers should be written in the order of the index.

Table 9: PLL configuration table.

Index	SPI address:	Data to write	Index	SPI address:	Data to write
1	0x40	0x0077	23	0x1E	0x0034
2	0x3E	0x0000	24	0x1D	0x0084
3	0x3D	0x0001	25	0x1C	0x2924
4	0x3B	0x0000	26	0x19	0x0000
5	0x30	0x03FC	27	0x18	0x0509
6	0x2F	0x08CF	28	0x17	0x8842
7	0x2E	0x0F23	29	0x16	0x2300
8	0x2D	0x0000	30	0x14	0x012C
9	0x2C	0x0000	31	0x13	0x0965
10	0x2B	0x0000	32	0x0E	0x018C
11	0x2A	0x0000	33	0x0D	0x4000
12	0x29	0x03E8	34	0x0C	0x7001
13	0x28	0x0000	35	0x0B	0x0018
14	0x27	0x8204	36	0x0A	0x10d8
15	0x26	0x0032	37	0x09	0x0302
16	0x25	0x4000	38	0x08	0x1084
17	0x24	0x0810	39	0x07	0x28B2
18	0x23	0x001b	40	0x04	0x1943
19	0x22	0xC3EA	41	0x02	0x0500
20	0x21	0x2A0A	42	0x01	0x0808
21	0x20	0x210A	43	0x00	0x2218
22	0x1F	0x0401			

Appendix C: ADC configuration

Below is a table with the typical initialization sequence to configure the ADC and to train the LVDS interface in the FPGA. This sequence assumes that training is done on a FLASH pattern 0x0D and a length of 10. Before running this sequence there should be a valid clock for the ADC.

Table 10: ADC configuration table.

Index	Action	Interface
1	Assert ADC nreset	I2C
2	Deassert ADC nreset	I2C
3	Set ADC LVDS to full swing	SPI
4	Disable ADC cores C and D (LPC mode only)	SPI
5	Set ADC reset length to 8	SPI
6	Set FLASH length to 10	SPI
7	Set data source to FLASH pattern to 0xD	SPI
8	Reset SERDES and IDELAY	FPGA
9	Set the ADC SYNC source to FPGA_SYNC	I2C
10	Drive a SYNC pulse of 16 clock cycles on the SYNC_FROM_FPGA pin	FPGA
11	Start IDELAY training in FPGA	FPGA
12	Set the ADC data source to RAMP	SPI
13	Select the Appropriate Calibration data (HOT, COLD, interpolated	SPI
14	Read a burst of data from the ADC	FPGA
15	Verify If the RAMP pattern is contiguous and aligned per ADC channel.	Software
16	Set the ADC data source to ADC	0x4000

Appendix D: DAC configuration

Below is a table with the typical initialization sequence to configure the DAC and to train the LVDS interface in the FPGA. This sequence assumes that training is done on a FLASH pattern 0x0D and a length of 10. Before running this sequence there should be a valid clock for the ADC.

Table 11: ADC configuration table.

Index	Action	Interface
1	Set the ADC and DAC SYNC source to FPGA_SYNC	I2C
2	Drive a SYNC pulse of 16 clock cycles on the SYNC_FROM_FPGA pin	FPGA
3	Assert the OCDS signal towards the DAC	I2C
4	Assert the DAC NCS	I2C
5	Assert the DAC nreset	I2C
6	De-assert the DAC nreset	I2C
7	De-assert the DAC NCS	I2C
8	Set DAC state register to 0x921	SPI
9	Set the ADC and DAC SYNC source to FPGA_SYNC	I2C
10	Drive a SYNC pulse of 16 clock cycles on the SYNC_FROM_FPGA pin	FPGA
11	Reset SERDES and ODELAY	FPGA

Appendix E: Revision history

Document Revision	Changes			Quality Approval	Date
R1.0	Initial Release			EBa	April 7 2020