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OpenVPX

FMC™

VF361
ARRIA® V SOC FPGA MODULE WITH DUAL-CORE ARM, DSP CO-PROCESSOR AND FMC FOR DEMANDING COMPUTATION AND I/O APPLICATIONS

The **VF361** is a 3U OpenVPX module that leverages on INTEL Arria® V SOC FPGA, ARM Cortex-A9, and Texas Instruments KeyStone Multicore DSP technology to provide a high bandwidth processing platform, ideally suited for computation and bandwidth intensive applications such as Radar, Networking, SIGINT, EW, SDR and Video.

The Arria® V SOC FPGA integrates a Hard Processor System (HPS) with dual-core ARM Cortex-A9 MPCore processor, DDR SDRAM Controller, Memory Management Unit (MMU) and numerous interface peripherals into the FPGA.

The ARM Neon™ media processing engine with double-precision vector floating-point (VFP) unit accelerates multimedia and signal processing algorithms.

The ARM processor supports symmetric (SMP) and asymmetric (AMP) multiprocessing, running from simple bare-metal applications to single and multicore operating systems like Linux, VxWorks® and others. It is ideal for safety- and mission critical software applications.

The ARM Development studio (DS-5) Intel Edition provides a suite of tools for embedded C/C++ software development with powerful debugging capabilities such cross-trigger (FPGA   ARM) debug, program trace and multi-core debug through the ARM Coresight™ JTAG debug port.

A PC based Intel SOC virtual target allows firmware and software development to start on a virtualized Intel development board.

Specifications

SOC FPGA

- Arria® V SX family in the KF40 (1517 FBGA) package
  - SX Device variants: B3 and B5
- Hard Processor System (HPS)
- Embedded device memory: 19-25 Mb
- Embedded device multipliers (18x18): 1,618 – 2,180
- DDR3 ARM external memory
  - Up to 1GB DDR3 @ 667MHz, default 512MB
- DDR3 and QDRII+ FPGA external memory
  - Up to 1GB DDR3 @ 667MHz (arranged as 256M x 32-bit), default 512MB
  - Up to 16MB QDRII+ SRAM @ 400MHz (arranged as 8M x 18-bit), default 8MB

Hard Processor System (HPS)

- Dual-core ARM Cortex-A9 MPCore processor
- ARM Neon™ media processing engine with double precision vector floating point (FVP)
- 8-channel DMA controller
- USB On-The-Go controller (OTG)
- Numerous other system and interface peripherals
- ARM CoreSight™ JTAG debug access port

Digital Signal Processor

- Ti KeyStone Multicore C667x family of processors
  - Up to 8 cores @ 1.2 GHz
External memory: Up to 2 GB DDR3 @ 667MHz, default 1GB

FPGA Mezzanine Card (FMC)

- 5x High-Speed Serial Interface lanes
- Differential and single-ended interfaces on LA and HA

VPX Interface

- Comply with OpenVPX MOD3-PAY-3F2U-16.2.12-2 module profile
  - PCIe Gen2 Data plane (3x Fat Pipes)
  - GigE 1000BASE-BX Control plane (2x Ultra-Thin Pipes)
  - Payload module with System Controller capability
- Supports FPGA configurable User I/O on P2
  - 24x single-ended 2.5V LVCMOS I/Os
  - 5x High-Speed Serial Interface lanes

Software & Firmware Support

- Board support package for Bare-metal, Linux and VxWorks (on request)
  - Sample application
  - FPGA Firmware reference design
- VR301 Test RTM with USB-Blaster II, ARM Coresight debug port, DSP XDS100 and Ethernet (via SFP)

intel FPGA Design Solutions Network Gold

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The Arria® V FPGA connects to dedicated DDR3 and QDRII+ memories for algorithms with high bandwidth and/or large memory size requirements. High-speed serial interfaces to the OpenVPX data plane and the FMC site creates abundant FPGA IO throughput.

The multicore DSP from Texas Instruments acts as co-processor to perform complex post processing DSP functions. High bandwidth communication between the DSP and FPGA is provided through both PCIe and Serial Rapid IO (SRIO) interfaces.

The **VF361** FMC carrier enables modular solutions that accommodate a wide range of I/O requirements.

The **VF361** conforms to the OpenVPX standard and operates as a Payload module with System Controller capability. Both aircooled and conduction cooled versions are available. Further flexibility is provided through build options to cater for different FPGA's from Intel's Arria® V SX device family.

FMC Companion Modules

- FM501 Test FMC with USB-Blaster II, ARM Coresight debug port, XDS100 and mini-SAS interfaces
- FM510 Video IO FMC
- FM550 Two Channel mini-SAS I/O FMC
- FM570 Dual Channel DAC FMC
- FM580 Eight Channel ADC FMC

Typical Applications

- System Controllers and Mission Computers
- Radar Signal Processing (Doppler filter, Pulse compression, CFAR)
- Spectrum analysis in EW (Signal detection & classification, jammer control)
- Video and image processing (DCT, 1D/2D convolution, etc.)
- Software Defined Radio (SDR)
- Real-time DSP functions (DDC, FFT, FIR, NCO, etc.)

Ordering Information

Generic order code = VF361-A-B-C-D-E-F-G
A: SOC FPGA (B3, B5) for 5ASXB3 or 5ASXB5 with dual-core ARM
B: Speed grade (4 or 6) for Transceiver speed, (C or I) for Commercial/Industrial temp (3 to 6) for FPGA speed
C: DSP co-processor (1, 2, 4 or 8) for TMS320C667X one, two, four or eight core
D: DDR3 (2 or 4) GB total DDR3 memory (512MB | 1GB for ARM+ 512MB | 1GB for FPGA + 1GB | 2GB for DSP)
E: QDRII+ (8 or 16) MB total QDRII+ memory for FPGA
F: THERMAL (0 or 1) for air-cooled or conduction cooled
G: Conformal Coating (0 or 1) for un-coated or coated

Standard order code = VF361-B3-4I4-4-2-8-0-0
5ASXB3 FPGA 4 | 4 speed grade (Industrial temperature)
TMS320C6674 four core DSP
DDR3 = 2GB, 512MB for ARM + 512MB for FPGA + 1GB for DSP
QDRII+ = 8MB for FPGA
Air-cooled, un-coated
Contact factory for other order options

Block Diagram