MICROCHIP POLARFIRE

SoM3-MPF300T

User Guide

Revision History

Revision	Comments	Originator	Date
1.0	Initial draft	Stephen Malchi	Mar 18th 2019
1.1	Updated FPGA Bank Assignment	Stephen Malchi	Apr 16th 2019
1.2	Added FlashPro5 EMC2 connectivity	Stephen Malchi	May 14th 2019
1.3	Updated level translator description	Stephen Malchi	Jan 22nd 2020
1.4	Updated operating temperature	Stephen Malchi	Feb 28th 2020
1.5	Updated MTBF	Stephen Malchi	Mar 12th 2020
1.6	Updated Storage temperature	Stephen Malchi	Apr 14th 2020
1.7	Updated operating temperature	Stephen Malchi	July 14th 2020
1.8	Updated JM3 pinout	Stephen Malchi	July 30th 2020
1.9	Updated section 1.1; 3.5;3.7; replaced 3.6 with new tables.	KMA	March 20th 2021
2.0	Updated text on SPI FLASH access from EMC2, etc	NN	April 20th 2022
2.1	Added DDR Libro setting	NN	Oct. 11th, 2022
2.2	Removed DDR pin out tale	NN	Oct. 19th, 2022
2.3	Added MPF300TS explicitly and its features	NN	Dec. 9th, 2022
2.4	Added link on how to remove SOM from carrier and using SOM3 with Trenz carrier	NN	Jan. 11th, 2023
2.5	Corrected SPI flash section, added comments on DDR4 memory section, added differences between rev 0.1 and rev 1.0 SOM3s	RC	Aug 17th, 2023

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2.6	Corrected JM3 Pinout table	RC	Oct. 19th, 2023
2.7	Clarified new DC-DC converter on rev1.0	RC	Aug. 8th, 2024

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1 INTRODUCTION

SoM3-MPF300T or SOM3-MPF300TS (SOM3) is a System on Module (SoM) with a powerful, low power, high security PolarFire device from Microsemi (now part of Microchip). It is based on MPF100/200/300 (as default it is populated with 300T) range of devices in FCVG484 (19mm x 19mm) package with ample processing resources and many soft IPs such as JESD204B, RISC-V and many more. SoM3 also offers an Ethernet PHY, one bank of DDR4 memory and SPI flash that makes it a low power, cost optimized solution in the field of Defense, Communications and Industrial applications.

1.1 HARDWARE FEATURES

The hardware has the following features:

- Microsemi MPF300T-1FCVG484E as default; It can also be populated with MPF300TS version.
- 4 GB of 32-bit wide DDR4 memory using 2 MT40A1G16WBU-083E from Micron (stacked 2 x8 8Gb chips), speed limited to 1600MHz;
- 256Mb SPI Serial NOR FLASH for storing boot image;
- 10/100/1000Mbit Ethernet PHY on board;
- Programmable clocks using - SI5338A-B-GM – provides flexible clocking to FPGA and High-Speed transceivers. Uses onboard 25MHz ±10ppm reference oscillator;
- 4 High-speed low-power Transceivers from 250Mbps – 12.7Gbps;
- 136 IO's via high speed Samtec LSHM™ connectors
- B2B Connectors: from Samtec - LSHM-130-04.0-L-DV-A-S-K-TR and LSHM-150-04.0-L-DV-A-S-K-TR;
- Power range for FPGA banks: 1.2V – 2.5V. LVDS available only at 2.5V;
- Mechanical dimensions are 40 x 50 mm;
- Power IN from 3.3V to 5.5V on rev 0.1, on rev1.0 Power IN is 4.5V to 5.5V;
- Approximate power consumptions for FPGA is 7W, and total maximum power consumption is 10W (depends on the IP core);
- Temperature range 0°C to +65°C.

1.2 SOM MODULES LIMITATIONS AND NOTES.

1. **WARNING! VAUX for FPGA Banks connected to 2.5V. So maximum allowable banks voltage is limited to 2.5V or device damage may occur!**
2. **VIN and VIN_3V3 power must be powered first, then banks power can be applied, otherwise device damage can occur!**

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3. **Note LSHM connector pin numbering with vertical mating part is not 1 to 1. Mating numbering are 1 to 2, 2 to 1, 3 to 4, 4 to 3 etc.**
4. Due to internal FPGA limitations, effective data lanes speed of DDR4 interface is reduced to 1600Mb/s – clock rate maximum 800MHz.
5. If MPFxxxTS is populated, then it may require additional documentation to export from the United States. This is due to encoding features of the device.
6. **Note rev1.0 SOM3s have a different DC/DC converter for the FPGA core voltage (PN MYMGK1R820FRSR). This changes the VCC_IN voltage range to 4.5V to 5.5V. Additionally, the DDR4 package footprint was increased to accommodate newer Micron package types. Some passive components have been moved or removed from the design to accommodate for these changes.**
7. **On rev 1.0 SOM3s produced after 08/2023 require a different FW configuration for DDR4 (BG1 signal must be tied low in the FW)**

1.3 ACRONYMS, ABBREVIATIONS AND DEFINITIONS

JTAG	Joint Test Action Group (IEEE 1149.1 test access port)
FPGA	Field Programmable Gate Array
PCB	Printed Circuit Board
GPIO	General Purpose I/O
SoM	System on Module
TBD	To Be Discussed.

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2 BOARD DESCRIPTION

SoM3 includes DDR4 memory and SPI flash. The module has two 100-pin high speed LSHM-150-04.0-L-DV-A-S-K-TR and one 60 pin LSHM-130-04.0-L-DV-A-S-K-TR LSHM™ “Razor Beam” connector from Samtec. The core voltage for the FPGA is generated on board. The IO bank voltages are provided from the Razor Beam™ connectors. All the IO’s and high-speed transceivers are accessed through these connectors. The block diagram is shown below:

2.1 BLOCK DIAGRAM

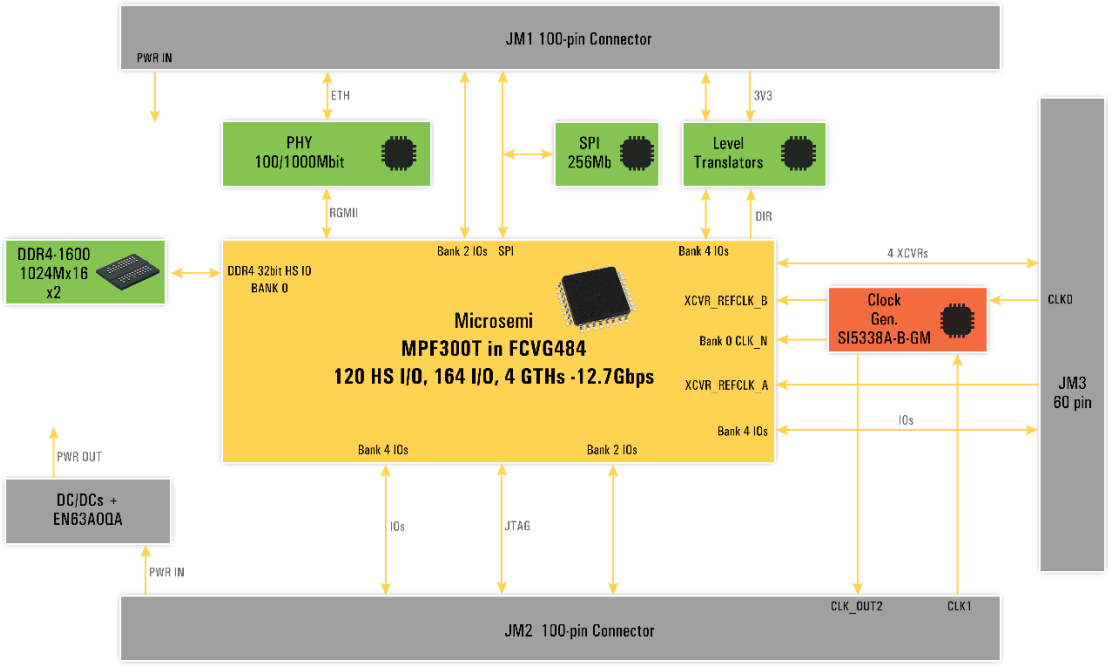

Figure 1 - Block diagram of SoM3-MPF300T

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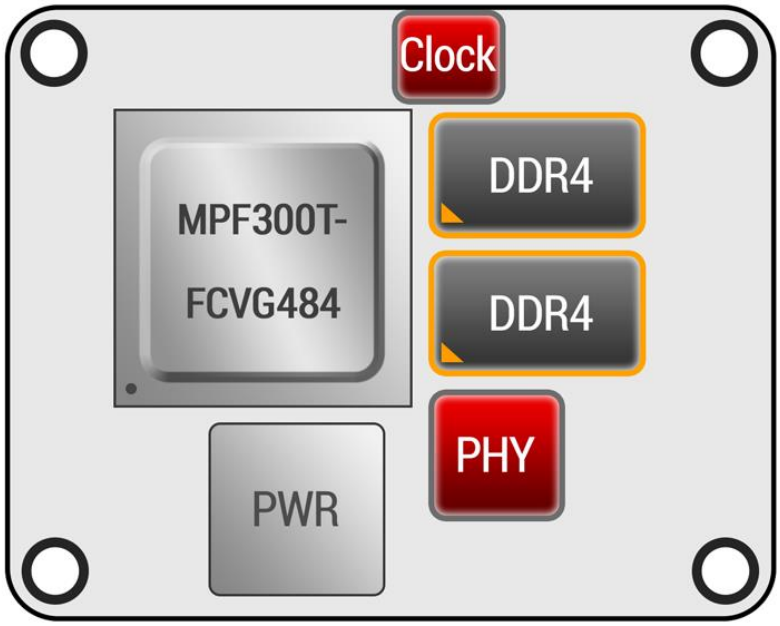

Figure 2 - Placement diagram of component side

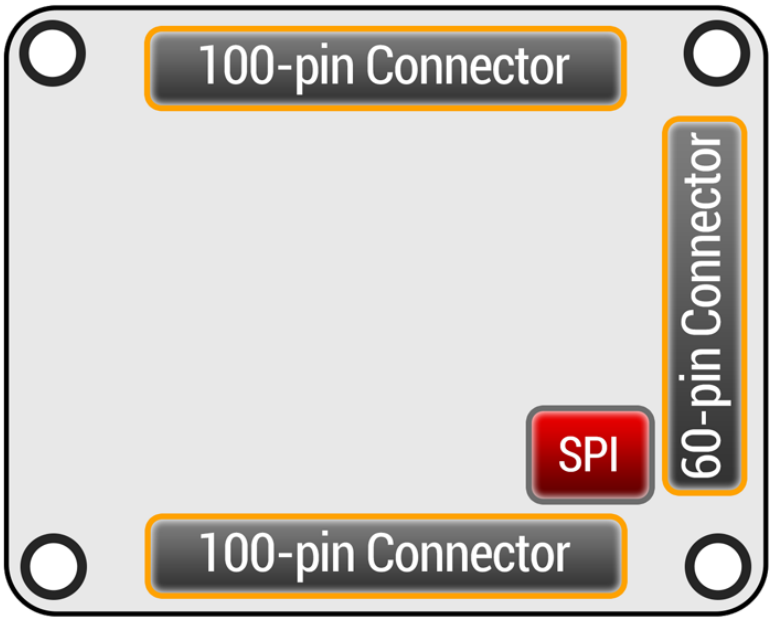

Figure 3 - Placement diagram of solder side

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2.1.1 Dimensions

Width: 40mm

Length: 50 mm

Thickness: 9.4 mm

3D Model for measurement purposes

2.1.2 Environmental

- Operating junction temperature (Tj)
  - Extended Commercial: 0˚C to 85˚C
  - Industrial: -40˚C to 85˚C

Notes:

1. A thermal solution must be designed to ensure that the board does not exceed the maximum (Tj) during operation.
2. Device functionality is not guaranteed if the board exceeds maximum (Tj) during operation.

- Storage temperature: -65˚C to +150˚C
- Humidity: 10% to 90% non-condensing

2.1.3 Operating Voltage

Provided from the carrier card via Samtec LSHM-150-04.0-L-DV-A-S-K-TR connectors

2.1.4 MTBF

The MTBF for SoM3 without the carrier card is 3831845 hrs

2.1.5 Ordering Information

SoM3-D-S-T

D	=	MPF300T or MPF200T or MPF100T	
S	=	Blank	(STD Speed Grade)
		-1	(15% Faster)
T	=	E	(Extended Commercial Tj = 0 C to 100 C)
		I	(Industrial Tj = -40 C to 100 C)

Note: SoM3 comes with MPF300T as default. Customers have the option of ordering the module with MPF200T or MPF100T. The device also comes in different speed and temperature variants.

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2.2 BOARD IMAGES

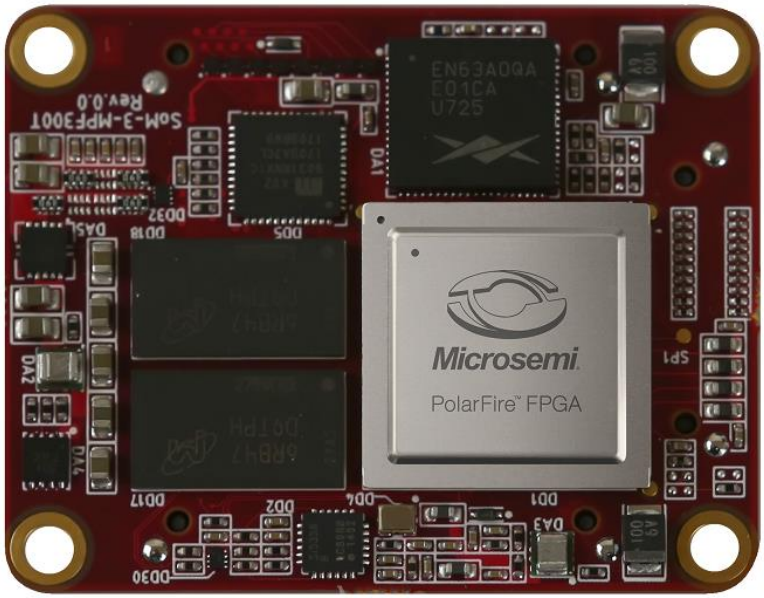

Figure 4 - SoM3 Component side

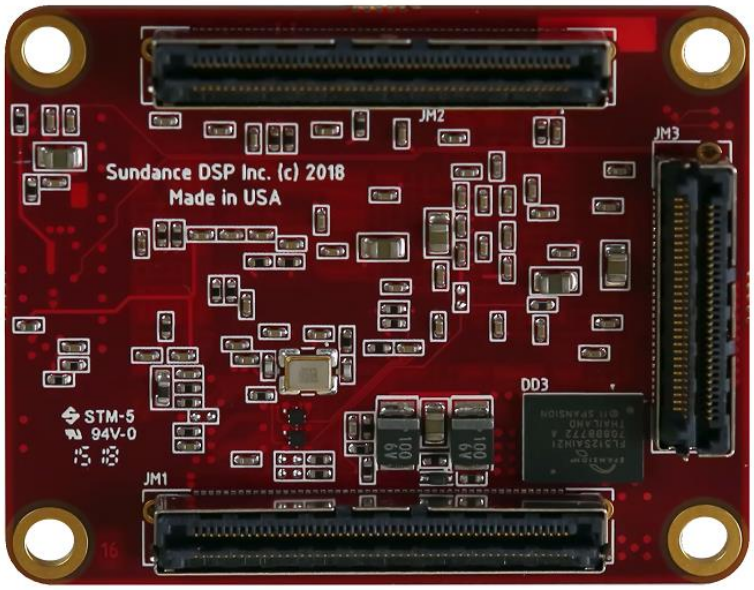

Figure 5 - SoM3 Solder Side

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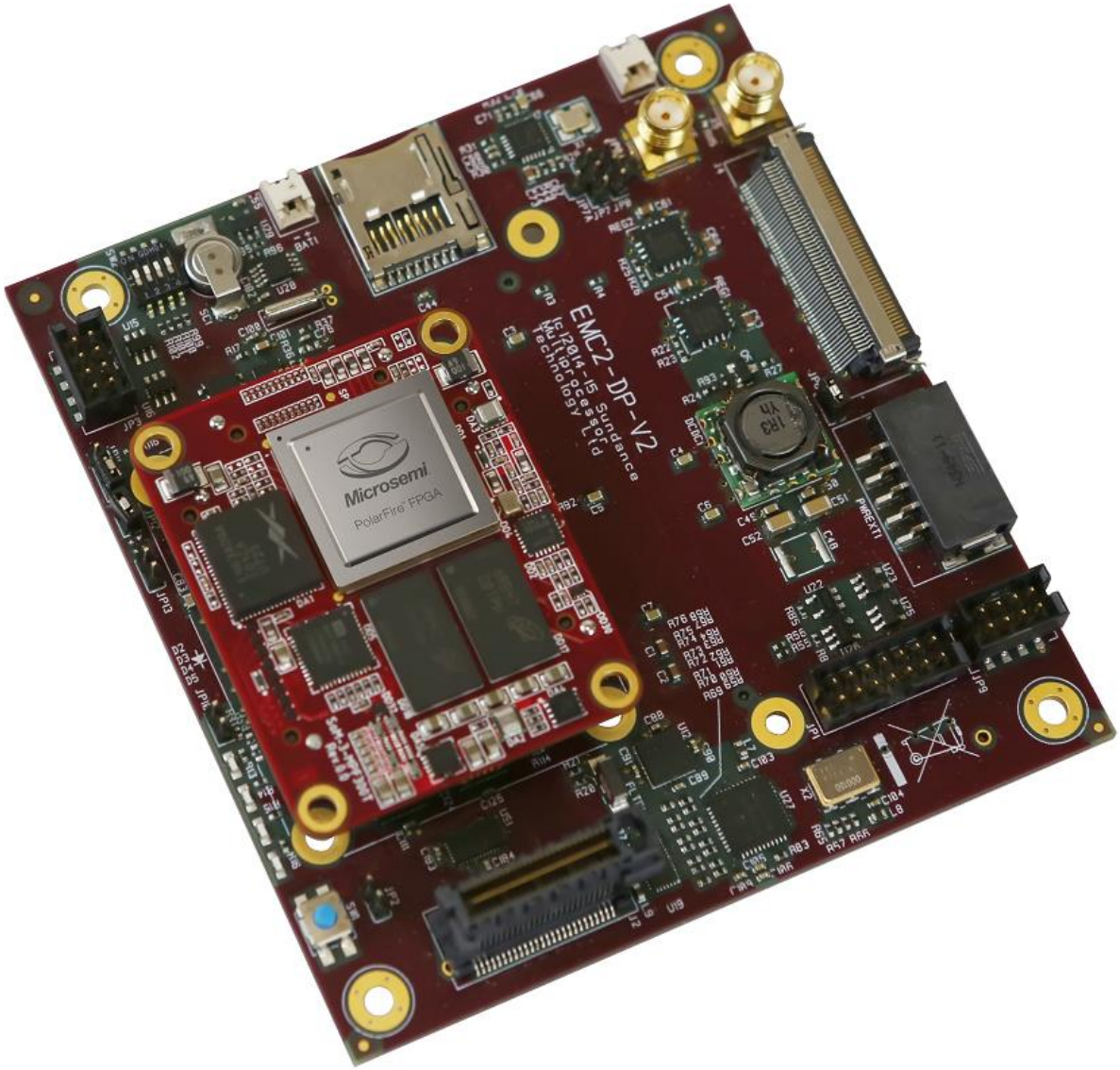

Figure 6 - SoM3 populated on EMC2-SoM

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3 BOARD COMPONENT DESCRIPTION

The functional description of the board components and pinouts are provided below.

3.1 MPF300T-FCVG484E

SoM3 is populated with MPF300T-FCVG484E device which has 300K logic cells, 4 high speed transceivers, two PCIe hard blocks and 284 IO's (120 HSIO's, 164 GPIO's). The HSIO pins are connected to 32-bit DDR4 interface and out of 164 GPIO's 12 are connected to 1Gb ethernet PHY and 152 are connected to LSHM connectors.

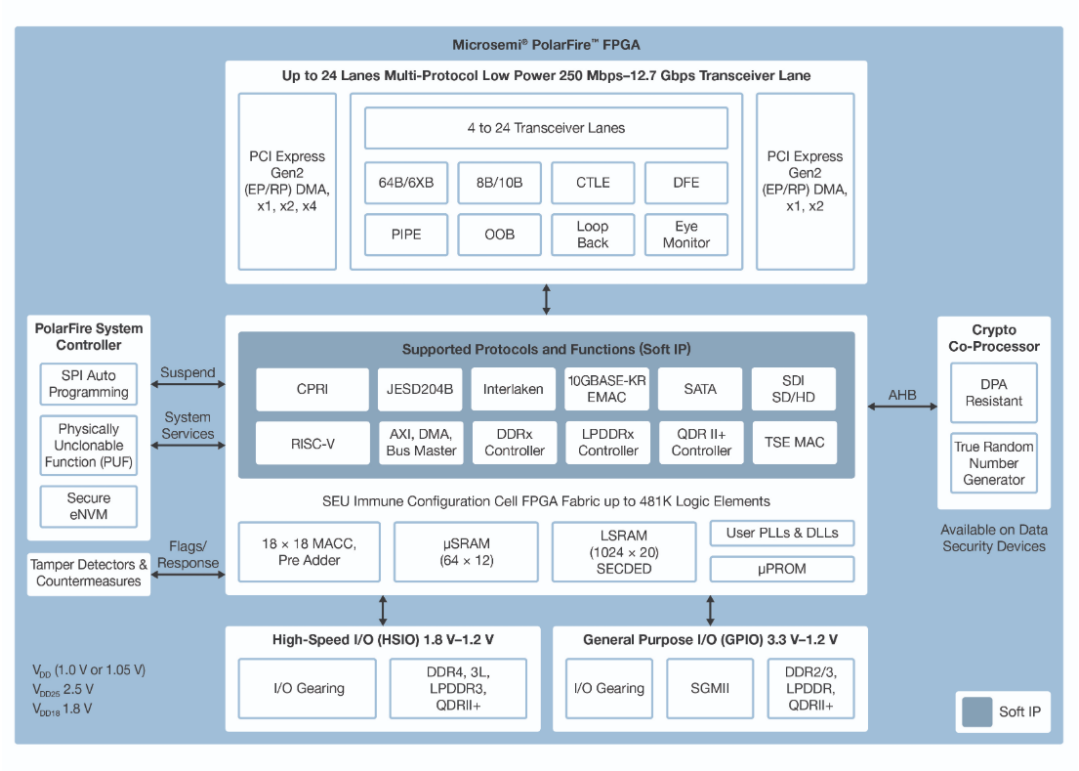

Figure 7 - Microsemi Polar Fire Block Diagram

More information on the MPF devices can be found in the link below

https://www.microsemi.com/product-directory/fpgas/3854-polarfire-fpgas#overview

Note: The SoM3 can alternatively be populated with MPF100Tand MPF200T devices, with the same number of IO's and transceivers as MPF300T but with less logic elements. Optional faster speed-grade and extended temperature range are available.

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3.2 FPGA BANK ASSIGNMENTS

Interface	MPF300T Bank	VCCIO
DDR4	0	1.2v
DDR4	1	1.2v
JM1/JM2	2	1.2v – 2.5v
JTAG/SPI	3	1.8v
JM1/JM2/JM3	4	1.2v – 2.5v

Table 1 - FPGA Bank Assignments

Bank 0 and Bank 1 are HSIO banks and the IO's are connected to DDR4 memory. Banks 2 and 4 are GPIO banks connected to SoM connectors JM1/JM2 and JM3.

Note: The max allowable IO voltage on Banks 2 and 4 is 2.5v as noted in section 1.2 (1).

For available IO Standards on MPF FPGA's please refer to

Microsemi_PolarFire_FPGA_Product_Overview_PO0137_15.pdf

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3.3 DDR4 MEMORY

The FPGA is connected to 2x16Gb (total of 4GByte) DDR4 components from Micron MT40A1G16WBU-083E:B, which provides a 32-bit wide memory (see note below).

Connection is standard for this FPGA and can be fully configured via Libero software. DDR4 interface located at NORTH_NE anchor.

Note: MT40A1G16KNR-062E:E and MT40A1G16WBU-083E:B are obsolete DDR4 components. All boards produced after 8/2023 will have MT40A1G16TB-062E IT:F installed. This memory type requires a change to the Bank Group addressing in the FW design (ONLY BG0 is used BG1 must be tied low in the FW)

3.4 SPI SERIAL NOR FLASH MEMORY

SPI flash memory (256 Mb) is connected to the FPGA (see note below for capacities of the SPI flash and types used). The serial NOR Flash is used for storing boot image for the FPGA and data storage.

- Part number: S25FS256SAGBHI200
- Supply voltage: 1.8V
- Maximum clock: 133 MHz

Connections between SPI flashes and FPGA are listed below.

FPGA Pin	Signal
H6	SPI_M/S#
H5	SPI_CLK
G9	SPI_MISO
H4	SPI_MOSI
H9	SPI_EN
F8	SPI_CS#

Table 2 - SPI FLASH to FPGA Pinout

The SPI interface is connected to JM1 Samtec LSHM™ connector.

Writing to SPI flash can be accomplished by:

1. A firmware supplied as part of BSP supplied by SDSP.
2. Through JTAG using one of SDSP carrier cards like SE215 or SE216 via Libro tool. **(ONLY Micron Flash can be targeted via Flash Pro 5 using Libero)**

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3. Through SPI connector on the SE215 carrier using a suitable host side SPI software.

Note: Depending on SPI flash component availability. The SOM3 may be populated with 512Mb or 1Gb flash parts (MT25QU512ABB8E12-0SIT, MT25QU01GBBB8E12-0SIT). Contact SDSP if a certain SPI Flash capacity is required by the application.

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3.5 RGMII INTERFACE

Bank 2 of the FPGA is connected to an Ethernet RGMII PHY before being routed to JM1 connector, which implements a Gigabit ethernet (10/100/1000 Mb ethernet)

- PHY IC: KSZ9031RNXIC – MicroChip;
- Speed modes: 10/100/1000BASE;
- Link capabilities: Auto MDI/MDI-X, Cable diagnostics;
- Transformer centre tap: must be separated, and AC coupled to GND.

Connections between RGMII PHY interface and FPGA Bank 2 are listed below.

MPF300T-1FCVG484E		Schematic Net Name	PHY IC	
Pin Name	Ball Number		Pin number	Pin name
GPIO19NB2, GPIO19PB2, GPIO21PB2, GPIO21NB2	A16, A15, C15, C14	RGMII_TXD[0:3]	19 - 22	TXD[0:3] (in)
GPIO20NB2/DQS	B17	RGMII_TX_CTL	25	TX_EN (In)
GPIO20PB2/DQS	A17	RGMII_TXC	24	GTX_CLK (In)
GPIO0NB2, GPIO0PB2, GPIO1PB2, GPIO1NB2	D8,E8, B8, A8	RGMII_RXD[0:3]	27,28,31,32	RXD[0:3]
GPIO2NB2/DQS	D9	RGMII_RX_CTL	33	RX_DV
GPIO2PB2/DQS	E9	RGMII_RXC	35	RX_CLK
HSIO162PB0	W6	RGMII_MDC	36	MDC
HSIO163PB0, HSIO164PB0	T6, V5	RGMII_MDIO	37	MDIO
HSIO161PB0	Y5	RGMII_RES#	42	RESET_N
HSIO168P/CLKIN_N_3	W2	RGMII_CLK125	41	CLK125_NDO(Out from PHY)

Table 3 - RGMII to FPGA Pinout

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3.6 SAMTEC LSHM CONNECTOR

SoM3 has two high speed 100 pin LSHM connectors and one 60 pin LSHM connector from Samtec. These connectors are used to provide 5v input voltage to power up the module and provide IO bank voltages generated on the carrier card. All the interfaces on the FPGA (4 transceivers and 136 GPIO's) are taken to these connectors. The reference designators of the connectors are JM1, JM2, JM3.

For removing a SOM3 from the carrier card please follow instructions on this video:

How to remove a SoM from a EMC2 - YouTube

Note: LSHM connector pin numbering with vertical mating part is not 1 to 1. Mating numbering are 1 to 2, 2 to 1, 3 to 4, 4 to 3 etc.

The pinout of these high-speed connectors is given below:

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3.6.1 JM1 Connector Pinout (LSHM-150-04.0-L-DV-A-S-K-TR)

FPGA ball	Pin name	Pin number		Pin name	FPGA ball
	VIN(3.3V – 5.5V)	1	2	GND	
	VIN(3.3V – 5.5V)	3	4	ETH_A_p	
	VIN(3.3V – 5.5V)	5	6	ETH_A_n	
	N.C.	7	8	GND	
	VCCIO_B2	9	10	ETH_B_p	
	VCCIO_B2	11	12	ETH_B_n	
	VIN_3V3	13	14	N.C.	
	VIN_3V3	15	16	ETH_C_p	
F8	SPI_CS# (PU 10k to 1V8)	17	18	ETH_C_n	
	N.C.	19	20	GND	
	N.C.	21	22	ETH_D_p	
G9	SPI_MISO	23	24	ETH_D_n	
H4	SPI_MOSI	25	26	GND	
H5	SPI_CLK (PD 1k)	27	28	SPI_EN (PU 10k to 1V8)	H9
	GND	29	30	N.C.	
A2	B2_SW_PLL1_OUT0/GPIO246/DQS+	31	32	SPI_M/S# (diode + PU 10k to 1V8)	H6
A3	B2_SW_PLL1_OUT0/GPIO246/DQS-	33	34	GND	
A5	B2_GPIO253+	35	36	B2_SW_PLL1_OUT1/GPIO248+	D4
A6	B2_GPIO253-	37	38	B2_SW_PLL1_OUT1/GPIO248-	C4
	VCC_1V8_OUT	39	40	B2_GPIO250+	E5
B10	B2_GPIO5-	41	42	B2_GPIO250-	E6
C10	B2_GPIO5+	43	44	GND	
D6	B2_GPIO252/DQS+	45	46	B2_GPIO251+	C5
C6	B2_GPIO252/DQS-	47	48	B2_GPIO251-	B5
C7	B2_GPIO254+	49	50	B2_GPIO255+	A7
D7	B2_GPIO254-	51	52	B2_GPIO255-	B7
	GND	53	54	GND	

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FPGA ball	Pin name	Pin number		Pin name	FPGA ball
A10	B2_GCLK/GPIO6+	55	56	B2_GPIO3+	B9
A11	B2_GCLK/GPIO6-	57	58	B2_GPIO3-	C9
C11	B2_GCLK/GPIO7+	59	60	B2_GPIO4+	F10
D11	B2_GCLK/GPIO7-	61	62	B2_GPIO4-	E10
	GND	63	64	GND	
C12	B2_GCLK/GPIO9+	65	66	B2_GCLK/GPIO11+	A12
D12	B2_GCLK/GPIO9-	67	68	B2_GCLK/GPIO11-	B12
D14	B2_GPIO10+	69	70	B2_GPIO12+	H12
D13	B2_GPIO10-	71	72	B2_GPIO12-	G12
	GND	73	74	GND	
F16	B2_CLK_SE/GPIO35+	75	76	B2_GPIO8/DQS+	A13
E16	B2_CLK_SE/GPIO35-	77	78	B2_GPIO8/DQS-	B13
	N.C.	79	80	B2_GPIO23-	B14
M4	B4_GCLK/CLK_W/NW_PLL0_OUT1/GPIO180-	81	82	B2_GPIO23+	B15
M5	B4_GCLK/CLK_W/NW_PLL0_OUT1/GPIO180+	83	84	GND	
N2 N1	B4_GPIO181/DQS+ (int. converted to 3V3) DIR pin – B4_GPIO179+	85	86	B2_GPIO18-	C16
K3 J3	B4_GPIO217/DQS- (int. converted to 3V3) DIR pin – B4_GPIO217/DQS+	87	88	B2_GPIO18+	C17
H7	JTAG_TRST# (diode + PU to 1V8)	89	90	GND	
J1 H2	B4_GCLK/GPIO215- (int. converted to 3V3) DIR pin – B4_GPIO218+	91	92	B4_GLCK/CLK_NW/GPIO216+ (int. converted to 3V3) DIR pin – B4_GLCK/GPIO216-	L3 L2
P1 P2	B4_GPIO179- (int. converted to 3V3) DIR pin – B4_GPIO181/DQS-	93	94	B4_GCLK/CLK_W/NW_PLL0_OUT0/GPIO174-	T1
J2 H1	B4_GPIO218- (int. converted to 3V3) DIR pin – B4_GCLK/GPIO215+	95	96	B4_GCLK/CLK_W/NW_PLL0_OUT0/GPIO174+	R1
P4 P3	B4_GPIO183+ (int. converted to 3V3) DIR pin – B4_GPIO183-	97	98	B4_GPIO176-	T2

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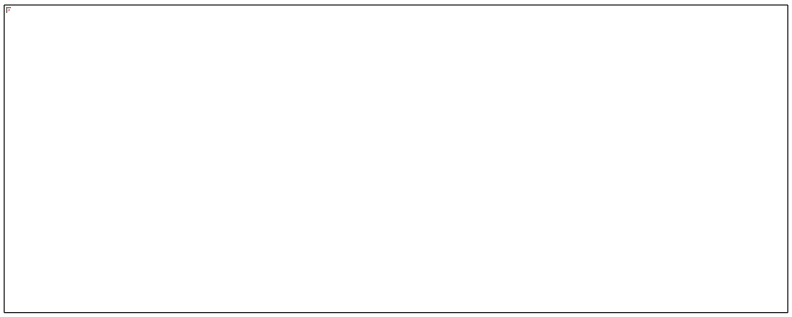
FPGA ball	Pin name	Pin number		Pin name	FPGA ball
L1 K1	B4_GPIO214- (int. converted to 3V3) DIR pin – B4_GPIO214+	99	100	B4_GPIO176+	T3

Table 4 - JM1 Connector Pinout

Note: There are eight 3.3v tolerant pins on JM1 connector which are connected to the FPGA via level translators 74AVC1T45GS,132

(Pins 85, 87, 91, 92, 93, 95, 97, 99)

https://www.nexperia.com/products/analog-logic-ics/asynchronous-interface-logic/voltage-translators-level-shifters/74AVC1T45GS.html



As shown in the above figure for Pin 85. ‘A’ is connected to FPGA pin N2, ‘DIR’ pin is connected to FPGA pin N1. ‘B’ is connected to pin 85 of LSHM connector and is 3.3v tolerant.

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3.6.2 JM2 Connector Pinout (LSHM-150-04.0-L-DV-A-S-K-TR)

FPGA ball	Pin name	Pin number		Pin name	FPGA ball
	VCCIO_B4	1	2	VIN(3.3V – 5.5V)	
	VCCIO_B4	3	4	VIN(3.3V – 5.5V)	
	VCCIO_B4	5	6	VIN(3.3V – 5.5V)	
	VCCIO_B2	7	8	VIN(3.3V – 5.5V)	
	VCCIO_B2	9	10	VIN_3V3	
J9	B4_GPIO213-	11	12	VIN_3V3	
J8	B4_GPIO213+	13	14	B4_SW_PLL0_OUT1/GPIO238+	F2
P9	B4_GPIO186-	15	16	B4_SW_PLL0_OUT1/GPIO238-	G2
R8	B4_GPIO186+	17	18	DEV_RST# (diode + PU 10k to 1V8)	G8
	N.C.	19	20	GND	
F5	B4_GCLK/CLK_SW/GPIO243-	21	22	B4_GPIO210-	J6
G5	B4_GCLK/CLK_SW/GPIO243+	23	24	B4_GPIO210+	J7
G4	B4_GCLK/CLK_SW/GPIO240+	25	26	B4_GCLK/CLK_SW/GPIO219-	J4
G3	B4_GCLK/CLK_SW/GPIO240-	27	28	B4_GCLK/CLK_SW/GPIO219+	K4
	N.C.	29	30	GND	
N7	B4_GPIO187/DQS+	31	32	B4_GPIO212	L8
N6	B4_GPIO187/DQS-	33	34	B4_GPIO212-	L7
P8	B4_GPIO184-	35	36	B4_GPIO185+	M8
P7	B4_GPIO184+	37	38	B4_GPIO185-	M7
	GND	39	40	GND	
D21	B2_GCLK/CLK_SE/GPIO29+	41	42	B2_GCLK/CLK_SW/GPIO249+	B3
D20	B2_GCLK/CLK_SE/GPIO29-	43	44	B2_GCLK/CLK_SW/GPIO249-	B4
C19	B2_SE_PLL0_OUT1/GPIO28-	45	46	B2_CLK_SE/SE_PLL1_OUT0/GPIO33-	D18
C20	B2_SE_PLL0_OUT1/GPIO28+	47	48	B2_CLK_SE/SE_PLL1_OUT0/GPIO33+	D19
	GND	49	50	GND	
C2	B2_GCLK/CLK_SW/PLL1_OUT0 /GPIO247+	51	52	B2_CLK_SW/GPIO244+	E4
B2	B2_GCLK/CLK_SW/PLL1_OUT0 /GPIO247-	53	54	B2_CLK_SW/GPIO244-	D3
	CLK0_SI5338+ (IN)	55	56	B2_CLK_SW/GPIO245+	C1
	CLK0_SI5338- (IN)	57	58	B2_CLK_SW/GPIO245-	B1
	GND	59	60	GND	
	CLK_OUT2- (OUT)	61	62	B2_GPIO25+	A20
	CLK_OUT2+ (OUT)	63	64	B2_GPIO25-	A21
E18	B2_GPIO31-	65	66	B2_GPIO24+	B19
E19	B2_GPIO31+	67	68	B2_GPIO24-	B20
	GND	69	70	GND	
G17	B2_GPIO30-	71	72	B2_GPIO16+	E14

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FPGA ball	Pin name	Pin number		Pin name	FPGA ball
F17	B2_GPIO30+	73	74	B2_GPIO16-	E13
D17	B2_SE_PLL1_OUT0/GPIO32/DQS+	75	76	B2_GPIO14/DQS+	F11
D16	B2_SE_PLL1_OUT0/GPIO32/DQS-	77	78	B2_GPIO14/DQS-	E11
	GND	79	80	GND	
F15	B2_SE_PLL1_OUT1/GPIO34+	81	82	B2_GPIO13+	F13
E15	B2_SE_PLL1_OUT1/GPIO34-	83	84	B2_GPIO13-	F12
G14	B2_GPIO17+	85	86	B2_GPIO15+	G15
G13	B2_GPIO17-	87	88	B2_GPIO15-	H15
B22	B2_SE_PLL0_OUT0/GPIO26/DQS-	89	90	GND	
	VCC_1V8_OUT	91	92	B2_GPIO22+	A18
F6	TMS	93	94	B2_GPIO22-	B18
G7	TDI	95	96	B2_GCLK/CLK_SE/SE_PLL0_OUT0 /GPIO27+	C22
F7	TDO	97	98	B2_GCLK/CLK_SE/SE_PLL0_OUT0 /GPIO27-	D22
H10	TCK (PD 10k)	99	100	B2_SE_PLL0_OUT0/GPIO26/DQS+	B21

Table 5 - JM2 Connector Pinout

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3.6.3 JM3 Connector Pinout (LSHM-130-04.0-L-DV-A-S-K-TR)

FPGA ball	Pin name	Pin number		Pin name	FPGA ball
D1	B4_GPIO241/SW_PLL0_OUT0 /DQS-	1	2	B4_GPIO242-	F3
D2	B4_GPIO241/SW_PLL0_OUT0 /DQS+	3	4	B4_GPIO242+	E3
	GND	5	6	GND	
T21	XCVR_TX3-	7	8	XCVR_RX3-	R19
T22	XCVR_TX3+	9	10	XCVR_RX3+	R20
	GND	11	12	GND	
P21	XCVR_TX2-	13	14	XCVR_RX2-	M22
P22	XCVR_TX2+	15	16	XCVR_RX2+	M21
	GND	17	18	GND	
H21	XCVR_TX1-	19	20	XCVR_RX1-	K22
H22	XCVR_TX1+	21	22	XCVR_RX1+	K21
	GND	23	24	GND	
F21	XCVR_TX0-	25	26	XCVR_RX0-	G20
F22	XCVR_TX0+	27	28	XCVR_RX0+	G19
	GND	29	30	GND	
N20	XCVR_REFCLK_B-	31	32	XCVR_REFCLK_C+	J19
N19	XCVR_REFCLK_B+	33	34	XCVR_REFCLK_C-	J20
	GND	35	36	GND	
M3	B4_GPIO178-	37	38	B4_GPIO177-	T5
M2	B4_GPIO178+	39	40	B4_GPIO177+	R5
K8	B4_GPIO211/DQS-	41	42	B4_GPIO175/DQS+	R3
K9	B4_GPIO211/DQS+	43	44	B4_GPIO175/DQS-	R4
	GND	45	46	GND	
M9	B4_GPIO189+	47	48	B4_GPIO188+	R6
N8	B4_GPIO189-	49	50	B4_GPIO188-	P6
L5	B4_GPIO208+	51	52	B4_GPIO182+	N4
L6	B4_GPIO208-	53	54	B4_GPIO182-	N5
	N.C.	55	56	N.C.	
K5	B4_GPIO209-	57	58	B4_GCLK/CLK_SW/SW_PLL0_OUT0 /GPIO239-	F1
K6	B4_GPIO209+	59	60	B4_GCLK/CLK_SW/SW_PLL0_OUT0 /GPIO239+	E1

Table 6 - JM3 Connector Pinout

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3.7 CLOCK GENERATION

The board has one multi-channel low jitter clock generation chip from Silabs Si5338A. It is used for different interfaces on the board. This IC can use crystal clock as reference or user clock from LSHM connector.

The clock distribution block diagram with default values and pinout is shown below

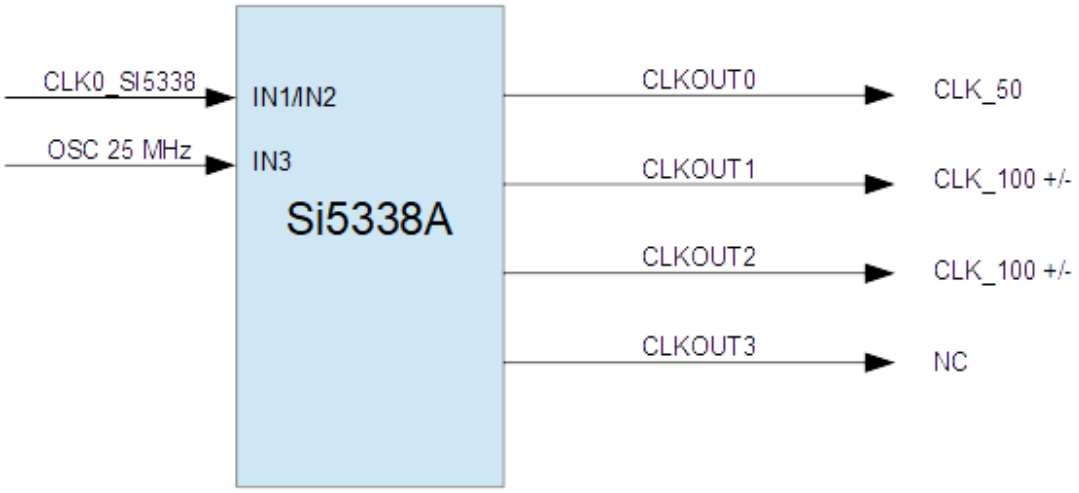

Figure 8 - SoM3 Clock Distribution Circuit

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Connections between Si5338A and SoM3 are listed below

MPF300T-1FCVG484E or connector		Schematic Net Name	Clock IC	
Pin Name	Ball Number		Pin number	Pin name
HSIO173PB0	Y1	SCL_1V8	12	SCL
HSIO172NB0, HSIO173NB0	U2, AA1	SDA_1V8	19	SDA
JM2	55	CLK0_SI5338+	1	IN1
	57	CLK0_SI5338-	2	IN2
25MHz ±10ppm from XO		CLK_REF	3	IN3
JM2	63	CLK_OUT2+	14	CLK2A
	61	CLK_OUT2-	13	CLK2B
XCVR_0A_REFCLK+	L19	XCVR_REFCLK_C+	18	CLK1A
XCVR_0A_REFCLK-	L20	XCVR_REFCLK_C-	17	CLK1B
CLKIN_N2/HSIO170PB0	AA2	CLK_REF0+	22	CLK0A

Table 7 - Si5338A to SoM3 Pinout

For the main and primary clocks, SI5338A-D-GM is used which is a 4 channel, multi frequency low jitter generator IC, configurable via I2C. It consists of 5 independent fractional dividers and 10 independent integer dividers for each output. This provides capability of 0.001ppb frequency tuning.

Note: The board comes programmed with default values as mentioned above. The clock chip can also be programmed with custom values after board start-up via I2C.

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4 BOARD SETUP AND CONFIGURATION

4.1 EMC2 CARRIER CARD

EMC2 is a single slot SoM carrier card in PCIe104 form factor. SoM3 module can be plugged into EMC2 as shown in figure 4 and in figure 7 it shows the carrier EMC2-DP with optional IO card and cable.

Figure 9 - EMC2-DP w. optional cable

The carrier card provides the input voltage and IO Voltage via the Samtec connectors. Please refer to section 3.4 for pinout. It also interfaces the transceivers and IO's to various features like FMC, Ethernet, USB, SATA, PCIe etc. More information can be found on EMC2-DP user guide. As current EMC2 was designed to host Trenz modules, it may have interfaces that may not be supported by SoM3 due to the Microchip FPGA limitations. Here is a list of features that may or may not work when SoM 3 is used on EMC2:

WARNING! VCCIO35 and VCCIO34 jumpers (JP8, JP7) can be only 1.8V or 2.5V, don't use 3.3V

Will work:

1. 1G Ethernet
2. JTAG(after relocating R36 to R54 On SoM-3, R48 on EMC must be in pull-up position)
3. FMC CLK_M2C lanes.
4. FMC LA lanes, LA26 has reverse polarity
5. Clocking
6. HDMI
7. RS-232
8. PCIe
9. SATA
10. FMC DP[0] lane with GBTCLK

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11. I2C with note(driver is Push-pull, not OD)
12. The SPI flash signals on SOM3 going to JM1 coincide with SD card on EMC2. So, EMC2 cannot access the FLASH on the SOM3. But older SD cards utilize the SPI interface and therefore, the old SD cards maybe accessible by the FPGA on SOM3.

so Old SD card, can be accesed by FPGA**Will not work**
USB

4.2 FPGA CONFIGURATION

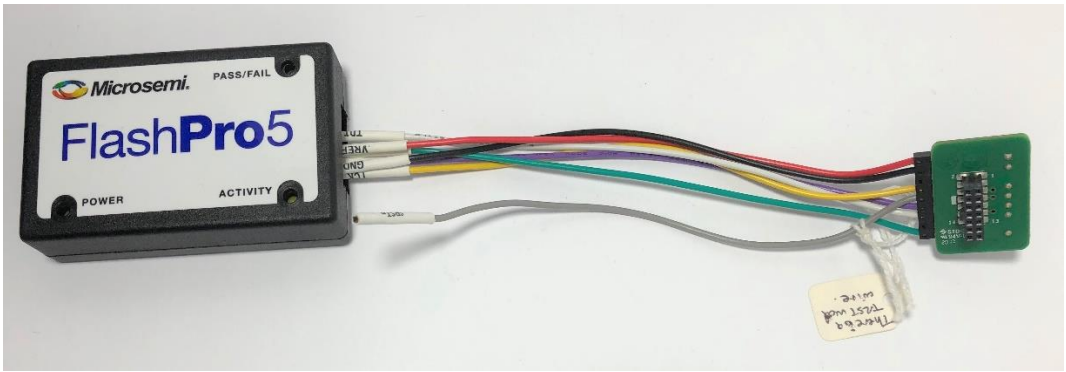
EMC2 carrier card provides JTAG interface to the SoM and it can be configured in three ways when connected to:

1. Using JTAG
2. Using eNVM
3. Using SPI Serial Flash

All the three interfaces can be accessed by FlashPro PolarFire v2.3 and later version of the Microsemi Libero design suite.

4.3 FLASHPRO5 WITH EMC2

The Flashpro5 JTAG POD from Microsemi has a 10-pin header whereas the EMC2 carrier card has a 14-pin header. Therefore, flying probes need to be used in order to connect FlashPro5 pod to EMC2 card as shown below



FlashPro5 pins are connected to a 14-pin adapter

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Note: Make sure TRST pin 8 is not connected.

Figure 10 - EMC2 with FlashPro5 JTAG POD

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Only 6 pins are connected between EMC2 JP1 header and FlashPro5 POD

VCC_JTAG, TMS, TCK, TDO, TDI and GND

EMC2 JP1 Header Pinout			
Signal	Pin No	Pin No	Signal
GND	1	2	VCC_JTAG
GND	3	4	TMS
GND	5	6	TCK
GND	7	8	TDO
GND	9	10	TDI
GND	11	12	-
GND	13	14	-

Table 8 - EMC2 JP1 Pinout

FlashPro5 Header Pinout			
Signal	Pin No	Pin No	Signal
TCK	1	2	GND
TDO	3	4	PROG_MODE
TMS	5	6	VCC_JTAG
VPUMP	7	8	TRST
TDI	9	10	GND

Table 9 - FlashPro5 Header Pinout

4.4 USING SOM3 ON TRENZ TE0701 CARRIER

SOM3 can be used on TE0701 and all features will work but not the followings:

1. HDMI
2. SD card

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5 BOARD SUPPORT PACKAGE

A Board support package is available for SoM3 which allows the user to see the board in Libero SoC PolarFire Design suite and select the interfaces available on board to use in block design. Please contact Sundance DSP Inc support for further information. The board support package also includes a PCIe interface driver and API for host communication to the FPGA via PCIe.

Microsemi Web site provides PCIe driver for Windows 10 and several demos for MPF FPGA series

https://www.microsemi.com/product-directory/fpgas/3854-polarfire-fpgas#documentation

Look under Demo Guides

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6 SAFETY

This module presents no hazard to the user

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7 EMC

This module is designed to operate from within an enclosed host system, which is built to provide EMC shielding. Operation within EU EMC guidelines is not guaranteed unless it is installed with an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host system to lockup or reboot.

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