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VF370 User Manual

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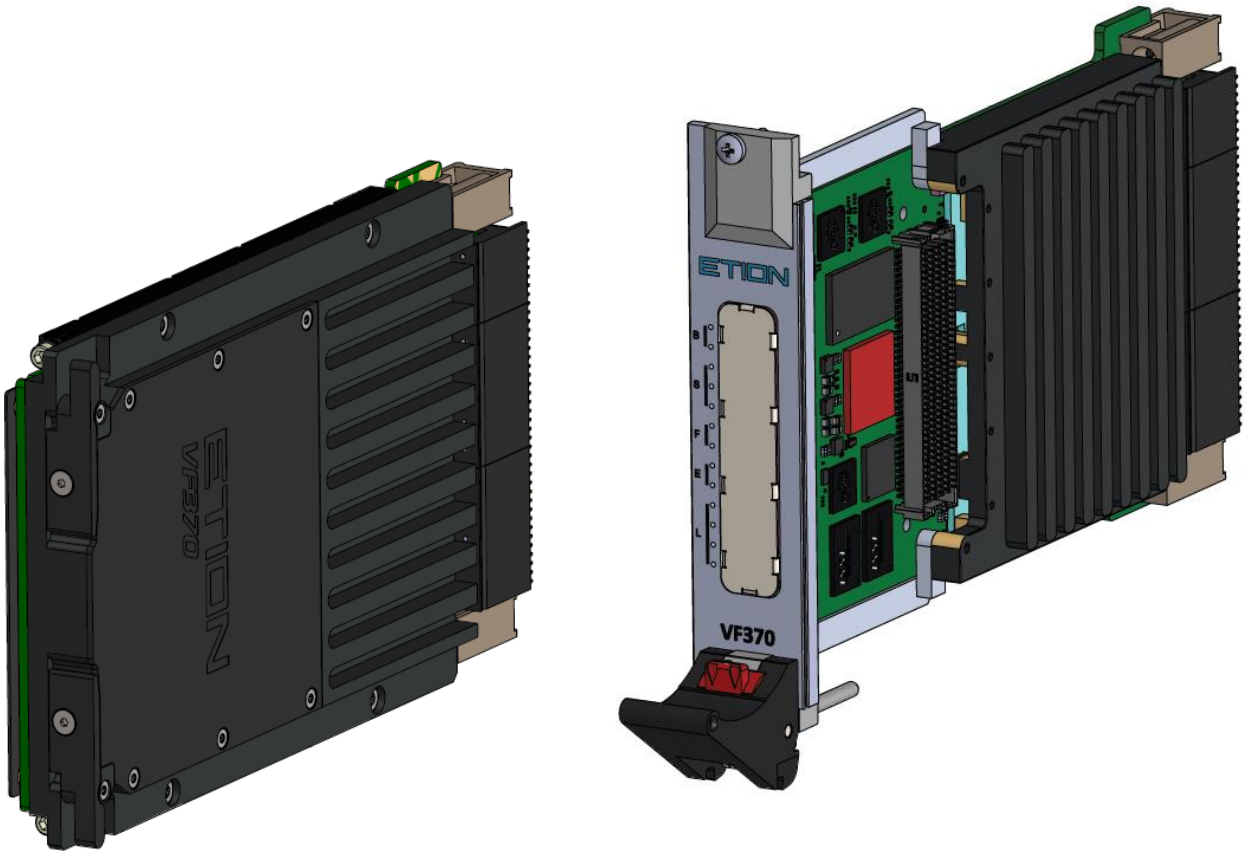
Rev. 01



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Revision History

Revision	Date	Changes
01	2019-11-26	First release of the VF370 User Manual

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About This Manual

This manual consists of information to simplify your installation, configuration and operation of the VF370 board. *About this Manual* describes the contents of each chapter and includes document conventions and technical support information

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Chapters Overview

About This Manual - This chapter provides an overview of the chapters, document conventions, and technical support information.

Chapter 1 Acronym List - This chapter expands abbreviations used in this manual.

Chapter 2 Introduction - This chapter provides a brief introduction to the VF370 3U FPGA and Intel Atom OpenVPX single board computer. It also provides a list of reference documents whose information supplements this user manual.

Chapter 3 Product Overview - This chapter provides detailed functional information for the VF370.

Chapter 4 Specifications - This chapter provides the specifications for the functional areas of the VF370.

Chapter 5 Installation and Setup - This chapter includes instructions for unpacking and installing the VF370.

Chapter 6 Operating Guide - This chapter provides information on proper operation of the VF370.

Chapter 7 BIOS - This chapter describes the VF370 BIOS settings.

Document Conventions

The following icons are used in this manual to emphasize setup or system information:

Icon	Use
	Alerts you to the important details regarding the setup and maintenance of your system.
	Alerts you to potential damage to the board during system setup and installation.

Technical Support

Should you require additional technical information or assistance, contact Etion Create (Pty) Ltd:

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1 Acronym List

AC	Air cooled
API	Application Programming interface
ATA	Advanced Technology Attachment
AUX	Auxiliary
BMP	Board Management Processor
BSP	Board Support Package
CBIT	Continuous BIT
CC	Conduction Cooled
CLK	Clock
CML	Current Mode logic
CPU	Central Processing Unit
DDR	Double Data Rate
DMA	Direct Memory Access
ECC	Error Correcting Code
EP	Endpoint
ESD	Electrostatic Discharge
ETH	Ethernet
FDK	FPGA Firmware Development Kit
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
GND	Ground
GUI	Graphical User Interface
I2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
KB	Kilo Byte(s)

LED	Light Emitting Diode
MB	Mega Byte(s)
Mb	Mega Bit(s)
MLC	Multi-level Cell
MT/s	Mega Transfers per second
NTB	Non-Transparent Bridge
OS	Operating System
PBIT	Power-up BIT
PCA	Printed Circuit Assembly
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PHY	Physical interface
PSU	Power supply
RAM	Random Access Memory
RTC	Real Time Clock
RTM	Rear Transition Module
SATA	Serial ATA
SBC	Single-board Computer
SFP	Small form-factor pluggable
SOC	System On Chip
SPI	Serial Peripheral Interface
SSD	Solid State Drive
SSH	Secure-Shell
TDP	Thermal Design Power
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus

2 Introduction

This chapter provides a brief introduction to the VF370 3U FPGA and Intel Atom OpenVPX single board computer. It also provides a list of reference documents whose information supplements this user manual.

2.1 The VF370 OpenVPX SBC

The VF370 is a 3U OpenVPX module that leverages on Intel APL-I E3900 series processors and Intel Cyclone® V FPGA technology to provide a single board computer (SBC) ideally suited for VPX system controller and general computing tasks typically required by VPX systems. Refer to the functional block diagram in Figure 1.

The on-board Intel Atom E3900 SoC is a highly integrated low power processor providing features such as memory controller, 4k graphics capability and high definition audio interface amongst others. (Refer to [3] for more information). Dual- or quad-core CPUs with three different speed grades are available depending on the build option selected. The processor is connected to an FPGA and to the backplane and through one 4 lane (x4) two 4 lane PCIe interfaces respectively. The APL-I E3900 series processor is hereafter referred to as the Processor.

The VF370 provides 4GB of DDR3 Processor memory with ECC, onboard 32GB SSD mass storage and two 1Gbps network interfaces. Other build options for onboard mass storage is available.

The VF370 uses an Intel Cyclone® V GX/GT FPGA device to implement a high-speed processing node. The FPGA is available to the user for custom firmware development. Depending on the FPGA resources and interface bandwidth required, one of four different FPGAs from the Cyclone® V GX and GT families can be populated on the VF370.

The Cyclone® V FPGA has one bank of dedicated DDR3 memory.

The VF370 FMC carrier card, combined with a variety of FMC cards, provides a modular solution that accommodates a wide range of I/O requirements. High-speed FPGA serial interfaces to the FMC site creates abundant FPGA IO throughput. FMC front panel IO's can optionally be routed to the P2 VPX connector for FMC backplane I/O.

This is accomplished by routing FMC User I/O signals to a custom FMC IO connector, which loops these signals back to the VF370 module and routes it to the P2 backplane connector. The FMC User IO's can then be accessed through the P2 backplane interface of the VF370.

The VF370 conforms to the OpenVPX standard as a Payload module with System Controller capability. Both air-cooled and conduction cooled versions are available.

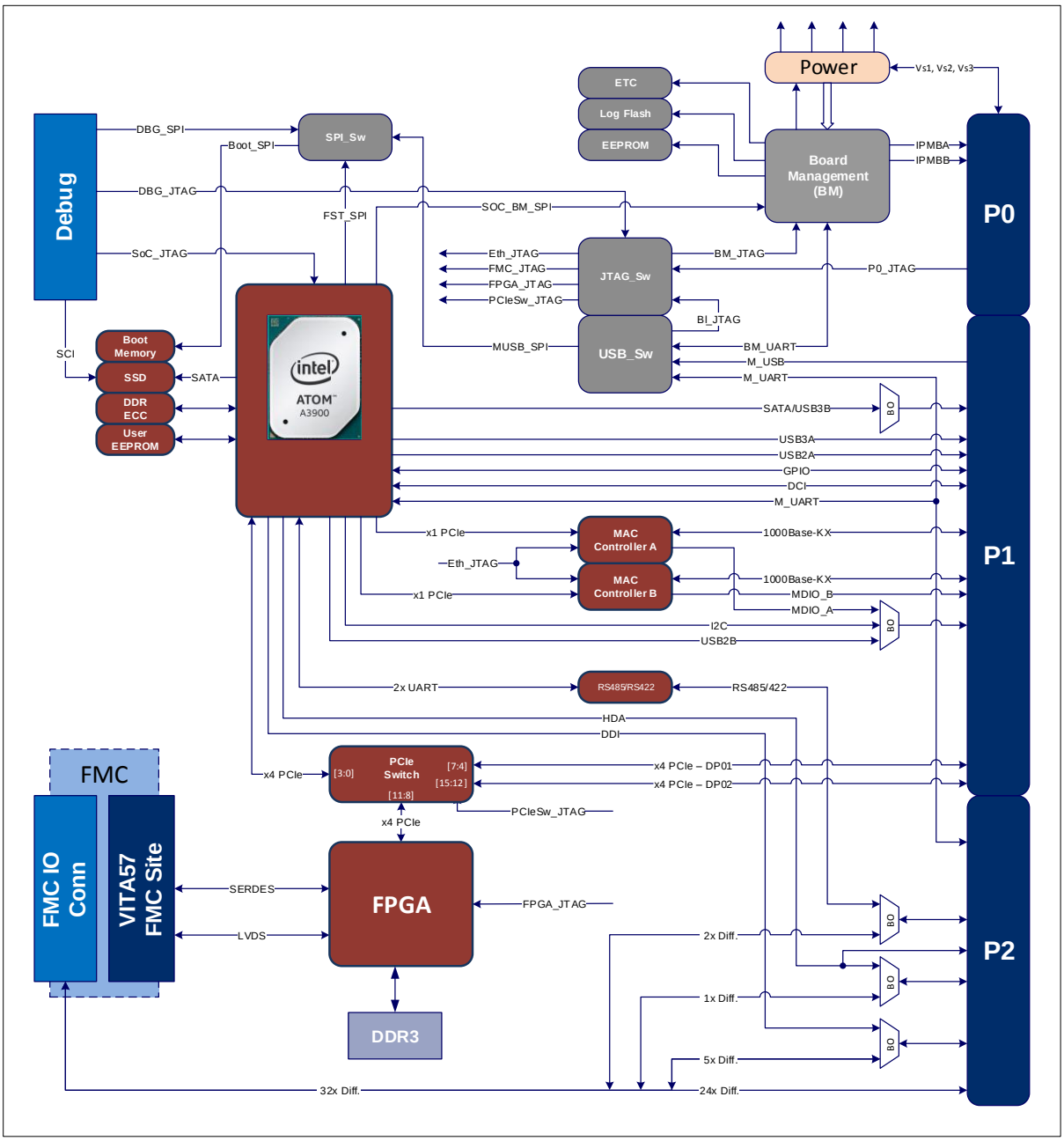

Figure 1: VF370 Functional Block Diagram.

2.2 Features

- **Processor**
  - CPU cores: Two/four cores @ 1.3GHz or 1.6GHz base frequency respectively (up-to 2GHz burst)
  - Intel HD graphics supporting 4096x2160 resolution @ 60Hz
  - Single-channel 4GB DDR3 @ 1333MT/s with ECC
  - On board SATA SSD (32 GB standard build option)

- High speed FPGA processing with Intel Cyclone® V GX/GT FPGA
  - GX Device variants: 5CGXD7, 5CGXD9
  - GT Device variants: 5CGTD7, 5CGTD9
  - Embedded device memory: 4.4 - 12.2 Mb
  - Embedded device multipliers (18x18): 300 – 684
  - The Processor and FPGA are connected through a PCIe (x4) interface

- **FPGA external DDR memory**
  - Single bank of 2GB DDR3 @ up to 666MT/s (arranged as 256M x 32-bit)

- **VPX Interface**

  Comply with OpenVPX MOD3-PAY-2F2U-16.2.3-3 module profile
  - PCIe Gen2 Data plane (2x Fat Pipes)
  - GigE Control plane 1000BASE-BX/KX or external PHY (2x Ultra-Thin Pipes)
  - Payload module with System Controller capability

  Supports FMC User I/O on P2
  - This feature is only available through the FMC I/O connector

- **VITA 57 FPGA MEZZANINE CARD (FMC) site**
  - 4x High-Speed Serial Interface (HSSI) lanes
  - 58x Differential LVDS interfaces on LA and HA

- Custom FMC I/O connector for backplane I/O from FMC

❖ **FPGA configuration**

The FPGA supports the following configuration options:

- Automatic configuration after power-up from on-board non-volatile storage
- Configuration through JTAG (M_USB)
- Configuration through the Processor
  Note: This is not currently supported in the API

❖ **Software & Firmware support**

Linux distribution and BSP (Board support package)

- User API and example application
- API Reference Manual
- PCIe driver for FPGA with DMA support
- Example application showing FPGA memory access and DMA

Contact us for information regarding the FPGA Firmware Development Kit (FDK).

Custom application/driver software and FPGA firmware development is available on request.

❖ **Companion Module(s)**

VR307 Rear Transition Module (RTM)

2.3 Product Applications

The VF370 is targeted at applications requiring the following:

- 3U VPX compatible single board computer
- High-performance low-power Intel X86 multi-core Processing
- FPGA processor for custom firmware applications and co-processing

2.4 Reference Documents

The following sources provide important reference information that may provide useful input for achieving optimal operation of the VF370:

[1] VF370 API Reference Manual

[2] VF370 Firmware Reference Manual (part of the FDK)

[3] https://www.intel.com/content/www/us/en/embedded/products/apollo-lake/overview.html

3 Product Overview

This chapter provides detailed functional information for the VF370.

3.1 Overview of the VF370

Figure 1 shows a functional block diagram of the VF370 with I/O build option configurations.

- The Board Management function controls the power sequencing, reset signals and health monitoring.
- The Processor boots into the Linux kernel and, through its non-transparent (NTB) PCIe bridge, allows multi-master communication with other VPX slots if required. The NTB option is enabled/disabled in the BIOS.
- The FPGA boots from on-board non-volatile memory.
- The JTAG_-, SPI_- and USB_Switch functions respectively control JTAG access, boot flash programming and routing of maintenance USB/UART interfaces.

3.2 Board Management

The VF370 board management controller (BM), a MAX10 device from Intel, performs the following functions:

- Start-up and PBIT
    - Monitors external power supplies (VS1=12V, VS2=3.3V and VS3=5V) for correct levels
    - Enables local power supplies
    - Performs reset actions (nSYSRESET and local resets)
    - Check critical board temperatures:
        - PCIe Switch, FPGA, FPGA Core supply, FMC temperature
- CBIT: Continuously monitors external voltages, local voltages, currents and temperatures
    - Makes available voltages, temperatures and other information to the Processor Linux host through the API via the SOC_BM_SPI interface.
    - Log PBIT and CBIT events in non-volatile memory.
- Shut-down the VF370 if any power supply or device temperature is out of its critical limits. Refer to Table 1 for voltage and temperature warning can critical limits and to for the temperature sensor locations.

Table 1: Voltage and temperature limits

Description	Critical Minimum	Warning Minimum	Warning Maximum	Critical Maximum
VS1	10.5V	11.0V	12.6V	12.8V
VS2	3.0V	3.15V	3.45V	3.5V
VS3	4.6V	4.75V	5.2V	5.4V
SoC DDR temperature (T1, bottom side)			90°C	100°C
PCIe switch temperature (T2)			100°C	115°C
FPGA temperature (T3)			90°C	100°C
VF370 temperature (T4)			90°C	100°C
FPGA core supply temperature (T5)			90°C	100°C
FMC site temperature (T6)			90°C	100°C
BM die temperature (T7)			100°C	110°C
PMIC die temperature (T8)			100°C	115°C

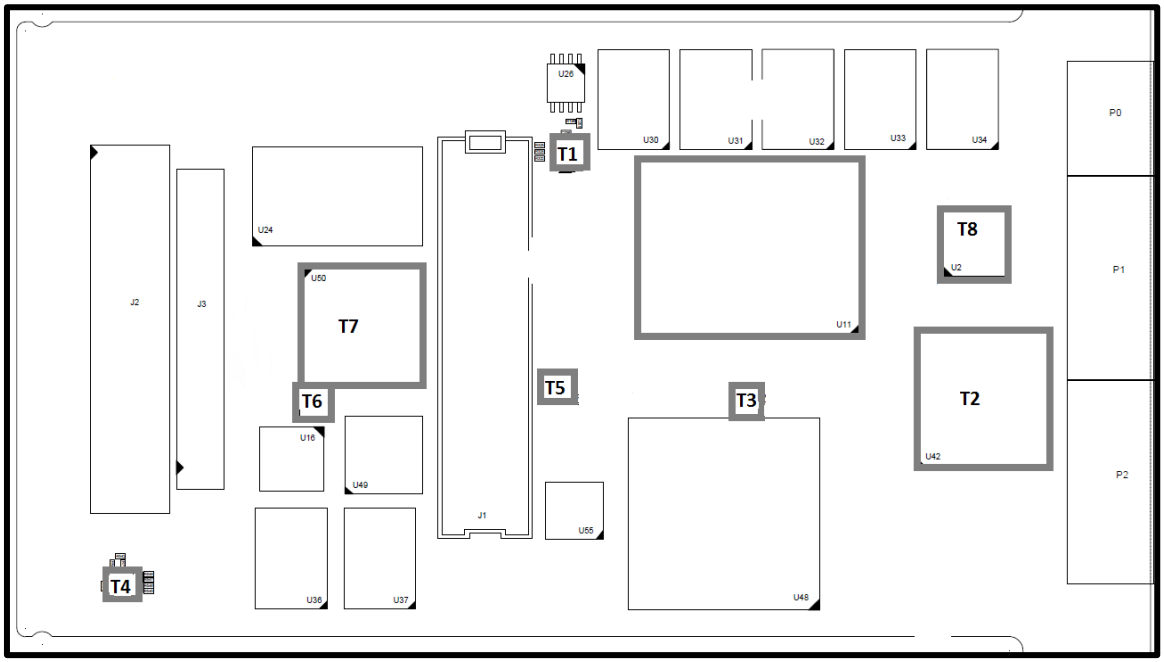

Figure 2: BM Temperature sensor locations

3.3 VPX Interface

The VF370 complies with the 3U OpenVPX slot profile SLT3-PAY-2F2U-14.2.3 as shown in Figure 3.

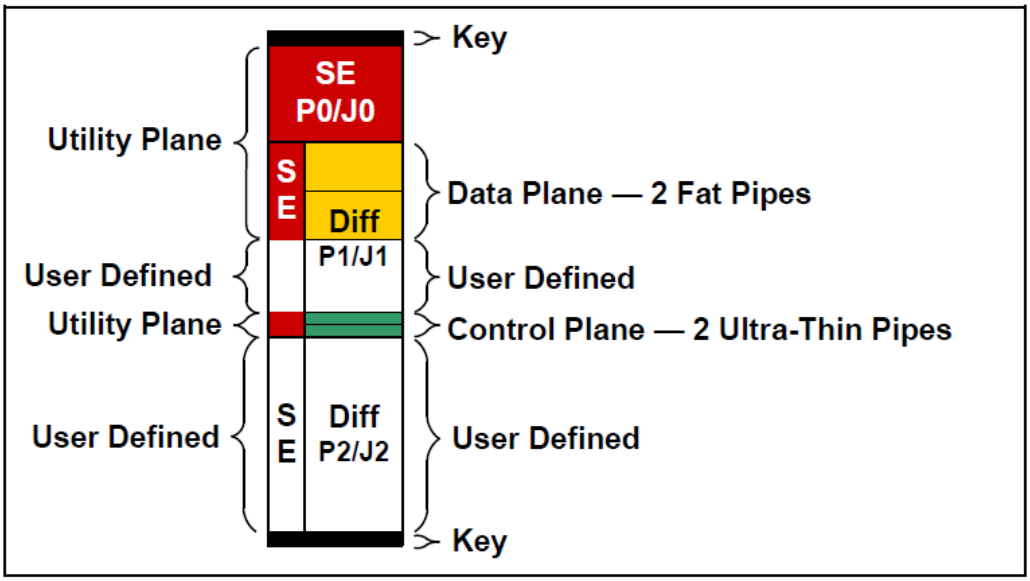

Figure 3: VF370 Slot Profile

The VF370 standard module profile (**MOD3-PAY-2F2U-16.2.3-3**) provides the following VPX interfaces:

- P0 as per ANSI/VITA65 OpenVPX
- Two PCIe **Gen2** Data plane Fat Pipes (4X) on DP01and DP02
  MOD3-PAY-2F2U-16.2.3-3 also supports PCIe **Gen1** on the Data plane
  - The following additional Data plane options are available in the BIOS:
    - DP01 (x4 PCIe) and DP02 to DP05 (four x1 PCIe)
    - DP01 to DP08 (eight x1 PCIe)
- Two GigE 1000BASE-BX/KX Control plane Ultra-Thin Pipes on CPutp01 to CPutp02 with external PHY option for CPutp02.
- P1 and P2 User Defined I/O connections are customisable through build options. The default build option is:
    - SATA interface
    - User I2C interface (single-master only, multi-master **not** supported)
      Note: 100 kHz, 400 kHz, 1 MHz and 3.1 MHz clock rates supported by the processor
    - RS422 or RS485 (selectable in the BIOS)
      Note: Functionality based on the 16550 and 16750 industry standard UART
    - High Definition Audio interface
    - Display port interface
    - 24 differential FMC User IOs

The following three figures show the VF370 VPX connector pin assignments.

Plug-in module P0	G	F	E	D	C	B	A
1	+12V_D	+12V_D	+12V_D	No Pad	+3.3V_D	+3.3V_D	+3.3V_D
2	+12V_D	+12V_D	+12V_D	No Pad	+3.3V_D	+3.3V_D	+3.3V_D
3	+5V_D	+5V_D	+5V_D	No Pad	+5V_D	+5V_D	+5V_D
4	IPMBB_SCL	IPMBB_SDA	GND	NC (-12V Aux)	GND	nSYSRESET	NVMRO PROG_ID[2]
5	nGAP	nGA4	GND	+3.3V_Aux	GND	IPMBA_SCL	IPMBA_SDA
6	nGA3	nGA2	GND	+12V_Aux	GND	nGA1	nGA0
7	TCK	GND	TDO	TDI	GND	TMS	nTRST
8	GND	REF_CLK-	REF_CLK+	GND	AUX_CLK-	AUX_CLK+	GND

Figure 4: VPX P0 pin assignments

Plug-in module P1				G	F	E	D	C	B	A
1	Data Plane Port 1	8 X1	1 X4	GDiscrete1 PROG_ID1	GND	DP01-TD0-	DP01-TD0+	GND	DP01-RD0-	DP01-RD0+
2				GND	DP01-TD1-	DP01-TD1+	GND	DP01-RD1-	DP01-RD1+	GND
3				P1-VBAT	GND	DP01-TD2-	DP01-TD2+	GND	DP01-RD2-	DP01-RD2+
4				GND	DP01-TD3-	DP01-TD3+	GND	DP01-RD3-	DP01-RD3+	GND
5	Data Plane Port 2		1 X4 / 4 X1	nSYS_CON	GND	DP02-TD0-	DP02-TD0+	GND	DP02-RD0-	DP02-RD0+
6				GND	DP02-TD1-	DP02-TD1+	GND	DP02-RD1-	DP02-RD1+	GND
7				Reserved P1-REF_CLK-SE	GND	DP02-TD2-	DP02-TD2+	GND	DP02-RD2-	DP02-RD2+
8				GND	DP02-TD3-	DP02-TD3+	GND	DP02-RD3-	DP02-RD3+	GND
9	User Defined			GPIO4/ USBB_Pwr	GND	SATA-TD-/ USB3B-TD-	SATA-TD+/ USB3B-TD+	GND	SATA-RD-/ USB3B-RD-	SATA-RD+/ USB3B-RD+
10				GND	USB3A-TD-	USB3A-TD+	GND	USB3A-RD-	USB3A-RD+	GND
11				USBA_Pwr	GND	I2C_SCL/ MDCLK1/ USB2B-	I2C_SDA/ MDIO1/ USB2B+	GND	USB2A-	USB2A+
12				GND	DCI-TD-	DCI-TD+	GND	DCI-RD-	DCI-RD+	GND
13				M_USB_Vbus	GND	MDCLK2	MDIO2	GND	M_USB-	M_USB+
14				4	GPIO3 (SPI_CLK)	GPIO2 (SPI_nCS)	GND	GPIO1 (SPI_DO)	GPIO0 (SPI_DI)	GND
15	Control Plane			nMaskable_Reset	GND	Cputp02-TD-	Cputp02-TD+	GND	Cputp02-RD-	Cputp02-RD+
16				GND	CPutp01-TD-	CPutp01-TD+	GND	CPutp01-RD-	CPutp01-RD+	GND

Figure 5: VPX P1 pin assignments

Note: Signals with two or more functions are selectable through build options. The first function described is the default option. For example, pin E9 is SATA-TD- by default, but can be changed to USB3B-TD- through a build option.

Plug-in module P2		G	F	E	D	C	B	A
1	User Def.	HDA_nRST	GND	DDI1-/ FMC_DP30-	DDI1+/ FMC_DP30+	GND	DDI0-/ FMC_DP31-	DDI0+/ FMC_DP31+
2		GND	DDI3-/ FMC_DP28-	DDI3+/ FMC_DP28+	GND	DDI2-/ FMC_DP29-	DDI2+/ FMC_DP29+	GND
3		HDA_BCLK	GND	HDA_SDO/ FMC_DP26-	HDA_SDI/ FMC_DP26+	GND	DDI_Aux-/ DDI_DDC_SDA/ FMC_DP27-	DDI_Aux+/ DDI_DDC_SCL/ FMC_DP27+
4		GND	RS485B- RS422-TD-/ FMC_DP24-	RS485B+ RS422-TD+/ FMC_DP24+	GND	RS485A- RS422-RD-/ FMC_DP25-	RS485A+ RS422-RD+/ FMC_DP25+	GND
5		HDA_SYNC	GND	FMC_DP22-	FMC_DP22+	GND	FMC_DP23-	FMC_DP23+
6		GND	FMC_DP20-	FMC_DP20+	GND	FMC_DP21-	FMC_DP21+	GND
7		CPLD_JTAGEN	GND	FMC_DP18-	FMC_DP18+	GND	FMC_DP19-	FMC_DP19+
8		GND	FMC_DP16-	FMC_DP16+	GND	FMC_DP17-	FMC_DP17+	GND
9		nPROG_Sel	GND	FMC_DP14-	FMC_DP14+	GND	FMC_DP15-	FMC_DP15+
10		GND	FMC_DP12-	FMC_DP12+	GND	FMC_DP13-	FMC_DP13+	GND
11		M_UART_TX	GND	FMC_DP10-	FMC_DP10+	GND	FMC_DP11-	FMC_DP11+
12		GND	FMC_DP8-	FMC_DP8+	GND	FMC_DP9-	FMC_DP9+	GND
13		PROG_ID0 M_UART_RX	GND	FMC_DP6-	FMC_DP6+	GND	FMC_DP7-	FMC_DP7+
14		GND	FMC_DP4-	FMC_DP4+	GND	FMC_DP5-	FMC_DP5+	GND
15		DDI_HPD	GND	FMC_DP2-	FMC_DP2+	GND	FMC_DP3-	FMC_DP3+
16		GND	FMC_DP0-	FMC_DP0+	GND	FMC_DP1-	FMC_DP1+	GND

Figure 6: VPX P2 pin assignments

Note: Signals with two or more functions are selectable through build options. The first function described is the default option.

- M_UART_TX/RX are the maintenance UART signals. During power-up this interface initially displays the boot-up information from the board management processor. As soon as the Processor start-up sequences succeeded, the M_UART interface switches over to the Processor maintenance UART interface to display boot information and provide access to the BIOS by pressing “2” during boot-up.

- To access the FMC_DPx signals through P2, an FMC with an FMC IO connector is required.

3.4 Processor interfaces

The Processor power and reset de-assertion are controlled by the board management processor. Default BSP is based on Linux operating system and provides support for the following features either through the OS or the API:

- On board SATA SSD (Gen1 1.5 Gbps)
- On board user EEPROM (512Kb) - (API)
- Module health information (from BM) - (API)
- User GPIO control - (API)
- User I2C interface - (OS)
- RS485/422 interfaces selectable in BIOS - (OS)
- External SATA interface – (OS)
- External USB3 interface – (OS)
- 1000Base-BX/KX and external PHY (default on CPutp02) Ethernet support – (OS)
- PCIe Switch interfaces (Up-to Gen2) – (OS)
    - x4 PCIe from Processor to the PCIe Switch
    - x4 PCIe from PCI Switch to the FPGA through the PCIe switch
    - The PCIe Switch backplane interfaces can be repartitioned through the BIOS as follows:
        - DP01 (x4 PCIe) and DP02 (x4 PCIe)
        - DP01 (x4 PCIe) and DP02 to DP05 (four x1 PCIe)
        - DP01 to DP08 (eight x1 PCIe)
    - NTB on either DP01 or D02 selectable through the BIOS

3.4.1 Processor interface/pin mappings

The table below lists the Processor interface/pin mappings for applicable user interfaces, amongst others GPIO, I2C, UARTS etc.

Table 2: Processor pin mappings

Interface	Processor pin mapping	Description
I2C_SCL	LPSS_I2C0_SCL	User I2C
I2C_SDA	LPSS_I2C0_SDA	
RS422/485B_TX	LPSS_UART0_TX	RS422 / RS485-B
RS422/485B_RX	LPSS_UART0_RX	
RS485A_TX	LPSS_UART1_TX	RS485-A
RS485A_RX	LPSS_UART1_RX	
M_UART_TX	LPSS_UART2_TX	Maintenance UART
M_UART_RX	LPSS_UART2_RX	
AuxCLK Out	GPIO_27	AUX Clock
AuxCLK In	GPIO_183	
GDiscrete1 Out	GPIO_0	GDiscrete1
GDiscrete1 In	GPIO_1	
SOC_FPGA_GPIO[3]	GPIO_160	SoC <=> FPGA GPIOs
SOC_FPGA_GPIO[2]	GPIO_159	
SOC_FPGA_GPIO[1]	GPIO_158	
SOC_FPGA_GPIO[0]	GPIO_157	

3.5 FPGA Interfaces

The following main FPGA interfaces are shown in Figure 7:

- **PCIe interface**
  The FPGA is connected to the Processor through a high speed x4 PCIe interface via the Gen2 PCIe Switch (GXB_L0 bank). PCIe link speed is determined by FPGA build option (GX = Gen1, GT = GEN2). The FPGA is also accessible through the backplane PCI interfaces (DP01 and DP02).

- **DDR3 interface**
  One bank of 2GB DDR3 RAM @ up to 666MT/s (arranged as 256M x 32-bit) is connected to FPGA banks 8A and 7A.

- **Miscellaneous interfaces**
  The FPGA optionally connects to the Processor through 4x GPIOs.

- **FMC interface**
  This interface is described in more detail in the following section.

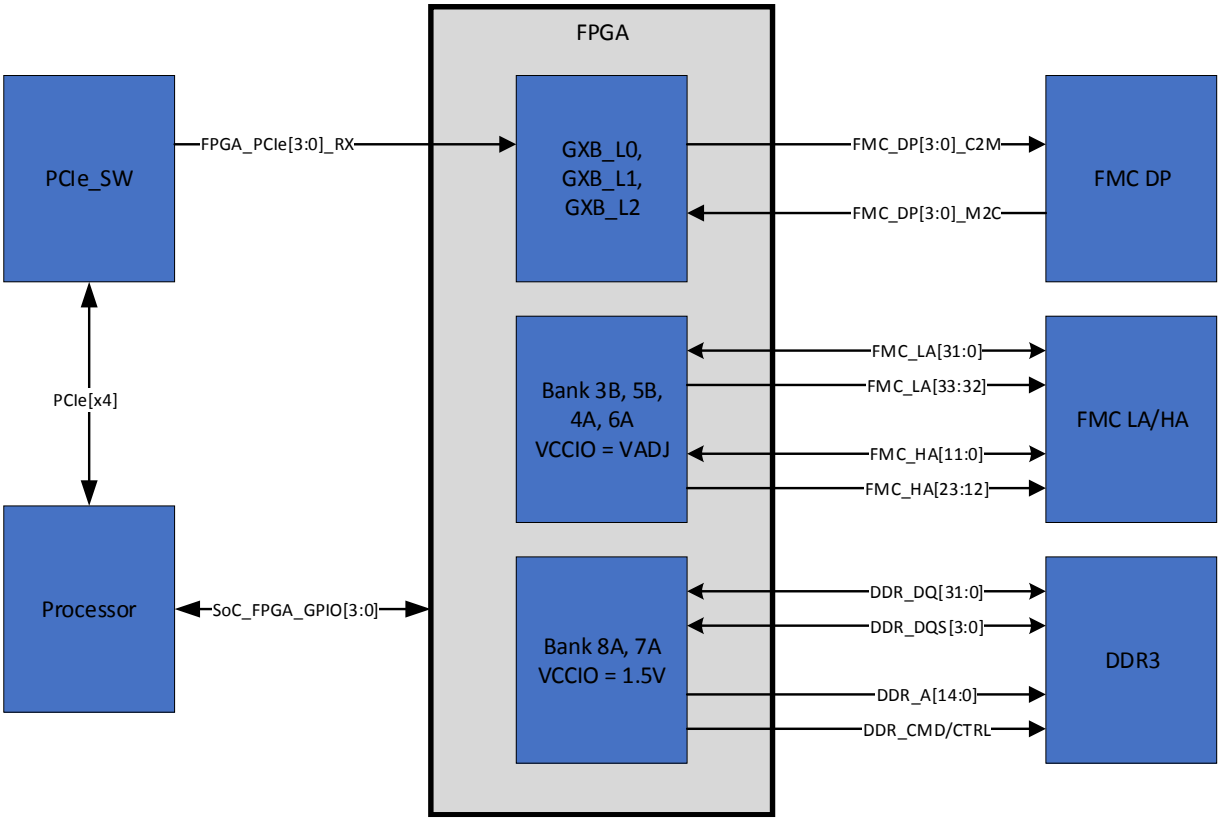

Figure 7: VF370 FPGA signals

3.5.1 FPGA FMC Interface

- FMC LA and HA busses are connected to banks 3B, 5B, 4A and 6A and supports the following:

Signal Name	LVDS	LVCMOS/LVTTL
FMC_LA[31..0]	Bidirectional	Bidirectional
FMC_LA[33,32]	TX only	Bidirectional
FMC_HA[11..0]	Bidirectional (Emulated LVDS)	Bidirectional
FMC_HA[23..12]	TX only	Bidirectional

- FMC multi-Gig signals are connected to FPGA GXB_L1 and GXB_L2 banks and support:

The **maximum input voltage** on FPGA signals from the FMC is **3.3V**.

Descriptions of the FPGA FMC signals are shown in Table 3.

Table 3: VF370 FPGA FMC signals

Signal	FPGA Pins	I/O Standard	Description
LA[00..33]p LA[00..33]n	2x 68	LVCMOS or LVDS	Differential pairs or single-ended signals to/from FPGA
HA[00..23]p HA[00..23]n	2x 48	LVCMOS or LVDS	Differential pairs or single-ended signals to/from FPGA
CLK[0..1]_M2Cp,n	4	LVDS	Two Differential Clocks from FMC to FPGA
CLK[2..3]_BIDIRp,n	4	LVDS	Two Bidirectional differential clocks between FMC and FPGA
CLK_DIR	1	2.5V	Direction signal for CLK[2..3]_BIDIR
GBTCLK[0..1]_M2C	4	CML / LVDS	FPGA Reference clock inputs for FMC transceiver signals DP[0..9]
DP[0..3]_M2C	8	CML	4x HSSI transceiver inputs on FPGA
DP[0..3]_C2M	8	CML	4x HSSI transceiver outputs on FPGA

Note that the FMC_LA[] and FMC_HA[] signals connect to LVDS transmitter (Tx) and LVDS receiver (Rx) pins on the FPGA, since the FPGA LVDS pins are uni-directional.

3.5.2 VF370 FPGA Configuration

The VF370 FPGA can be configured through the following devices/interfaces:

- Active serial configuration through 256Mb onboard flash.
    - The onboard configuration flash can be programmed by the Processor through the API. (currently not supported)
- Passive serial configuration controlled by the Processor.
- FPGA configuration and configuration flash programming via JTAG.

3.5.3 VF370 FPGA Clock distribution

The following diagram shows the available clocks connected to the FPGA:

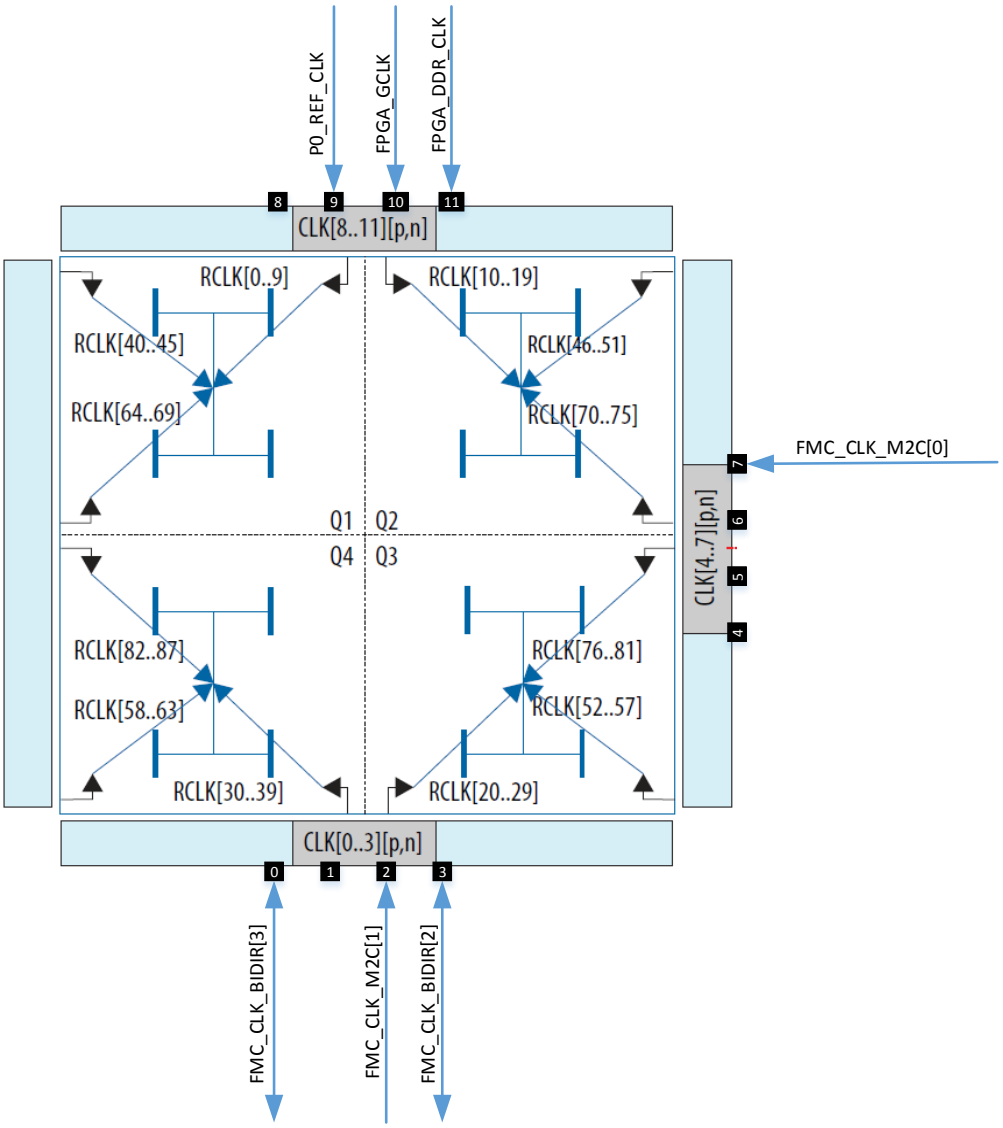

Figure 8: FPGA clock inputs

The sources of the FPGA clocks are discussed in following section.

3.6 VF370 Clock Structure

The following diagram shows an overview of the VF370 clock structure related to the FPGA and VPX clocks.

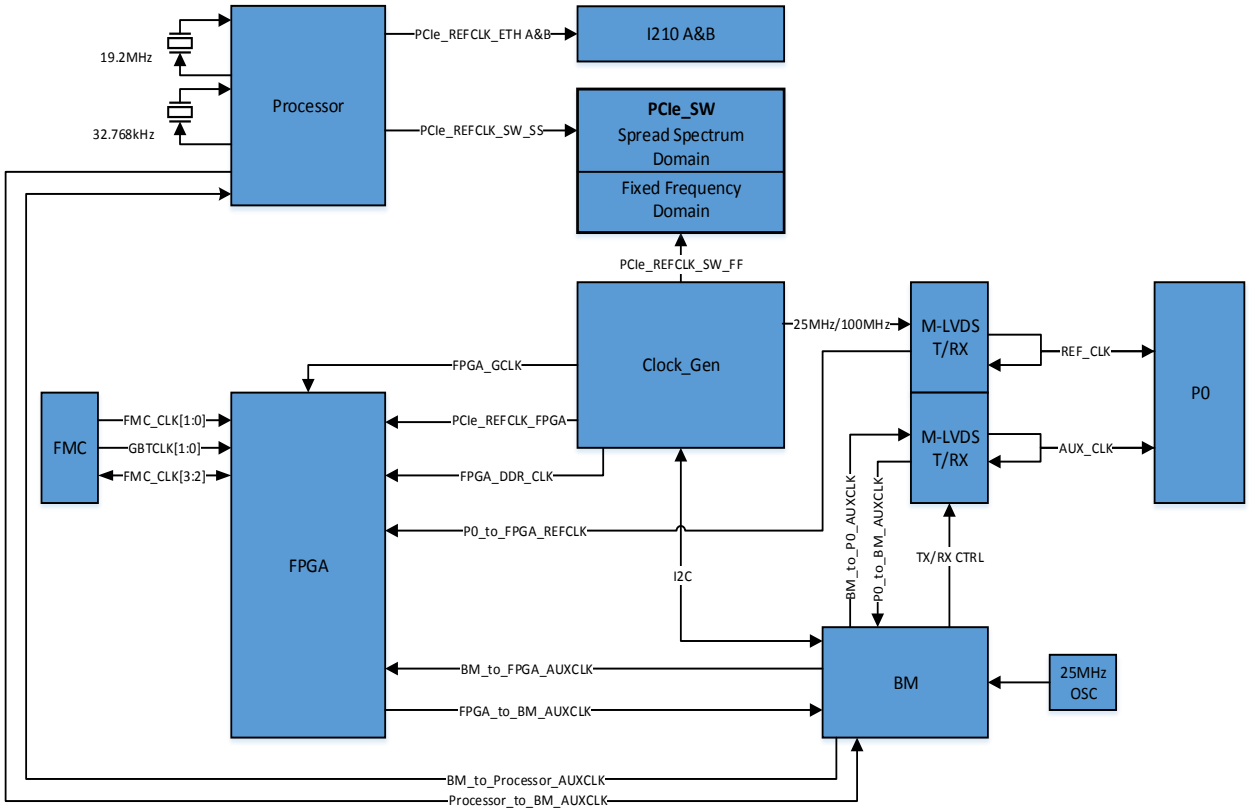

Figure 9: VF370 clock structure

The Processor generates required clocks from two dedicated oscillators

- 19.2MHz main clock
- 32.768KHz RTC clock

The following table gives a description of the clocks shown in Figure 9:

Table 4: VF370 clock description

Clock Name	Clock Description	Clock Frequency	IO Standard
VPX REF_CLK	VPX Reference clock as described in VITA65.0. This clock can be driven or received by the VF370 SBC.	25MHz Default 100MHz Alternate	M-LVDS
VPX AUX_CLK	VPX Auxiliary clock as described in VITA65.0	User dependant	LVCMOS

Clock Name	Clock Description	Clock Frequency	IO Standard
PCIe_REFCLK_ETHA/B	Ethernet PCIe reference clocks generated by the Processor	100MHz	
PCIe_REFCLK_SW_FF	Fixed Frequency PCIe reference clock to PCIe Switch	100MHz	
PCIe_REFCLK_SW_SS	Spread Spectrum PCIe reference clock to PCIe Switch, generated by the Processor	100MHz	LP_HCSL
FPGA_GCLK	Global clock source for use with FPGA	100MHz	LP_HCSL
FPGA_DDR_CLK	FPGA DDR reference clock	50MHz	LVDS
FMC_CLK[1:0]	Differential clocks signals driven by mezzanine module to FPGA	FMC dependant	LVDS
FMC_CLK[3:2]	Differential bidirectional clock signals. The direction of these clocks are determined by the CLK_DIR signal	FMC/FPGA dependant	LVDS
GBTCLK[1:0]	Reference clock signals for FMC_DP data signals	FMC dependant	LVDS

The PCIe Switch isolates the spread spectrum clock domain generated by the Processor from the fixed frequency clock domain used for backplane and FPGA PCIe interfaces.

3.7 Development and test interfaces

The VF370 provides access to typical development and test interfaces through the **VR307** Rear Transition Module (RTM).

3.7.1 VR307

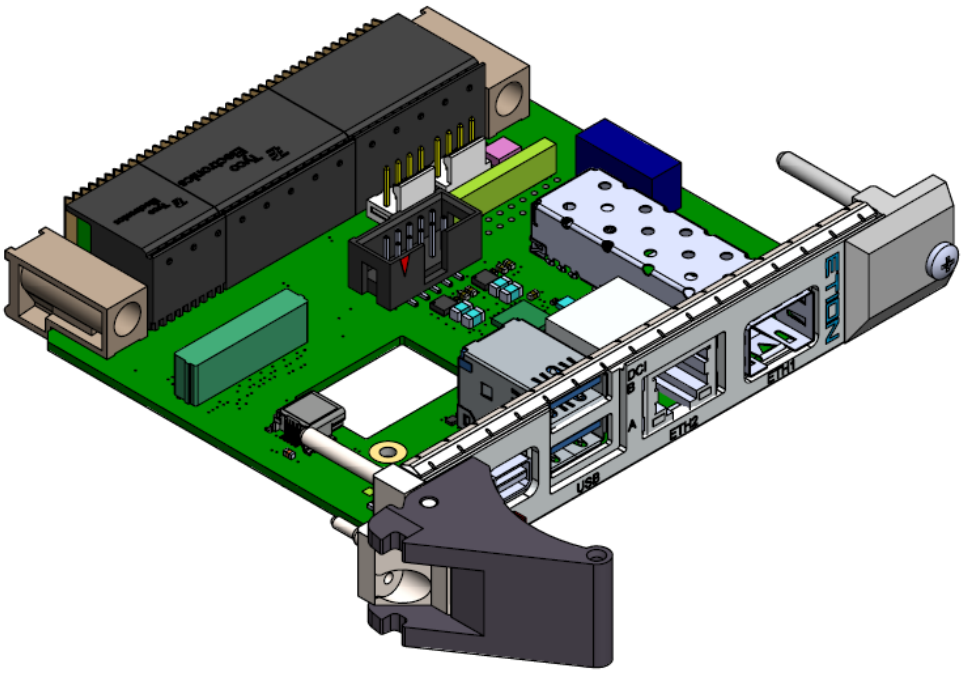

Figure 10: VR307 RTM

The VR307 (shown in Figure 10) is an RTM designed specifically for the VF370 SBC. It can be used during development, testing and integration of VF370 based systems. The following VF370 interfaces are available through the VR307:

- Display port interface through mini Display Port connector
- USB3 host interface(s)
- RJ45 Ethernet interface on CPutp02
- SFP Ethernet interface on CPutp01
- Mini USB 2.0 device interface (M_USB) providing access to BM UART, Processor UART, BM JTAG or FPGA JTAG (depending on DIP switch selection) and boot memory (SPI)
- External SATA interface with power connector
- P0 JTAG interface (typically only used for board bring-up and maintenance purposes)
- Header (10x2) with GPIO and User I2C interfaces
- High-density connector with FMC backplane IO, RS422 and HD Audio interfaces

- DIP Switch-3 is used to enable different JTAG programming modes (SW3):

Table 5: DIP Switch-3 settings

State Description	SW3
Normal Operation	Figure 11
FPGA programming and signal tap from on-board Arrow Blaster	Figure 12
BM programming and signal tap from on-board Arrow Blaster	Figure 13

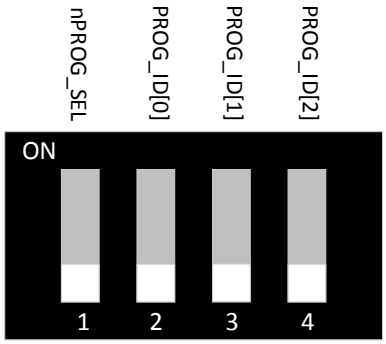

Figure 11: SW3 setting for normal operation

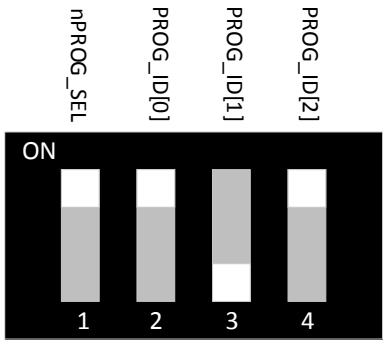

Figure 12: SW3 setting for FPGA programming and debugging

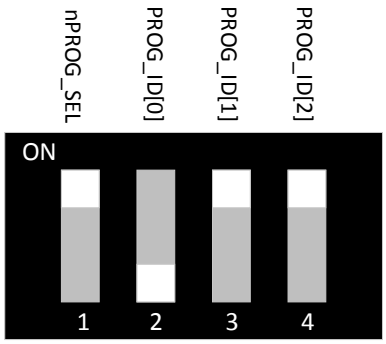

Figure 13: SW3 setting for BM programming

- **Note** – SW4 on the RTM should always be set to all off.
- SW1 and SW2 provides push buttons for testing the nSYSRESET and nMaskable_Reset functionality respectively.

Table 6: J9 – SATA Power connector

Pin #	Description 02360-01	Description 02360-02 and later
1	+12V DC output	+5.0V DC output
2	GND	GND
3	GND	GND
4	+5.0V DC output	+12V DC output

Note: The +5.0V and 12V pin locations differ for the first (-01) and subsequent RTMs.

Table 7: J10 – P0 JTAG

Pin #	Description		Pin #	Description
1	TCK		2	DGND
3	TDO		4	+3.3V
5	TMS		6	nTRST
7	open		8	open
9	TDI		10	DGND

Table 8: J12 - IO header

Pin #	Description		Pin #	Description
1	User_I2C_SCL		2	User_I2C_SDA
3	GND		4	GND
5	IPMBB_SCL		6	IPMBB_SDA
7	GND		8	User_GPIO[4]
9	IPMBA_SCL		10	IPMBA_SDA
11	+3.3V_AUX		12	User_GPIO[3]
13	M_UART_RX		14	M_UART_TX
15	+5.0V_VS3		16	User_GPIO[2]
17	GND		18	User_GPIO[1]/AUX_CLK_DIR[1]
19	+12.0V_VS1		20	User_GPIO[0]/REF_CLK_DIR[1]

Note 1 – Ensure all switches on DIP switch SW4 are in the off position when using User_GPIO[1:0].

Table 9: J13 – VBAT connector

Pin #	Description
1	GND
2	P1-VBAT
3	P1-VBAT
4	GND

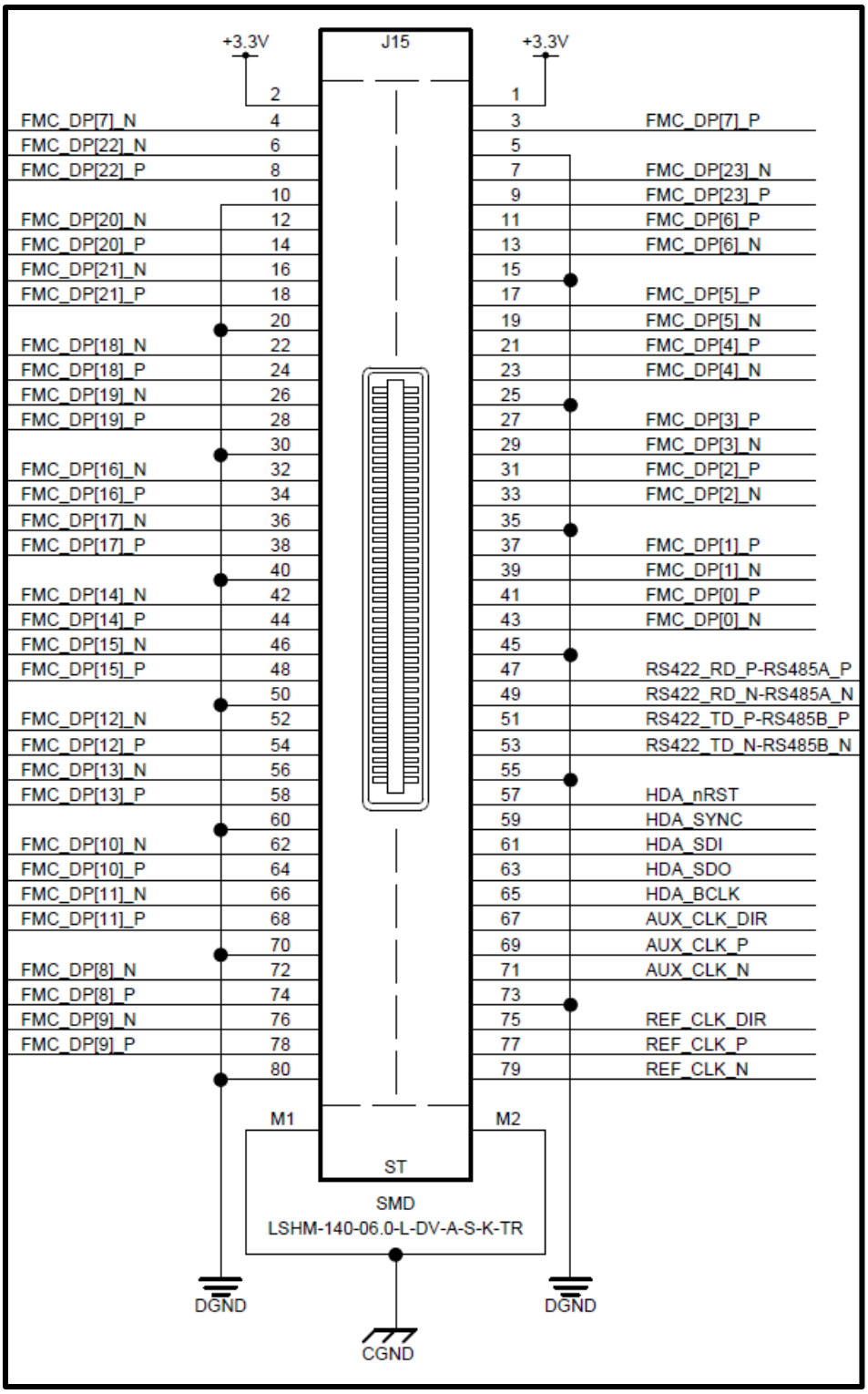

Figure 14: J15 high-density connector pinout

4 Specifications

This chapter provides the specifications for the functional areas of the VF370.

4.1 General Specifications

1. OpenVPX MOD3-PAY-2F2U-16.2.3-3 module profile, refer to 3.3 for detail.
2. VITA 57 FMC site with LA and HA connections, refer to 3.5.1 for detail.
3. Processor options:
    - Intel Atom x5 **E3930** (Standard build option)
        1. Dual-core Processor
        2. 1.3GHz base frequency (1.8GHz burst)
        3. TDP 6.5W
    - Intel Atom x5 **E3940**
        1. Quad-core 4 Processor
        2. 1.6GHz base frequency (1.8GHz burst)
        3. TDP 9.5W
    - Intel Atom x7 **E3950**
        1. Quad-core Processor
        2. 1.6GHz base frequency (2GHz burst)
        3. TDP 12W
4. Single-channel 4GB DDR3 @ 1333MT/s with ECC
5. On board SATA SSD @ Gen1 (1.5 Gbps), refer to 4.4 for SSD build option detail
6. External SATA interface @ up to Gen3 (6 Gbps)

4.2 Environmental Specification

4.2.1 Air-cooled module (non-coated)

Table 10: VF370 air-cooled non-coated specifications

Parameter	Class	Description
Operating Temperature	AC1	0 to +55 degrees Celsius with a linear air flow of > 2.5 m/s
Non-operating Temperature	C3	-50 to +100 degrees Celsius

4.2.2 Conduction-cooled module (ruggedization level 4, coated)

Table 11: VF370 conduction-cooled coated specifications (ruggedization level 4)

Parameter	Class	Description
Operating Temperature	CC4	-40 to +85 degrees Celsius at thermal interface Tested against MIL-STD-810 (Operational high and low temperature)
Non-operating Temperature	C4	-55 to +105 degrees Celsius Tested against MIL-STD-810 (Storage high and low temperature)
Random Vibration	-	Random vibration representing that of a helicopter with the following test level parameters: • W_0 = 0.001 g^2/Hz • W_1 = 0.01 g^2/Hz • f_t = 500 Hz • f_1 = 6.6 Hz, A_1 = 0.17 g • f_2 = 26.4 Hz, A_2 = 2.5 g • f_3 = 52.8 Hz, A_3 = 1.5 g • f_4 = 79.2 Hz, A_4 = 1.5 g Tested against MIL-STD-810 (Category 14 - Rotary Wing Aircraft)
Shock	OS1	Mechanical shock of 20g, 11ms sawtooth Tested against MIL-STD-810 (Method 516.6, Shock, Procedure I - Functional Shock)
Humidity	-	Fully operational at a relative humidity (RH) of 95% Tested according to MIL-STD-810 (Method 507.5, Procedure II – Aggravated)
Altitude	-	Fully operational at an altitude of 50,000 ft Tested according to MIL-STD-810 (Method 500.5, Procedure II – Operation/Air Carriage)

Consult the factory for other ruggedization levels of the air- and conduction-cooled VF370 variants.

4.2.3 Dimensions

Size (PCA) ……..…… 160 mm x 100 mm (excluding VPX connectors)

Width (air-cooled)…...……..… 5HP (1”) front panel

Width (conduction-cooled)…..… 4HP (0.8”)

Weight (PCA)……..…….. ≤ 160 g (Populated PCB with connectors and key guides, no mechanics)

Weight (PCA with CC)…… ≤ 520 g (With conduction-cooled mechanics)

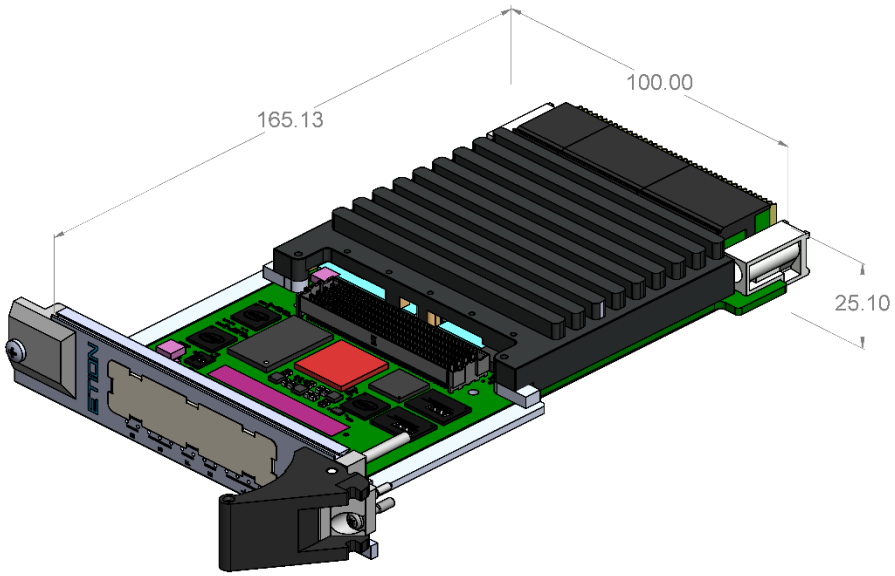

Figure 15: VF370 Air-cooled outline drawing.

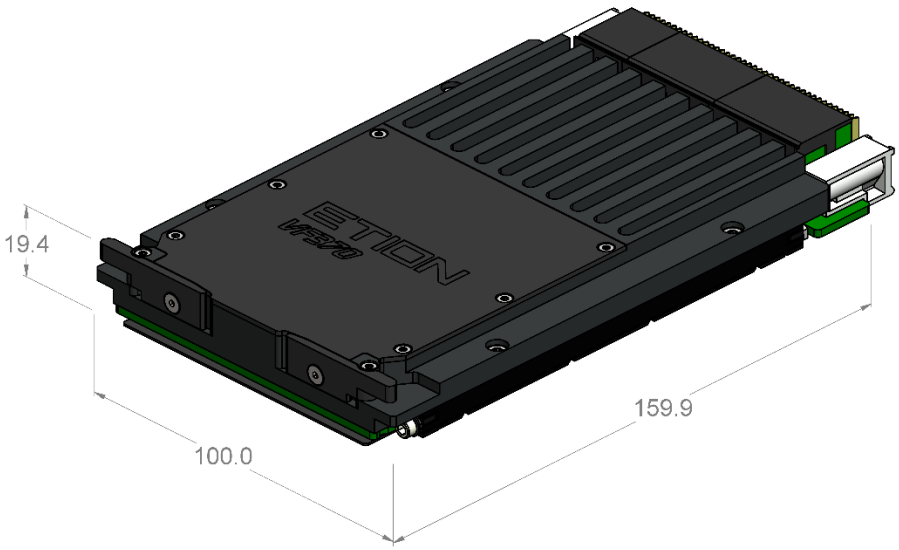

Figure 16: VF370 Conduction-cooled outline drawing.

4.3 Power Supply Requirements

The typical PSU current requirements for the VF370 with the E3930 Processor are shown in Table 12.

Table 12: VF370 Power supply requirements (E3930)

PSU Rail	Nominal Voltage	Min/Max Voltage	Minimum Current	Typical Current	High Current
Vs1	+12.0V	10.5V / 12.8V	N/A	N/A	N/A
Vs2	+3.3V	3.0V / 3.5V	1.2A	1.35A	2.5A
Vs3	+5.0V	4.6 / 5.4V	0.9A	2A	3A
3.3V_AUX	+3.3V	3.0V / 3.5V	0.38A	0.4A	0.45A
Total Power			~ 10W	~ 16W	~ 25W

Power consumption is highly dependent on the module build option, operational mode, system configuration and application software and firmware.

4.4 Ordering Information

The VF370 ordering information for the different build options is shown below.

Generic order code = VF370-Pxy-Fxy-Sxy-Ex-Ux-Vx-Dx-Ax-Sxy-Mxyz-Rxy-Cxy

-Pxy	-Fxy	-Sxy	-Ex	-Ux	-Vx	-Dx	-Ax	-Sxy	-Mxyz	-Rxy	-Cxy			
											-Cxy		Custom options (optional)
											-Rxy	1-4 : 0, 1	x: 0= 0 to 55 degC, 1=TBC, 2=TBC, 3=TBC, 4=Fully Rugged y: 0=un-coated, 1=conformal coated
											-Mxyz	A, C : 4, 5 : C, 0	Air, Conduction cooled, 4,5 HP width, Rear Cover present (C), No Rear cover (0)
											-Sxy	S/0 : S/0	Serial (RS422/485), No Serial (FMC I/Os) for RS485[A:B]
											-Ax	A, 0	HD Audio, No Audio output (FMC I/Os)
											-Dx	D, H, 0	DP, HDMI, No Display output (FMC I/Os)
											-Vx	3/5	3.3V, 5V GPIO voltage
											-Ux	I, M, U	I2C, MDIO, USB2
											-Ex	ES, EU	SATA, USB3
											-Sxy	32, 64, 00 : S, M	SATA SSD 32GB, 64GB, No SSD : SLC/MLC
											-Fxy	C7, C9, D7, D9, 00	C=CycloneV GX, D=CycloneV GT, 00=No FPGA
											-Pxy	15, 30, 40, 50, 00	E39xx variant, 00=No Processor

4.4.1 Standard air-cooled module

Order code = **VF370-P30-FC7-S32M-ES-UI-V5-DD-AA-SSS-MA5C-R10**

- E3930 Processor, CycloneV GX C7 FPGA, 32GB onboard MLC SSD
- External SATA, User I2C, 5V GPIO
- Display Port, HD Audio, 2x RS485 serial ports
- 5HP (1”) front panel width, rear cover, not coated

4.4.2 Full Rugged conduction-cooled module

Order code = **VF370-P30-FC7-S32M-ES-UI-V5-DD-AA-SSS-MC4C-R41**

- E3930 Processor, CycloneV GX C7 FPGA, 32GB onboard MLC SSD
- External SATA, User I2C, 5V GPIO
- Display Port, HD Audio, 2x RS485 serial ports
- 4HP width (0.8”), rear cover, ruggedization level 4, conformal coated

Contact the factory for other order codes / build options.

5 Installation and Setup

This chapter includes instructions for unpacking and installing the VF370.

5.1 Unpacking the product

Before unpacking the product, note the following guidelines:

1. Check the shipping carton for damage. If the product's shipping carton is damaged upon arrival, request that the carrier's agent be present during unpacking and inspection of the board.
2. Once unpacked, the board should be inspected carefully for physical damage, loose components etc. In the event of the board arriving at the customer's premises in an obviously damaged condition, Etion Create or its authorized agent should be notified immediately.
3. Make sure that the area designated for unpacking the product is a static electricity controlled environment. Unpack the VF370 board *only* on a ground conductive pad using an anti-static wrist strap grounded to the pad.
4. If moving the board is necessary, move it in an ESD protective container.
   Note: The VF370 board is shipped in an ESD protective container.

5.2 Installing the VF370 Hardware

Once the VF370 has been unpacked and inspected, it can be installed in a 3U VPX slot that is compatible with module profile MOD3-PAY-2F2U-16.2.3-3 and the following slot profiles:

- SLT3-PAY-2F2U-14.2.3

Plugging the VF370 into any other slots is NOT supported and can seriously damage the VF370. Etion Create should be contacted on any questions regarding VF370 compatible VPX slots.

It is strongly advised that, when handling the VF370 and its associated components, the user should wear an earth strap to prevent damage to the board as a result of electrostatic discharge.

The board is installed and powered up as follows:

- Ensure that the VF370 unit is only handled inside of an ESD controlled environment.
- Inspect the VF370 VPX connectors for any damage or debris.
  ↯ DO NOT insert the VF370 if any connector damage or debris is visible.
- Power down the VPX chassis/system.
- Carefully insert the VF370 into the VPX slot and secure by using the front side handles.
- Apply power to the VPX chassis/system and observe the LEDs through the small front panel holes (See Table 14 for more detail)
  - BM1 LED should be solid green.
  - BM2 LED should flash green at 1Hz.
  - Linux LED should flash a heartbeat sequence indicating the OS is running.
  - FPGA_CLK should flash yellow.
  - FPGA_USR1 should flash green.
  - SOC_L3 LED should be solid on, indicating a x4 PCIe Gen2 link to the PCIe SW.
  - FPGA_L11 should flash yellow, indicating a x4 PCIe Gen1 link to the PCIe SW.

5.3 Installing the VF370 Software and Firmware

The following is pre-installed on the VF370 module

- **BIOS**
- **Software (BSP)**
  - Linux kernel and file system with API and example application
  - Linux X86-64 drivers for FPGA
  - FPGA example application including
- **Firmware**
  - FPGA binary

The VF370 FPGA is configured with a Firmware Reference Design binary after power-up, no FPGA firmware need to be installed onto the VF370. An unconfigured FPGA (blank image) is available on request.

The VF370 FPGA Firmware Development Kit (FDK) is a separate order item.

5.3.1 Directory structure and file locations

The VF370 directory structure and related file locations are shown in Table 13.

Table 13: Directory structure and file locations.

Location	Description\ Contents
Documents (NextCloud) – VF370/docs	
/BIOS	BIOS upgrade howto file
/BMP	BMP upgrade howto file
/BSP	Changelog.txt Yocto.howto v1.xx (API versions)
/Marketing	VF370 Product Brief
/Manuals/VF370_UM.pdf	User Manual
VF370 OS image (onboard SSD)	
/usr/bin/test-api	API Test application
/usr/lib64/libbsp.so	API Library
/usr/bin/pci04_test	FPGA Test application
Tools	
https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Software/Drivers/Arrow_USB_Programmer	Arrow Blaster driver

5.4 Installing FW development tools

Quartus II Version 17.1 or later or Quartus Prime needs to be installed as development/debug environment for VF370 firmware. The Arrow USB blaster driver must be installed separately.

5.5 Installing a terminal program

A terminal program like Windows Hyper Terminal or PuTTY need to be installed on a test PC, since the VF370 does not have a GUI.

PuTTY can be found at www.putty.org

The VF370 is now ready for use, refer to § 6 for more information.

6 Operating Guide

This chapter provides information on proper operation of the VF370.

6.1 Configuration Settings

All configuration settings on the VF370 are performed through the BIOS settings, refer to § 7.1 for detail.

6.2 Status Indicators

The VF370 AC variant has thirteen front panel LEDs mounted on the bottom side of the PCB, visible through small pinholes in the front panel, refer to Figure 17. On the CC variant LED's are visible on the bottom of the module. The LED functions allocated are shown in Table 14.

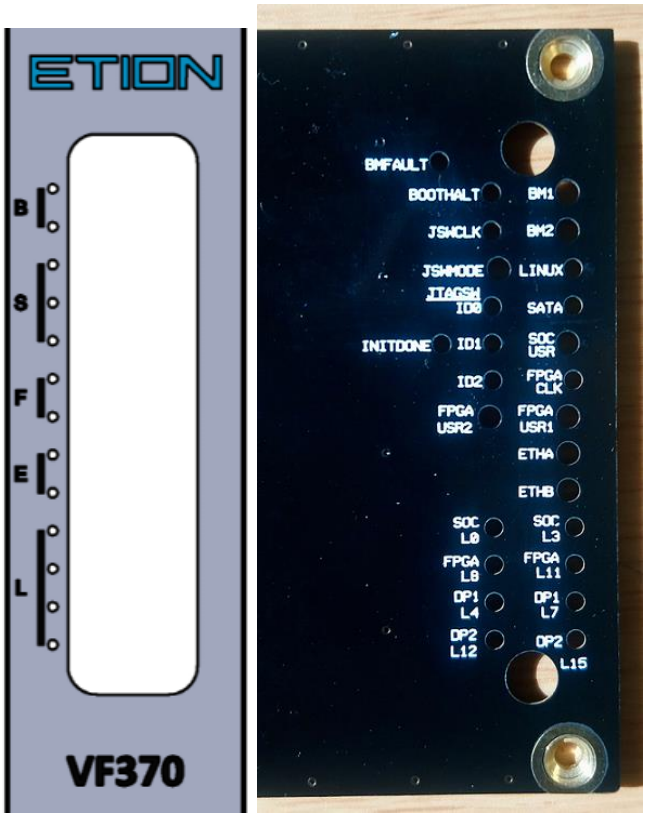

Figure 17: Front Panel and module bottom LED layout

Table 14: Front panel LED indicators (from top to bottom)

Position Front Panel	Position Module Bottom	LED	Status	Status description
B – 1	BM1	D10	BM1	**Solid Blue** – Starting up **Solid Yellow** – Start up completed with warning **Solid Green** – Start up completed with no warning **Solid Purple** – BMP service routine completed with warning
B – 2	BM2	D11	BM2	**Flashing Green** – BMP application executing **Flashing Yellow and Green** - Processor has access to log flash **Flashing Cyan and Blue** - Processor has access to FPGA configuration interface
S – 1	Linux	D33	Linux Heartbeat	OS is booted and running when flashing heartbeat sequence. **Off –** OS Boot failed
S – 2	SATA	D2	SSD	Flashing indicates internal SSD activity
S – 3	SOC USR	D32	Processor User LED	Functionality is programmable and determined by user. Default state is off.
F – 1	FPGA CLK	D15	FPGA_CLK	Flashing LED indicates FPGA internal clock is active
F – 2	FPGA USR1	D16	FPGA User LED	Functionality is programmable and determined by user. Default state – **flash green** indicating successful configuration.
E – 1	ETHA	D3	ETH Port A	**Off** – no connection **Flashing Green & Blue** – 1Gbps link **Flashing Green** – 100Mbps/10Mbps link
E – 2	ETHB	D4	ETH Port B	**Off** – no connection **Flashing Green & Blue** – 1Gbps link **Flashing Green** – 100Mbps/10Mbps link
L – 1	SOC L3	D13	Processor PCIe link	**Solid Yellow** – x4 Gen2 link established between Processor and PCIe SW **Flashing Yellow** - x4 Gen1 PCIe link established between Processor and PCIe SW
L – 2	FPGA L11	D5	FPGA PCIe link	**Solid Yellow** – x4 Gen2 link established between FPGA and PCIe SW **Flashing Yellow** - x4 Gen1 PCIe link established between FPGA and PCIe SW
L – 3	DP1 L7	D14	Backplane DP01 PCIe link	**Solid Yellow** – x4 Gen2 link established between DP01 and PCIe SW **Flashing Yellow** - x4 Gen1 PCIe link established between DP01 and PCIe SW
L – 4	DP2 L15	D12	Backplane DP02 PCIe link	**Solid Yellow** – x4 Gen2 link established between DP02 and PCIe SW **Flashing Yellow** - x4 Gen1 PCIe link established between DP02 and PCIe SW
	BMFAULT	D18	BM Fault indicator	**Solid Red –** Start-up Failed
	BOOTHALT	D23	Processor Boot Halt	**Solid Red –** Boot Halt signal to processor is asserted
	JSWCLK	D8	JTAGSW Clock	**Flashing Yellow –** JTAGSW clock is active
	JSWMODE	D27	JTAGSW Mode indicator	**Solid Green** – Normal (default) mode **Solid Red** – JTAG Switch reprogramming mode enabled **Solid Blue** – JTAG stearing mode enabled
	ID0	D26	See table Table 5	**Solid Yellow -** ID0 selection is switched on

Position Front Panel	Position Module Bottom	LED	Status	Status description
	ID1	D25	See Table 5	**Solid Yellow –** ID1 selection is switched on
	ID2	D24	See Table 5	**Solid Yellow –** ID2 selection is switched on
	INITDONE	D6	FPGA Initialisation	**Solid yellow –** FPGA busy initialising **OFF –** FPGA Initialisation complete
	FPGA USR2	D34	FPGA User LED	Functionality is programmable and determined by user. No Default state
	SOC L0	D19	Processor PCIe link	**Solid Yellow** – Lane 0 link indicator at Gen2 speed between Processor and PCIe SW **Flashing Yellow** - Lane 0 link indicator at Gen1 speed between Processor and PCIe SW
	FPGA L11	D21	FPGA PCIe link	**Solid Yellow** – Lane 0 link indicator at Gen2 speed between FPGA and PCIe SW **Flashing Yellow** - Lane 0 link indicator at Gen1 speed between Processor and PCIe SW
	DP1 L4	D20	DP01 backplane PCIe link	**Solid Yellow** – Lane 0 link indicator at Gen2 speed between DP01 and PCIe SW **Flashing Yellow** - Lane 0 link indicator at Gen1 speed between DP01 and PCIe SW
	DP2 L12	D22	DP02backplane PCIe link	**Solid Yellow** – Lane 0 link indicator at Gen2 speed between DP02 and PCIe SW **Flashing Yellow** - Lane 0 link indicator at Gen1 speed between DP02 and PCIe SW

6.3 VF370 Software

This section describes aspects related to software development on the VF370.

6.3.1 Processor PCIe mode

The Processor is always the root complex of the PCIe bus. It is possible to connect two VF370 modules through the backplane by enabling the non-transparent PCIe bridge (NTB) for DP01 or DP02. This setup is configurable in BIOS.

6.3.2 M_USB serial ports and M_UART functionality

Th VF370 provides two maintenance interfaces namely M_USB and M_UART. Both interfaces are accessible from the VR307 RTM.

Plug a USB cable into the mini USB connector of the VR307 to access the M_USB serial ports. The M_UART interface uses 3.3V UART logic signals and should be connected through a compatible USB to UART converter. Table 8 provides details for the M_UART pins.

When connected to the M_USB interface, two COM ports are enumerated on the PC/laptop. The lowest number COM port is always the Processor maintenance interface and the higher number is the BM maintenance interface. These ports are enumerated even if VF370 module is not powered.

6.3.3 Ethernet connection

The IP address of the module can be determined through the M_UART or M_USB ports. Open Hyper Terminal or PuTTY and connect to the serial port using the following settings - 115200 baud, 8N1 with no flow control. When powering the VF370 while connected to PuTTY, the Linux booting information or BM start up and service routine information should be displayed in the terminal window depending on the COM port connection.

Type **ifconfig**; the VF370 IP address should be displayed if connected to a DHCP server.

```
/ # ifconfig
eth0      Link encap:Ethernet  HWaddr 00:17:EA:D4:A1:15
          inet addr:172.17.7.58  Bcast:172.17.255.255  Mask:255.255.0.0
          UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
          RX packets:105 errors:0 dropped:0 overruns:0 frame:0
          TX packets:18 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:11033 (10.7 KiB)  TX bytes:5808 (5.6 KiB)
          Interrupt:48

lo        Link encap:Local Loopback
          inet addr:127.0.0.1  Mask:255.0.0.0
          UP LOOPBACK RUNNING  MTU:16436  Metric:1
          RX packets:0 errors:0 dropped:0 overruns:0 frame:0
          TX packets:0 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:0
          RX bytes:0 (0.0 B)  TX bytes:0 (0.0 B)
```

Figure 18: **ifconfig** terminal window

Connect an Ethernet cable into SFP transceiver module or RJ45 on the **VR307**, SSH to the VF370 and login as root. The terminal should now show the Linux root directory.

6.3.4 Test API application example application

The application can be used to verify the VF370 API functionality and extract health information such as voltages, current consumption and temperatures.

After logging into Linux (root with password r00t), type “test-api” to display the following menu:

```
Copyright 2019 Etion Create Pty (Ltd)
1. Distribution of source code must retain the above copyright notice and this list of conditions.
2. Distribution in binary form must reproduce the above copyright notice and this list of conditions (1 to 5).
3. Disclosure of this source code to any third party, with or without modification, is NOT permitted unless agreed to and explicitly stated by Etion Create Pty (Ltd) in writing.
4. The source and binary forms of this software is only supported in its original form.
The original form of this software is only supported when a valid and active support agreement exists between Etion Create Pty (Ltd) and the customer.
5. Any modified version of the source or binary forms of this software is not supported, unless agreed to and explicitly stated by Etion Create Pty(Ltd) in writing.

Application version: 1.2.0

Usage: test-api <-H|-P|-G|-I|-L|-S|-B| -r <offset> | -w <offset> | -d <cmd> | -c <cmd> | -l <count> | -g <low|high>>  [-f <filename>] [-F <filename>] [-t <sec|count>] [-v <level>]
       H: read VF370 health info
       P: read VF370 pbit info
       G: read GPIOs every second and show status (use -t for max period)
       I: detect interrupt on user GPIOs (use -t for time to wait)
       L: list elabels
       S: read serial port mode
       B: read PCIe BAR information
       p: (TODO) program FPGA configuration (flash|ps) (-t configfile)
              flash: write configuration to FPGA flash
              ps: program configuration directly to FPGA (passive-serial)
       v: verbose level 0=none(default), 1=normal
       r: read from user storage at offset for length given with option -l
       w: write to user storage at offset. Data is read from console (terminated with ctrl-D) or file (-f: specify filename)
       d: watchdog command (start|stop|kick)
              start: Start the watchdog with given time (-t: seconds)
              stop: Stop the watchdog
              kick: Reset the watchdog timeout to value set when enabled (for this application it is always 60 sec)
       c: command to send to BMP (etc|events|restart|reset|shutdown)
              etc: Get ETC of VF370
              events: Get event count of VF370
              restart: Restart VF370 immediately
              reset: Reset the SoC immediately
              shutdown: Notify BMP that the SoC will now shutdown (e.g. shutdown -P now)
       l: read log records (read|read_session|read_raw|parse_raw)
              read: Read specified number of log records (-t: specify the count)
              read_session: Session logs (-t: specify session, where the current session is 0)
              read_raw: Read the whole log flash to file (-f: binary output filename)
              parse_raw: Parse raw log flash image to text logs (-f: binary input filename, -F text output filename)
       g: set value on output GPIOs (-t: GPIO number)
              low: Set logic low
              high: Set logic high
       f: filename to read/store data (optional)
       F: filename to read/store data (optional)
       t: time in seconds OR count (default:10)
       h: help

NOTE: This file is compiled with the libbsp.so linked from the same directory as executable (not installed in default path)
```

Figure 19: Test API output

To view health information as an example, type “test-api -H”. This displays all external and internal voltages, temperatures and currents as shown below.

```
# 0:                          High voltage power input 1 voltage specifed in VITA 65 =  12098
# 1:  High voltage power input 2 voltage specifed differently for 3U or 6U in VITA 65 =   3323
# 2:                           Low voltage power input 3 voltage specifed in VITA 65 =   5065
# 3:                                                          SSD supply voltage =   1205
# 4:   FMC adjustable voltage level power from the carrier to the IO mezzanine module =   2512
# 5:                      Pre-driver supply voltage for the FMC I/O bank of the FPGA =   2518
# 6:                                          FPGA and PCIe Switch supply voltage =   2510
# 7:                                          12V0 auxiliary power supply voltage =      0
# 8:                                                        SoC 3V3 rail voltage =   3317
# 9:                                                        SoC 1V8 rail voltage =   1811
#10:                                       SoC core graphics ISP supply voltage =    893
#11:                                             SoC 1V35 rail voltage for DDR =   1355
#12:                                                   FPGA DDR supply voltage =   1504
#13:                                               FPGA transceiver supply voltage =   1109
#14:                                               PCIe Switch core supply voltage =   1007
#15:  High voltage power input 2 current specifed differently for 3U or 6U in VITA 65 =   1242
#16:                           Low voltage power input 3 current specified in VITA 65 =    967
#17:                                3V3 aux current: 3V3 auxiliary supply current =    372
#18:                                          PMIC switching regulator 0 current =    248
#19:                                          PMIC switching regulator 1 current =    272
#20:                                          PMIC switching regulator 2 current =    272
#21:                                          PMIC switching regulator 5 current =    272
#22:                                          PMIC switching regulator 6 current =    276
#23:                                  Voltage regulator A Buck output 0 current =    220
#24:                                  Voltage regulator A Buck output 1 current =     80
#25:                                  Voltage regulator A Buck output 2 current =    120
#26:                                  Voltage regulator A Buck output 3 current =      0
#27:                                  Voltage regulator B Buck output 0 current =     20
#28:                                  Voltage regulator B Buck output 1 current =    340
#29:                                  Voltage regulator B Buck output 2 current =   1420
#30:                                  Voltage regulator B Buck output 3 current =    300
#31:                                                       SoC DDR temperature =  28000
#32:                                                PCIe switch temperature =  41000
#33:                                                      FPGA temperature =  26000
#34:                                                     VF370 temperature =  25000
#35:                                           FPGA core supply temperature =  26000
#36:                                              FMC site temperature =  29000
#37:                                                BM die temperature =  30000
#38:                                               PMIC die temperature =  28000
#39:                                                     SPD temperature =  56513
#40:                                               SoC core temperature =  35000
#41:                             PMIC recorded cause of previous shutdown/reset =      0
SPD Temperature within range (-20000 < 57025 < 850000)
SoC Temperature within range (-20000 < 35000 < 850000)
12V within range (11500 < 12103 < 12500)
3V3 within range (3200 < 3323 < 3400)
```

6.4 VF370 Firmware

Refer to [2] for more information.

6.4.1 Arrow USB-Blaster

Switch the DIP Switch-3 on the VR307 as shown in Figure 12.

Ensure the Arrow blaster driver provided is installed before plugging a USB cable into the mini USB connector (J6) on the VR307. Refer to 3.7.1 for detail.

Run the Quartus II Programmer, click on “Hardware Setup” and select the available Arrow USB Blaster.

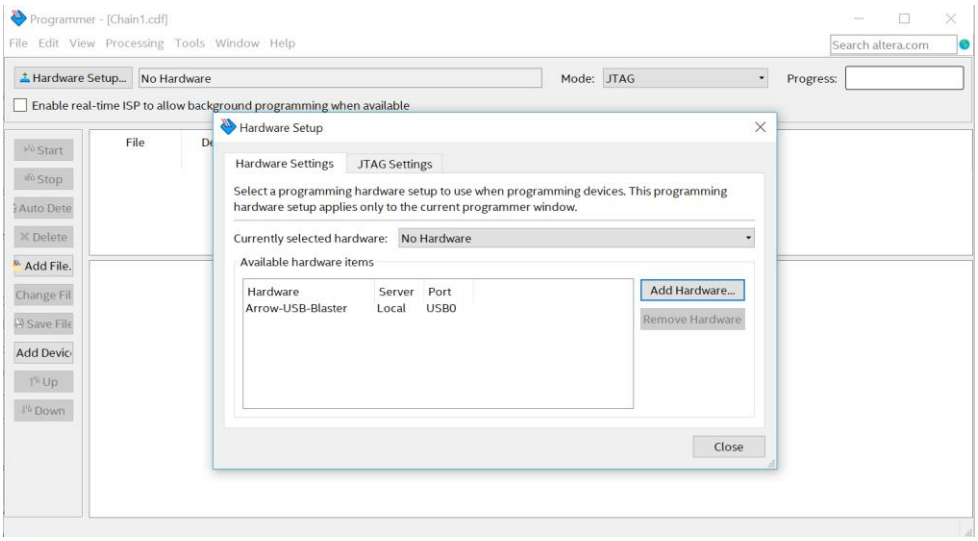

Figure 20: Arrow USB Blaster setup

6.4.2 Configuring the FPGA through JTAG

To configure the FPGA (volatile), click on “Auto Detect” and select the relevant FPGA device, i.e. 5CGXFC7D6 for the standard VF370. The FPGA is now listed. Right click on the FPGA in the list, select “Change File” and browse to the .SOF file to configure the FPGA with. Tick the “Program/Configure” box and press “Start”. The VF370 FPGA will now be configured with the selected .SOF file.

The FPGA configuration is volatile and will be lost after a power cycle.

6.4.3 Programming the FPGA configuration flash through JTAG

To program the FPGA configuration flash, a .JIC file first need to be created from the .SOF file.

In Quartus II or the Quartus II Programming, go “File => Convert Programming Files”

Set **Programming File Type** to => .JIC
Set **Configuration Device** to => EPCQ256
Set Mode to => Active Serial

Select **Flash Loader** and click on **Add Device,** select the **Cyclone V** Device family and the 5CGXFC7D6 Device name (standard VF370).

Select **SOF Data** and then **Add File** to add the SOF file created in Quartus.

Select the added SOF file, click on **Properties** and tick (enable) the **Compression** box, then press **OK**

Click **Generate** to create the .JIC file

Add the generated JIC file to the Quartus II Programmer and program the FPGA.

Power cycle the VF370 and the FPGA will be configured with the programmed SOF data.

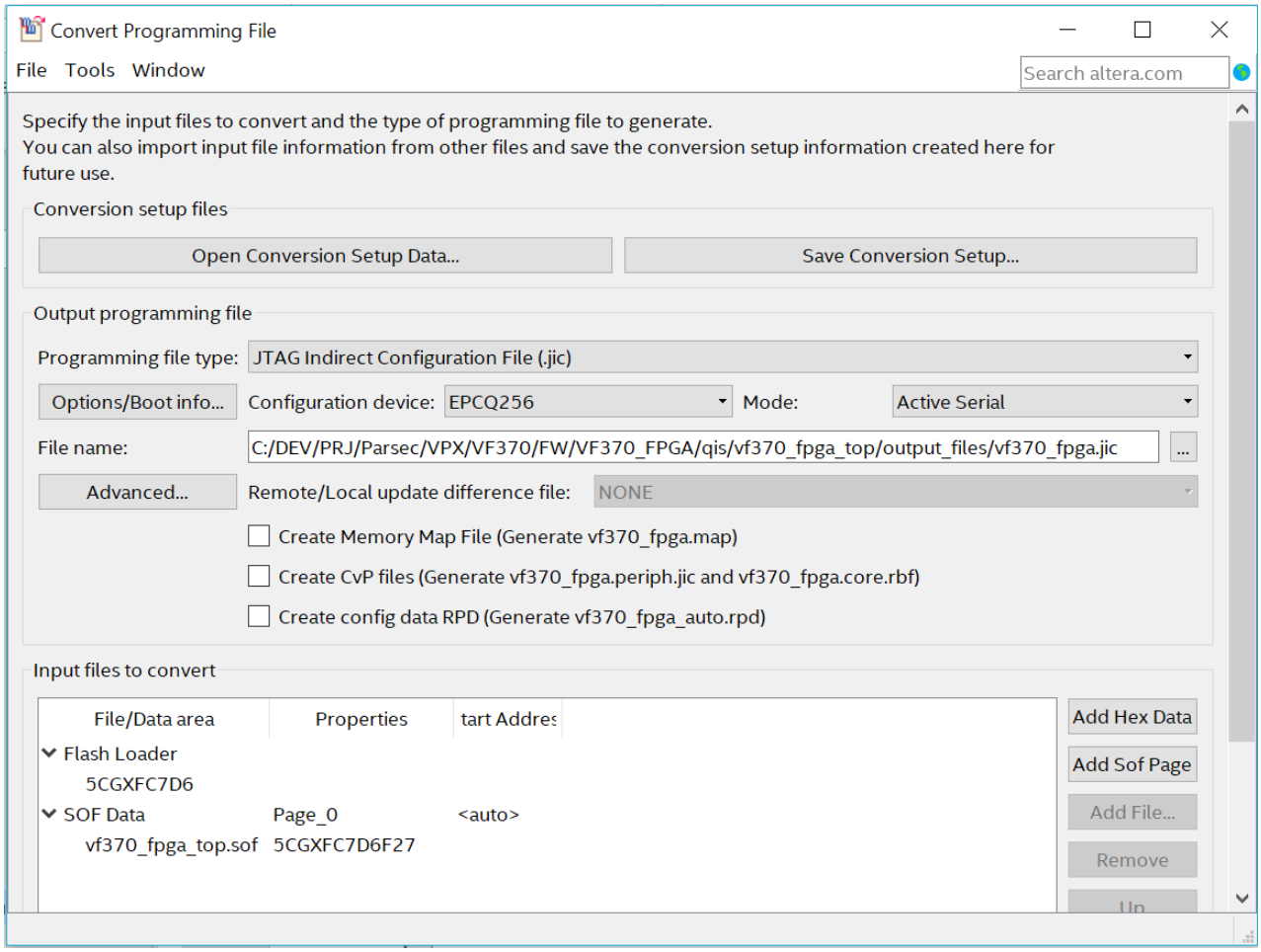

Figure 21: FPGA programming via JTAG

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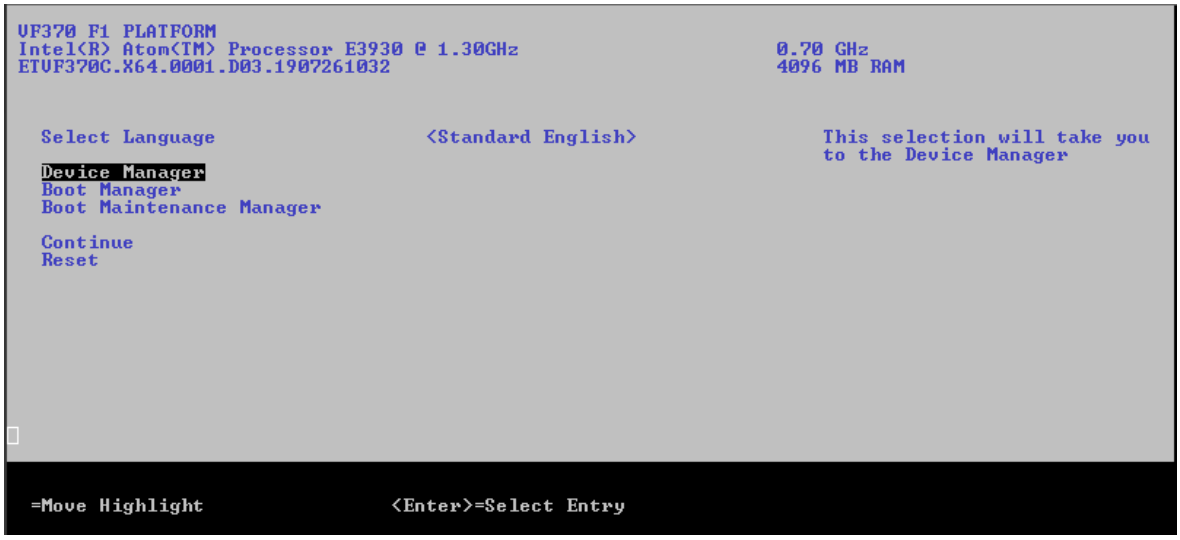
7 BIOS

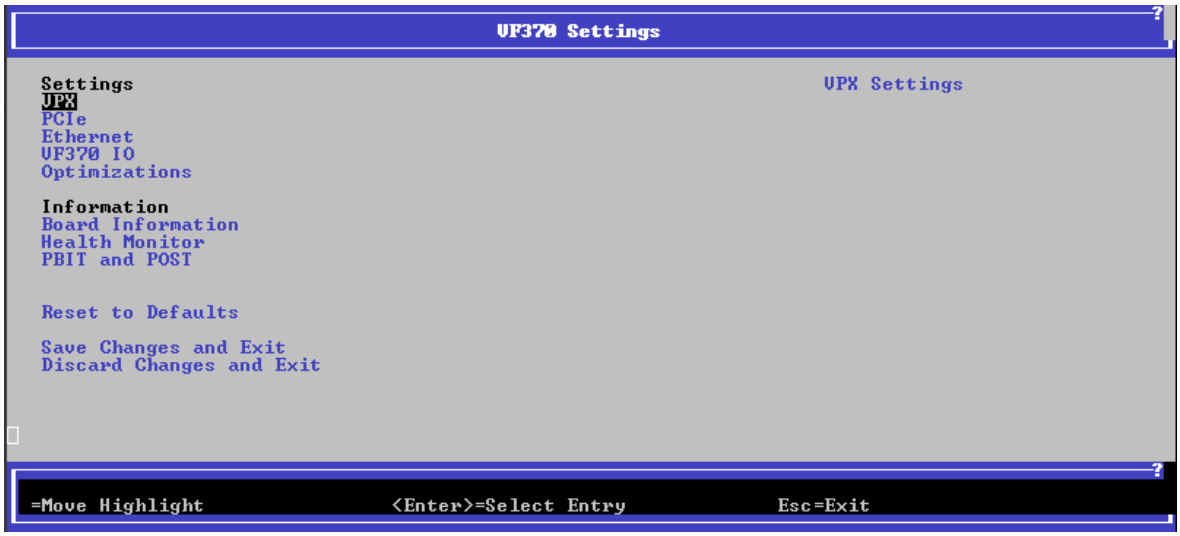
This chapter describes the VF370 BIOS settings.

7.1 BIOS settings

Through the Maintenance USB port, the BIOS settings can be accessed by pressing “F2”, while the VF370 is starting up. Connect PuTTY or Hyper Terminal to the Processor Maintenance USB port as described in section 6.3.3. The BIOS menu will now be displayed:



VF370 Configuration settings are located under Device Manager. This is where settings for PCIe, VF370 IO’s, Ethernet settings and VPX related settings are located:



Default settings are shown in **bold**.

Table 15: VPX BIOS settings

Setting	Options	Description
System Controller	**nSYS_CON**	The System controller state corresponds to the VPX signal
SYSRESET Signal Output	Off On **System Controller**	SYSRESET will never be driven SYSRESET will always be driven SYSRESET is only driven when board is System Controller
SYSRESET Signal Input	**Slave** On	SYSRESET is input only when not System Controller SYSRESET is always input

Setting	Options	Description
SYSRESET Signal Delay	Delay in ms **Default 0ms**	Time to wait after SYSRESET de-asserted
PCI Enumeration Delay	Delay in ms **Default 0ms**	Time to wait before enumerating PCI Bus
VPX REF_CLK	**Off** System Controller	REF_CLK is always off REF_CLK is driven only when board is System Controller
Maskable Reset Input	On/**Off**	If On, the maskable reset input signal generates a warm reset to the VF370
VAdj Selection	**BIOS Selection** FMC Selection	VaAdj Voltage is set through BIOS setting VAdj voltage is set through FMC EEPROM
VAdj Voltage	1.2V,1.25V, 1.35V, 1.5V, 1.8V, **2.5V**, 3.0V or 3.3V	VAdj Voltage value

Table 16: PCIe Settings

Setting	Options	Description
Backplane links DP01	**1 x4**; 8 x1	PCIe Lane setup configuration for DP01
Backplane links DP02	**1 x4**; 4 x1	PCIe Lane setup configuration for DP01
MAX Link speeds	**5.0Gbps**; 2.5 Gbps	Configure link speeds for Processor to PCIe SW, DP01 and DP02
Backplane link for NTB	**DP01**; DP02	Select backplane link to configure as Non-Transparent Bridge

Table 17: Ethernet configuration

Setting	Options	Description
CPUT01 Interface	1000BaseBX, **1000BaseKX** or external PHY	Select interface for CPUTP01
CPUT01 Autoneg	On/**Off**	Switch auto negotiation on or off for CPUTP01
CPUT02 Interface	1000BaseBX, 1000BaseKX or **external PHY**	Select interface for CPUTP02
CPUT02Autoneg	**On**/Off	Switch auto negotiation on or off for CPUTP02

Table 18: I/O Settings

Setting	Options	Description
UART Mode	**RS422**/RS485	Selects between external RS422 or RS485 interface
Watchdog	Enable/**Disable**	Enables or disables the Processor watchdog
GPIO [4:0]	**Output High (Tri-stated)** or Output Low	Selecting the open-drain Output High (tri-stated), pulls the output high and allows external devices to drive the I/O low. Selecting Output Low, drives the open-drain IO low and cannot be driven high by external devices.