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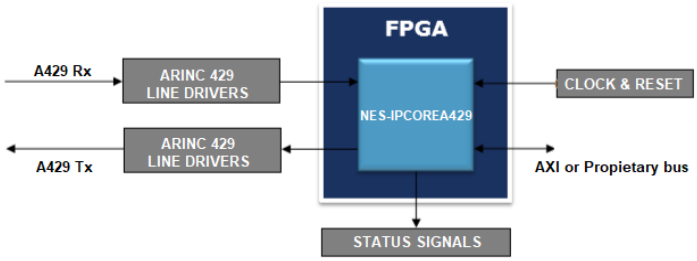
NES-IPCORE-A429

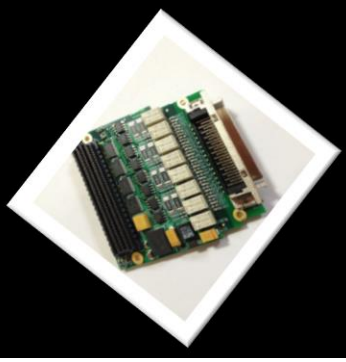
IP CORE ARINC-429

HIGHLIGHTS

- Independent Receivers (Rx) with FIFO
- Independent Transmitter (Tx) with FIFO
- Decoding signals interface type
- 16-Bit Data-bus
- Direct addressing of all Registers
- Support all ARINC 429 Data Rate Transfer
- Multi Label Capability
- Parity Control : Odd, Even, No Parity, Interrupt Capability
- Independent Interrupt Request Line for Rx and Tx Functions
- System clock 70 MHz can be customized



RELATED PRODUCTS



VAULT GUI

FMC™

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OVERVIEW

The NES-IPCOREA429 macro implements a ARINC 429 protocole with Transmit and Receive Controllers . The macro controls all ARINC 429 bus specific sequences, protocol and timing.

The NES-IPCOREA429 macro interface allows the parallel-bus microprocessor to communicate bidirectionally with the ARINC 429 bus. This macro can be customized according to specific needs (application specific requirements).

Any other pre-designed functions can be integrated into the FPGA. FPGA density and I/O requirements can be defined according to customer specifications.

Designers should be familiar with ARINC 429 standard,VHDL, synthesis tools, FPGA Place and Route data flow and VHDL simulation software. Experience with microprocessor is recommended. The macro can easily be integrated into hierarchical VHDL designs.

ORDERING INFORMATION:‘

NES-IPCORE-A429 IP CORE ARINC-429 Transmit/ Receive
NES-IPCORE-A429-Tx IP CORE ARINC-429 Transmit only
NES-IPCORE-A429-Rx IP Core ARINC-429 Receive only