

# NES-IPCORE-M1553

## IP CORE MIL-STD1553 BC/RT/MT

### ▶ HIGHLIGHTS

MIL-STD1553 intellectual property for FPGA and ASIC

Suitable for any MIL-STD1553 BC,RT,MT implementation

Local bus or AXI interface

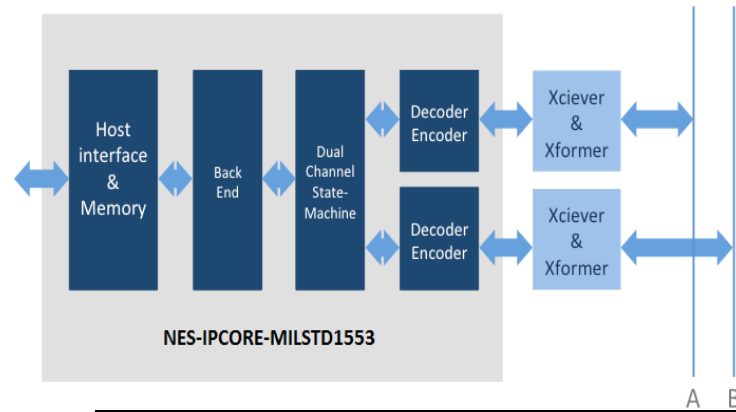
Small FPGA area utilization

Modular Architecture allowing flexible implementations

Provided with verification environment

Based on vendor and technology independent VHDL code

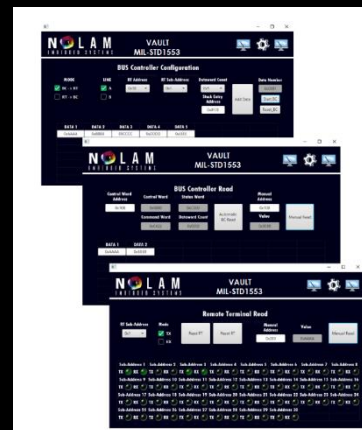
Configuration available : Simple Front end ,Local Bus and AXI interface



### ▶ RELATED PRODUCTS



**NES-FMC1553**



**VAULT-GUI**

# NES-IPCORE-M1553

## IP CORE MIL-STD1553 BC/RT/MT

### ► OVERVIEW

Combining the benefits of programmable devices (FPGA) and Nolam Embedded systems IP Cores provides a small-size, robust, reliable, flexible, future-proof and cost effective solution for Mil-Std-1553 interface.

Nolam Embedded systems IP cores are designed for any requirement and application. Customers can choose between various configurations and interfaces.

The NES-IPCORE-M1553 is designed for simple applications, where no CPU is controlling the system, to the most complex implementations, where a Local Bus is used by the CPU or Axi bus.

The NES-IPCORE-M1553 is available and is working with any FPGA, clock frequency and 1553 transceiver, providing the most robust, yet flexible, solution.

<b>Compatibility</b>	MIL-STD1553 MIL-STD1553B Notice 2 and 1760 RT Validated according to test plan from MIL-HDBK-1553A 1Mbps Data Rate Connects to any transceiver ,Transformer pair
<b>RAM :</b>	4,8,16,32,64K by 16 bits Dual port RAM (Limited by FPGA resources only)
<b>Clock :</b>	Any Even frequency from 12Mhz and higher 100Mhz,...) Including 33Mhz for PCI and 125Mhz for PCI Express implementations
<b>Supported FPGA :</b>	Any FPGA with sufficient number of LUTs and dual port memory FPGA families from the following vendors : Xilinx (AMD),Altera (Intel),Lattice , Achronix ,Efinix ,Microchip ,Quicklogic
<b>Deliverables</b>	Net list for the desired core (BC/RT/MT) for FPGA family and memory User's Manual Sample VHDL code that incorporates Synthesis script for sample code

The NES-IPCORE-M1553 is suitable for simple 1553 applications, protocol translators and hardware based implementations. NES-IPCORE-M1553 is suitable for more complex 1553 implementations, where the application is controlled by software.

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## IP CORE MIL-STD1553 BC/RT/MT

### ► OVERVIEW

Nolam Embedded Systems IP Cores require very small space from FPGA for complex applications. The following table summarizes the various available configurations :

<b>Backend Interface</b>	Local bus or PCI,compatible with existing drivers and applications No need to rewrite drivers code Eliminates replacement risk
<b>Manchester Recorder :</b>	The unique Manchester decoder can work with any clock reduce clock resources and clock domain on board (reduces EMI/RFI). Advanced algorithms for filtering out noise and disturbances enable the core to operate in harsh environments.
<b>Advanced Verification :</b>	To ensure a fully reliable and robust product the core was developed using advanced verification environment that includes a Random-generation engine ,code coverage and assertion tools. All 1553 protocol ,functions and performance requirements were verified.
<b>Simple Integration :</b>	In order to simplify the integration of the core, a sample VHDL design that uses the core is provided ,including : A comprehensive users manual A VHDL gate level model of the core for the target technology A Tranceiver VHDL model that connects the core to 2 buses A bus tester VHDL model that generates 1553 messages and checks the return replies A top test bench that instantiates all of these components to working example

#### ORDERING INFORMATION:

NES-IPCORE-M1553	IP MIL-STD1553 BC/RT/MT
NES-IPCORE-M1553-BC	IP MIL-STD1553 BC mode only
NES-IPCORE-M1553-RT	IP MIL-STD1553 RT mode only