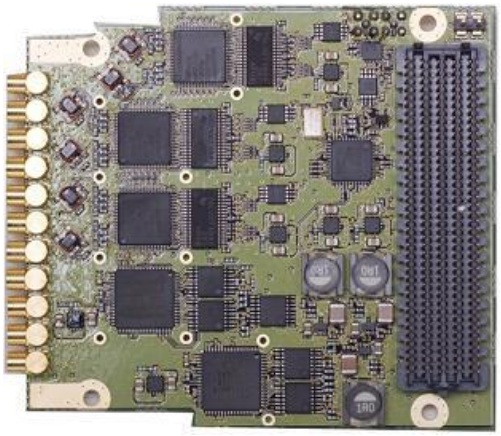
RFM-ADAFF62-A105/P500MH
(FMC AD/DA Board)
Hardware Referential Manual

Ver. 1.0



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Revision History

Revision	Date	Changes
ver1.0	2013/05/23	First Revision.

Table of Contents

Preface

Thank you for choosing our products. This user manual provides function and specification of RFM-ADAFF62-A105/P500MH. This manual describes the features and specifications of the board. Read and understand the contents of this manual before operating this board.

K.K Rocky reserves the right to revise this document and to make changes without notice.

Safety Instructions

Please keep the safety issue below for safety reason.

- **If smoke or an abnormal odor is detected from the board, power off and stop using the board.**
  Continuous use of the board under these conditions might cause fire or permanent damage to the system. Contact K.K.Rocky to test and repair.
- **Do not attempt to disassemble and modify this board.**
  Disassembly and modification could cause fire or electric shock.
  Please contact K.K.Rocky for any repair and test service.
- **Never allow any liquids to spill on the board, and never expose the board to water or moisture.**
  Exposure to liquid or moisture could cause electric shock or fire.
- **Avoid excessive vibration and any impact or shock to the board.**
  Neglect could result in any damage on the board.
- **Avoid handling the FMC board while it is powered. Only handle by the edges to minimize the risk of electrostatic discharge damage.**
- **If the board has been dropped and damaged, stop using the board and contact K.K.Rocky to repair.**
- **Never place the board where it will be exposed to excess heat, such as in direct sunlight, or near heater.**

1. Overview

This is FMC Mezzanine board which has 6 channel A/D and 2 channel D/A ports.

2. Hardware Overview

Table 2-1 shows main parts of the board.

Table 2-1 Main Parts

Subjects	Description	Remarks
FMC Connector (HPC)	ASP-134488-01 (SAMTEC Corp.)	
A/D Convertor	AD9650BCPZ-105 (Analog Devices)	
D/A Convertor	MAX5888AEGK+D (MAXIM)	
Clock Generator	AD9518-3ABCPZ (Analog Devices)	
Referential Clock Oscillator	FOX914B-20.000 (FOX)	
EEPROM(I2C)	BR24L01AFV-WE2 (ROAM Corp.)	
Coaxial Connectors (Front)	MMCX-LR-PC-1(40) (HIROSE Corp.)	
Coaxial Connectors (Board)	MMCX-R-PC(40) (HIROSE Corp.)	
(Ex. Coaxial Cable)	RF316-01SP1-03SP1-0500 (SAMTEC)	

3. Block Diagram

Figure 3-1 shows Block Diagram of the board.

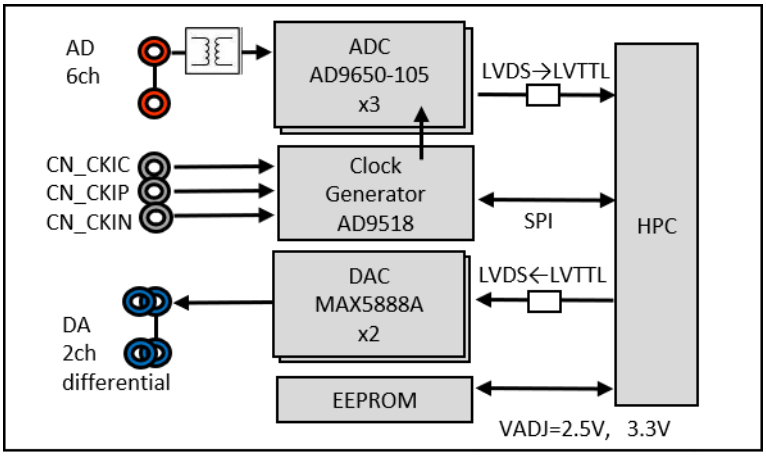


Figure 3-1 Block Diagram

4. Board Layout

Figure 4-1 shows the Layout of the board and Table 4-1 shows connectors of the board.

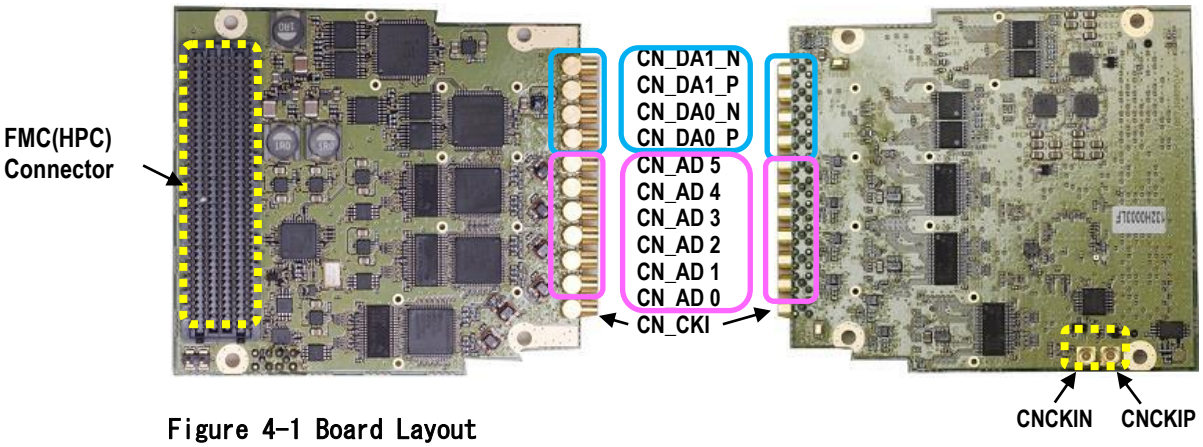


Figure 4-1 Board Layout

Table 4-1 Connectors of the board

Subjects	Description	Remarks
FMC Connector	FMC Connector (High-Pin Count)	ASP-134488-01 (SAMTEC Corp.)
CN_DA0_P／CN_DA0_N CN_DA1_P／CN_DA1_N	D/A Differential Analog Output	MMCX-LR-PC-1(40) (HIROSE Corp.)
CN_AD0～CN_AD5	A/D Analog Input	MMCX-LR-PC-1(40) (HIROSE Corp.)
CN_CKI	Single-end Clock IN	MMCX-LR-PC-1(40) (HIROSE Corp.)
CNCKIN	Differential Clock IN (－)	MMCX-R-PC(40) (HIROSE Corp.)
CNCKIP	Differential Clock IN (＋)	MMCX-R-PC(40) (HIROSE Corp.)

5. Interface Specification

5.1 A/D Input Specification

Table 5-1 shows the A/D input specification.

Table 5-1 the A/D input specification

Subjects	Description
Channel Number	6 CH
Resolution	16 bit
Coupling	AC Coupling with transformer.. Trans parts : Mini-Circuits TC4-1T(0.5-300MHz) 1 : 2
Input Impedance	50Ω (Single-End)
Input LPF	400KHz～30MHz@-3dB
Max Input Level	1.4Vpp

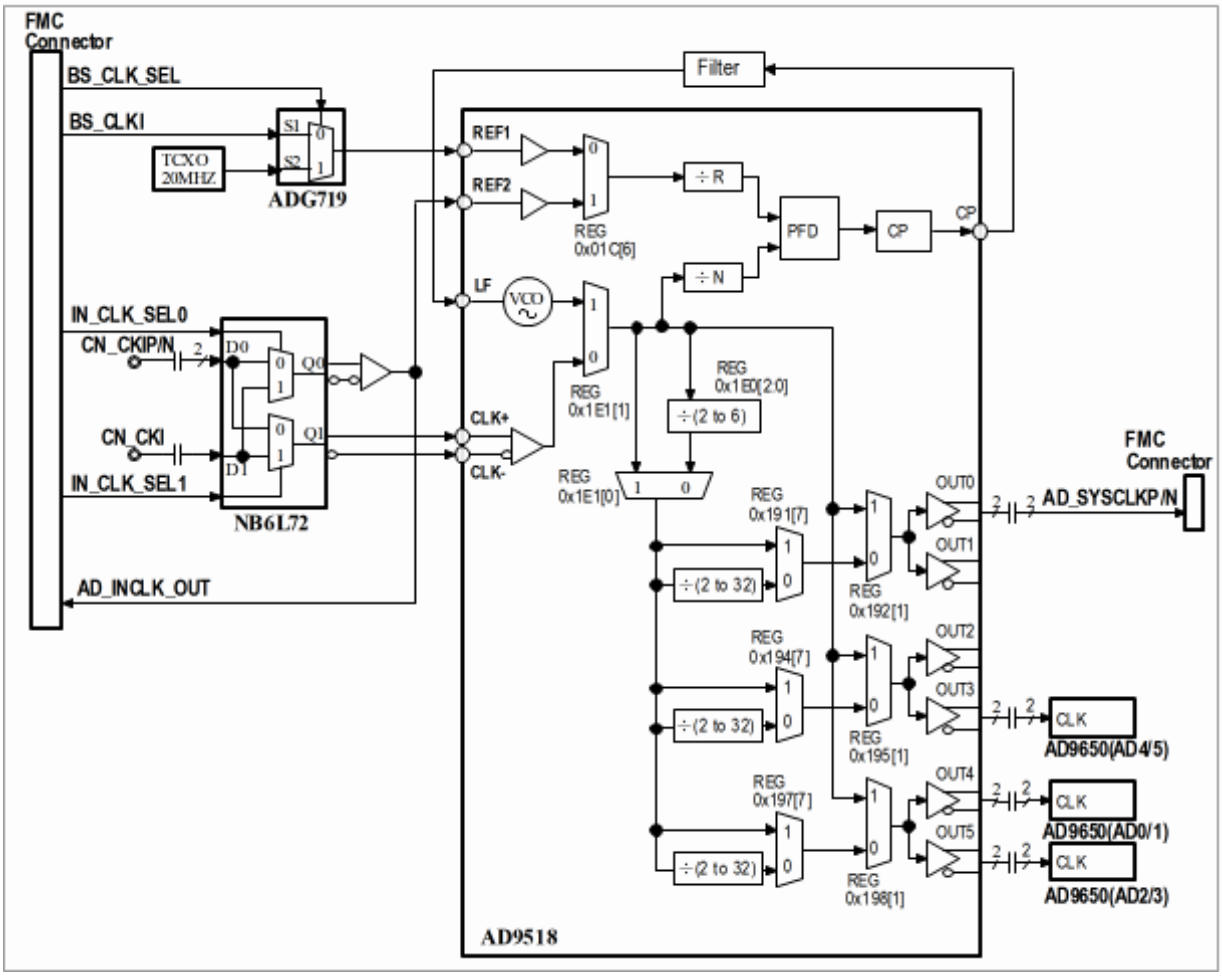
5.2 A/D Sampling Clock

Table 5-2 shows the specification of the A/D Sampling Clock and Figure 5-1 shows the Clock Diagram.

Table 5-2 Specification of the A/D Sampling Clock

Subjects	Remarks
External Input	Capacitor coupled Differential Capacitor coupled Single-ended
PLL Device	Analog Devices AD9518-3 (2.0GHz on-chip VCO)
REF Oscillator	TCXO 1.5ppm/℃ 20MHz
REF0 Input	FMC Carrier or TCXO
REF1 Input	External Input (CN_CKIP/N or CN_CKI)
CLK Input	AD9518 Through Mode or PLL Mode

Figure 5-1 Clock Layout



5-3 Analog Output Specification

Table 5-3 shows the Analog output specification.

Table 5-3 the Analog output specification.

Subjects	Description
Channel Number	2 CH
Resolution	16 bit
Coupling	Differential
Output Impedance	50Ω (Differential)
Output Voltage Range	0 ～1V (Differential ±1Vpp max) Output voltage range can be changed by replacing reference resister. (factory setting)

6. FMC Connector

FMC HPC PIN Assignment is based on ANSI/VITA57.1 standard.
Figure 6-1 shows HPC PIN Assignment and Table 6-1 shows HPC Signal Assignment.

Figure 6-1 HPC PIN Assignment.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	AD_PGOOD	GND	PG_C2M	GND		GND
2	GND		PRSNT_M2C	CLK1_M2C_P	GND		GND		GND	
3	GND		GND	CLK1_M2C_N	GND		GND		GND	
4		GND	AD_SYSCLKP	GND	DA1_CLK	GND		GND		GND
5		GND	AD_SYSCLKN	GND	HA00_N_CC	GND		GND		GND
6	GND	DA1_B2	GND		GND	DA1_B6	GND		GND	
7	DA1_B0	DA1_B3	DA0_B0		DA1_B4	DA1_B7	GND		GND	
8	DA1_B1	GND	DA0_B1	GND	DA1_B5	GND	DA0_CLK	GND		GND
9	GND	DA1_B10	GND	DA0_B2	GND	DA1_B14		GND		GND
10	DA1_B8	DA1_B11	DA0_B4	DA0_B3	DA1_B12	DA1_B15	GND	DA0_B8	GND	
11	DA1_B9	GND	DA0_B5	GND	DA1_B13	GND	DA0_B6	DA0_B9	GND	
12	GND		GND	DA0_B12	GND		DA0_B7	GND		GND
13	DA1_PD		DA0_B10	DA0_B13			GND	GND		GND
14	DA1_SEL0	GND	DA0_B11	GND		GND	DA0_B14	DA0_PD	GND	
15	GND		GND		GND	IN_CLK_SEL 0	DA0_B15	DA0_SEL0	GND	
16	_AD0_NCS						GND	GND		GND
17	_AD1_NCS	GND		GND		GND		GND		GND
18	GND	_AD2_NCS	GND		GND	_AD_SCK			GND	
19	PLL_NCS					_AD_SDIO	GND		GND	
20	PLL_NRST	GND		GND	AD_SYNC	GND	AD2_DCO	GND		GND
21	GND	PLL_MON	GND	AD2_D2	GND	AD1_D4		GND		GND
22	PLL_LOCK	PLL_SDIO	AD2_D0	AD2_D3	AD1_D2	AD1_D5	GND		GND	
23	PLL_SCLK	GND	AD2_D1	GND	AD1_D3	GND	AD2_D8		GND	
24	GND	AD1_D0	GND	AD2_D6	GND	AD1_D8	AD2_D9	GND		GND
25	AD1_DCO	AD1_D1	AD2_D4	AD2_D7	AD1_D6	AD1_D9	GND	GND		GND
26		GND	AD2_D5	GND	AD1_D7	GND	AD2_D14	AD2_OR	GND	
27	GND	AD1_D12	GND	AD2_D12	GND	AD1_OR	AD2_D15		GND	
28	AD1_D10	AD1_D13	AD2_D10	AD2_D13	AD1_D14		GND	GND		GND
29	AD1_D11	GND	AD2_D11	GND	AD1_D15	GND		GND		GND
30	GND	AD0_D1	GND		GND	AD0_D5	TDI	SCL	GND	
31		AD0_D2			AD0_D3	AD0_D6	TDI	SDA	GND	
32	AD0_D0	GND		GND	AD0_D4	GND	3P3VAUX	GND		GND
33	GND	AD0_D9	GND	BS_CLK1	GND	AD0_D15		GND		GND
34	AD0_D7	AD0_D10		BS_CLK_SEL	AD0_D11	AD0_OR		GA0	GND	
35	AD0_D8	GND		GND	AD0_D12	GND	GA1	12P0V	GND	
36	GND	AD0_D13	GND	AD_INCLK_O UT	GND		3P3V	GND		GND
37	AD0_DCO	AD0_D14		IN_CLK_SEL 1			GND	12P0V		GND
38		GND		GND		GND	3P3V	GND	GND	
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND		GND

Table 6-1 HPC Signal Assignment

Pin#		Signal Name	FMC_LOC	I/O	Remarks
E	18	_AD_SCK	HA20_P	I	
E	19	_AD_SDIO	HA20_N	I/O	
K	16	_AD0_NCS	HA17_P_CC	I	
K	17	_AD1_NCS	HA17_N_CC	I	
J	18	_AD2_NCS	HA18_P	I	
G	36	AD_INCLK_OUT	LA33_P	O	
F	1	AD_PGOOD	PG_M2C	O	
F	20	AD_SYNC	HA19_N	I	
H	5	AD_SYSCLKN	CLK0_M2C_N	O	
H	4	AD_SYSCLKP	CLK0_M2C_P	O	
K	32	AD0_D0	HB10_N	O	
J	30	AD0_D1	HB11_P	O	
J	31	AD0_D2	HB11_N	O	
J	31	AD0_D2	HB11_N	O	
F	31	AD0_D3	HB12_P	O	
F	32	AD0_D4	HB12_N	O	
E	30	AD0_D5	HB13_P	O	
E	31	AD0_D6	HB13_N	O	
K	34	AD0_D7	HB14_P	O	
K	35	AD0_D8	HB14_N	O	
J	33	AD0_D9	HB15_P	O	
J	34	AD0_D10	HB15_N	O	
F	34	AD0_D11	HB16_P	O	
F	35	AD0_D12	HB16_N	O	
J	36	AD0_D13	HB18_P	O	
J	37	AD0_D14	HB18_N	O	
E	33	AD0_D15	HB19_P	O	
K	37	AD0_DCO	HB17_P_CC	O	Data Clock
E	34	AD0_OR	HB19_N	O	Over Range
J	24	AD1_D0	HB01_P	O	
J	25	AD1_D1	HB01_N	O	
F	22	AD1_D2	HB02_P	O	
F	23	AD1_D3	HB02_N	O	
E	21	AD1_D4	HB03_P	O	
E	22	AD1_D5	HB03_N	O	
F	25	AD1_D6	HB04_P	O	
F	26	AD1_D7	HB04_N	O	
E	24	AD1_D8	HB05_P	O	
E	25	AD1_D9	HB05_N	O	
K	28	AD1_D10	HB06_P_CC	O	
K	29	AD1_D11	HB06_N_CC	O	
J	27	AD1_D12	HB07_P	O	
J	28	AD1_D13	HB07_N	O	

Pin#		Signal Name	FMC_LOC	I/O	Remarks
F	28	AD1_D14	HB08_P	O	
F	29	AD1_D15	HB08_N	O	
K	25	AD1_DCO	HB00_P_CC	O	Data Clock
E	27	AD1_OR	HB09_P	O	Over Range
H	22	AD2_D0	LA19_P	O	
H	23	AD2_D1	LA19_N	O	
G	21	AD2_D2	LA20_P	O	
G	22	AD2_D3	LA20_N	O	
H	25	AD2_D4	LA21_P	O	
H	26	AD2_D5	LA21_N	O	
G	24	AD2_D6	LA22_P	O	
G	25	AD2_D7	LA22_N	O	
D	23	AD2_D8	LA23_P	O	
D	24	AD2_D9	LA23_N	O	
H	28	AD2_D10	LA24_P	O	
H	29	AD2_D11	LA24_N	O	
G	27	AD2_D12	LA25_P	O	
G	28	AD2_D13	LA25_N	O	
D	26	AD2_D14	LA26_P	O	
D	27	AD2_D15	LA26_N	O	
D	20	AD2_DCO	LA17_P_CC	O	Data Clock
C	26	AD2_OR	LA27_P	O	Over Range
G	34	BS_CLK_SEL	LA31_N	I	
G	33	BS_CLK1	LA31_P	I	
H	7	DA0_B0	LA02_P	I	
H	8	DA0_B1	LA02_N	I	
G	9	DA0_B2	LA03_P	I	
G	10	DA0_B3	LA03_N	I	
H	10	DA0_B4	LA04_P	I	
H	11	DA0_B5	LA04_N	I	
D	11	DA0_B6	LA05_P	I	
D	12	DA0_B7	LA05_N	I	
C	10	DA0_B8	LA06_P	I	
C	11	DA0_B9	LA06_N	I	
H	13	DA0_B10	LA07_P	I	
H	14	DA0_B11	LA07_N	I	
G	12	DA0_B12	LA08_P	I	
G	13	DA0_B13	LA08_N	I	
D	14	DA0_B14	LA09_P	I	
D	15	DA0_B15	LA09_N	I	
D	8	DA0_CLK	LA01_P_CC	I	
C	14	DA0_PD	LA10_P	I	
C	15	DA0_SEL0	LA10_N	I	
K	7	DA1_B0	HA02_P	I	
K	8	DA1_B1	HA02_N	I	

Pin#		Signal Name	FMC_LOC	I/O	Remarks
J	6	DA1_B2	HA03_P	I	
J	7	DA1_B3	HA03_N	I	
F	7	DA1_B4	HA04_P	I	
F	8	DA1_B5	HA04_N	I	
E	6	DA1_B6	HA05_P	I	
E	7	DA1_B7	HA05_N	I	
K	10	DA1_B8	HA06_P	I	
K	11	DA1_B9	HA06_N	I	
J	9	DA1_B10	HA07_P	I	
J	10	DA1_B11	HA07_N	I	
F	10	DA1_B12	HA08_P	I	
F	11	DA1_B13	HA08_N	I	
E	9	DA1_B14	HA09_P	I	
E	10	DA1_B15	HA09_N	I	
F	4	DA1_CLK	HA00_P_CC	I	
K	13	DA1_PD	HA10_P	I	
K	14	DA1_SEL0	HA10_N	I	
H	2	PRSNT_M2C	PRSNT_M2C_L	O	= GND
E	15	IN_CLK_SEL0	HA16_P	I	
G	37	IN_CLK_SEL1	LA33_N	I	
K	22	PLL_LOCK	HA23_P	O	
J	21	PLL_MON	HA22_P	O	
K	19	PLL_NCS	HA21_P	I	
K	20	PLL_NRST	HA21_N	I	
K	23	PLL_SCLK	HA23_N	I	
J	22	PLL_SDIO	HA22_N	I/O	
D	30	TDI	TDI	I	
D	31	TDO	TDO	O	Loop Back from TDI
E	39	VADJ	VADJ	I	= 2.5V, 3.3V
F	40	VADJ	VADJ	I	= 2.5V, 3.3V
G	39	VADJ	VADJ	I	= 2.5V, 3.3V
H	40	VADJ	VADJ	I	= 2.5V, 3.3V
J	39	VIO_B_M2C	VIO_B_M2C	O	= VADJ
K	40	VIO_B_M2C	VIO_B_M2C	O	= VADJ

7. Environment

Subjects	Specifications		Description
Power Supply Voltage			
FMC HPC Connector	2.5V, 3.3V		
	3P3V,	3.3V ±5%	
	VADJ	2.5V, 3.3V ±5%	
	12P 0V	Not Used	
	3P3V AUX	3.3V ±5%	
Temperature, Humidity			
Temperature	0℃～50℃ (32℉～122℉)		
Humidity	20-90%RH Non-Condensation		