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VF365

Arria® 10 SoC FPGA module with multicore DSP and FMC for high-performance IO intensive applications

OpenVPX

FMC™

SPECIFICATIONS

Processing FPGA

- Arria® 10 SoC family SX Device variants - 570 / 660
- HPS: Dual-core ARM Cortex-A9 MPCore processor @ 1.2 GHz
- Embedded device memory - 36 / 43 Mb
- Embedded device multipliers (18x18) - 3,036 / 3,374
- DDR3 and QDRII+ external memory
- Up to 4GB DDR3 @ 1600MT/s (64-bit bank)
- Up to 64MB QDRII+ SRAM @ 450MHz (two 36-bit banks)

Digital Signal Processor

- Ti KeyStone Multicore C667x family of processors
- Up to 8 cores @ 1.25 GHz
- External memory: Up to 2 GB DDR3 @ 1333 MT/S

FPGA Mezzanine Card (FMC)

- 10x High-Speed Serial Interface lanes (≥ 10Gbps)
- LVDS interface on LA and HA (58 pairs TBC)

VPX Interface

- Comply with OpenVPX MOD3-PAY-3F2U-16.2.12-2 profile
  - PCIe Gen2 Data plane (3x Fat Pipes)
  - GigE 1000BASE-BX Control plane (2x Ultra-Thin Pipes)
  - Payload module with System Controller capability
- Supports FPGA configurable User I/O on P2
  - 24x single-ended 2.5V or 3.3V LVCMOS I/Os
  - 10x High-Speed Serial Interface lanes (≥ 10Gbps)

Software & Firmware Support

- Board support package with reference application
- Linux PCIe drivers
- FPGA Firmware reference design

The **VF365** is a 3U OpenVPX module that leverages on Intel Arria® 10 SoC FPGA and Texas Instruments KeyStone Multicore DSP technology to provide an ultra-high bandwidth processing platform, ideally suited for computation and bandwidth intensive applications such as Radar, SIGINT, EW, SDR, Networking and Video.

The **Arria® 10** SoC high-performance FPGA fabric provides abundant logic, internal memory and floating-point DSP resources for demanding applications in the industrial, aerospace and other markets.

The hard processor system (HPS) with **dual-core ARM Cortex-A9** MPCore processor, on-chip cache, system peripherals and hard memory interfaces provides additional software processing, tightly coupled with the FPGA through high-performance AXI bus bridges.

Connected to the FPGA are dedicated **DDR3 and QDRII+ memories** for algorithms with high bandwidth and/or large memory size requirements. **High-speed serial interfaces** to the OpenVPX data plane and the FMC site creates extremely high FPGA IO throughput capability.

The **multicore DSP** from Texas Instruments provides the flexibility to perform complex post processing functions suitable for the processor domain. High bandwidth communication between the DSP and FPGA is provided through both PCIe and Serial Rapid IO (SRIO) interfaces.

The **VF365** acts as an FMC carrier to provide a modular solution that accommodates a wide range of I/O requirements.

The **VF365** conforms to the OpenVPX standard and operates as a Payload module with System Controller capability. Both air-cooled and conduction cooled versions are available. Further flexibility is provided through build options to cater for different FPGA sizes from Intel's Arria® 10 SX device family.

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Companion Modules

- VR300 Test RTM with USB-Blaster II, XDS100 and Ethernet
- FM500 Test FMC
  - Board Management JTAG and USB serial port
  - FPGA USB-Blaster II and DSP XDS100
- FM550 Two Channel mini-SAS I/O FMC
- FM510 Video IO FMC

Typical Applications

- Radar (Digital Front-end, Doppler filter, Pulse compression, CFAR)
- Spectrum analysis in EW (Signal detection & classification, jammer control)
- Video and image processing (Overlay, DCT, 1D/2D convolution)
- Software Defined Radio (SDR)
- Real-time DSP functions (DDC, FFT, FIR, NCO, etc.)

Ordering Information

Generic order code = VF365-A-B-CcD-ExF-G-Hv-IJ

A: FPGA (SX057, SX066)
B: Speed grade (2 to 4) for Transceiver speed, (C or I)
Commercial/Industrial temp, (1 to 3) FPGA speed, Power (H, S or L)
C: DSP (1, 2, 4 or 8) for TMS320C667X number of cores
D: DSP (1 | 1.25) GHz DSP clock speed
ExF: DDR3 (1 | 2) GB DSP memory, (1 | 2 | 4) GB FPGA memory
G: QDRII+ (16 | 32 | 64) MB total QDRII+ FPGA memory as two x36 banks
(each bank is 2M | 4M | 8M x36)
H: (2.5 | 3.3) Volt for X24s VPX P2 IO voltage
I: THERMAL (0 | 1) for air-cooled or conduction cooled
J: Conformal Coating (0 | 1) for un-coated or coated

Standard order code = VF365-SX057-4I3S-8c1.25-2x2-16-2.5v-00

- SX **570** FPGA **4I3** speed grade with **standard power** option
- TMS320C6678 **eight core** DSP at **1.25 GHz** clock speed (TBC)
- DDR3 = **2GB DSP** memory, **2GB FPGA** memory
- QDRII+ = **16MB total** (two 2M x36 banks) FPGA memory (TBC)
- **2.5V IO** Voltage on VPX P2
- Air-cooled, un-coated

Contact factory for other order options

Block Diagram