



User Guide

FMC-SDR400D Module

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REVISION HISTORY

Revision	Comments	Originator	Date
0.1	Initial Revision	RC	Nov. 9th, 2022
0.2	Added Images, Links, Edits	RC	Dec. 1 st , 2022
0.3	Changed OCXO frequency; corrected some values	KMA	Dec 2 nd , 2022
0.4	Final review and edit	NN	Dec 9 th 2022
0.5	Added Reset Signal for AD9361 to Pinout table, changed hyperlink in introduction, table 3.3 hyperlink corrected	RC	Dec 12 th 2022

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1 INTRODUCTION

The FMC-SDR400D is a conduction cooled FMC card with 2x2 channels of 12 bit DACs and ADCs from Analog Devices (AD9361). The digital interface is provided over high-speed serial links through the FMC connector. This module is suitable for applications such as the prototyping and development of software defined radio systems, point-to-point communication systems, femtocell/picocell/microcell base stations, and general-purpose radio systems. The card is designed to work with the VPX3-ZU1B carrier card and Sundance DSP's PCIe104z or S120 but can also work with other FMC carrier cards. Please contact Sundance Technical Support for more information.

1.1 Hardware features

The hardware has the following features:

1. FMC LPC connector for interfacing with an FPGA carrier card
2. All electrical signals comply with the Vita 57.1 FMC standard
3. 5 SSMC RF connectors (7110-1511-000)
 - 2 RX connectors
 - 2 TX connectors
 - 1 Reference clock connector
4. RF Input specifications:
 - 50-Ohm impedance, single ended
 - Input frequency range 0.1 GHz – 6 GHz, input Bandwidth –up to 56 MHz
 - Gain nonlinearity – ± 3 dB*
 - Channel gain mismatch – max 1 dB*
 - Return loss ≥ 6 dB*
 - Maximum allowable input power – 20 dBm
5. Input LNA [HMC8410LP2FE](#); NF = 1.6 (0.3 to 3 GHz); Gain ≤ 17.5 dB (parameters from IC datasheet)
6. Input tuneable attenuator is HMC624A
7. RF Output specifications:
 - 50-Ohm impedance, single ended
 - Output frequency range 50MHz – 6 GHz, TX EVM ≤ -40 dB
 - Maximum output power 28 dBm at 800 MHz, 26 dBm at 2.4 GHz
 - Gain nonlinearity – ± 4 dB*
 - Channel gain mismatch – 1 dB max*
8. TX path contains a 22 dB TX amplifier ADL5611
9. External reference clock input range – 10 – 80 MHz
10. Internal 20 MHz OCXO, ± 100 ppb, option to be used as a 20 MHz TCXO
11. Maximum Power consumption:
 - 12V – Max 0.6A
 - 3V3 – Max 0.1A
 - VADJ – Max 1A
12. VADJ supported - 1.8V, 2.5V
13. FMC_LA[00...28+], FMC_CLK[0,1] – FMC lanes required from the carrier card

*All RF parameters get from post layout simulation, not from real board. Parameters valid via 0.1 – 6 GHz range.

1.2 Board limitations and notes.

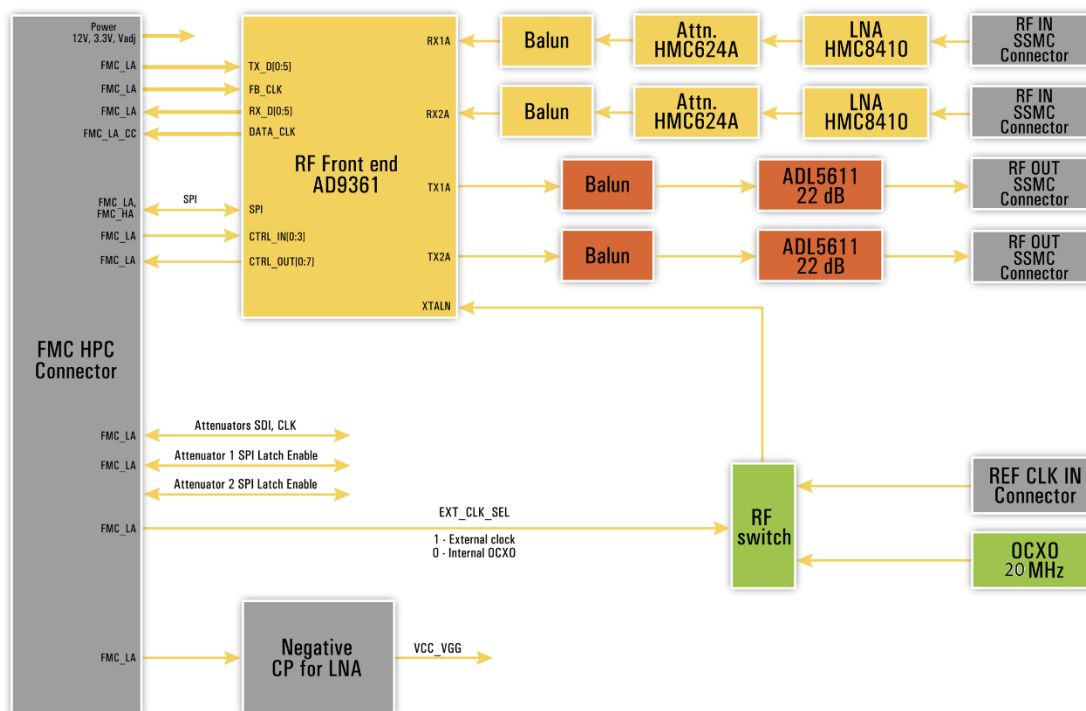
1. **Warning!!!** RF inputs, connected directly to the ADC can damage hardware, it is the user's responsibility to protect and to NOT overload the ADC inputs.

2. The RF input LNA requires a special power up and power down sequence, see chapter 2.4

3. Operation with VADJ 2.5 is not recommended in high ambient temperatures, due to higher heat dissipation.

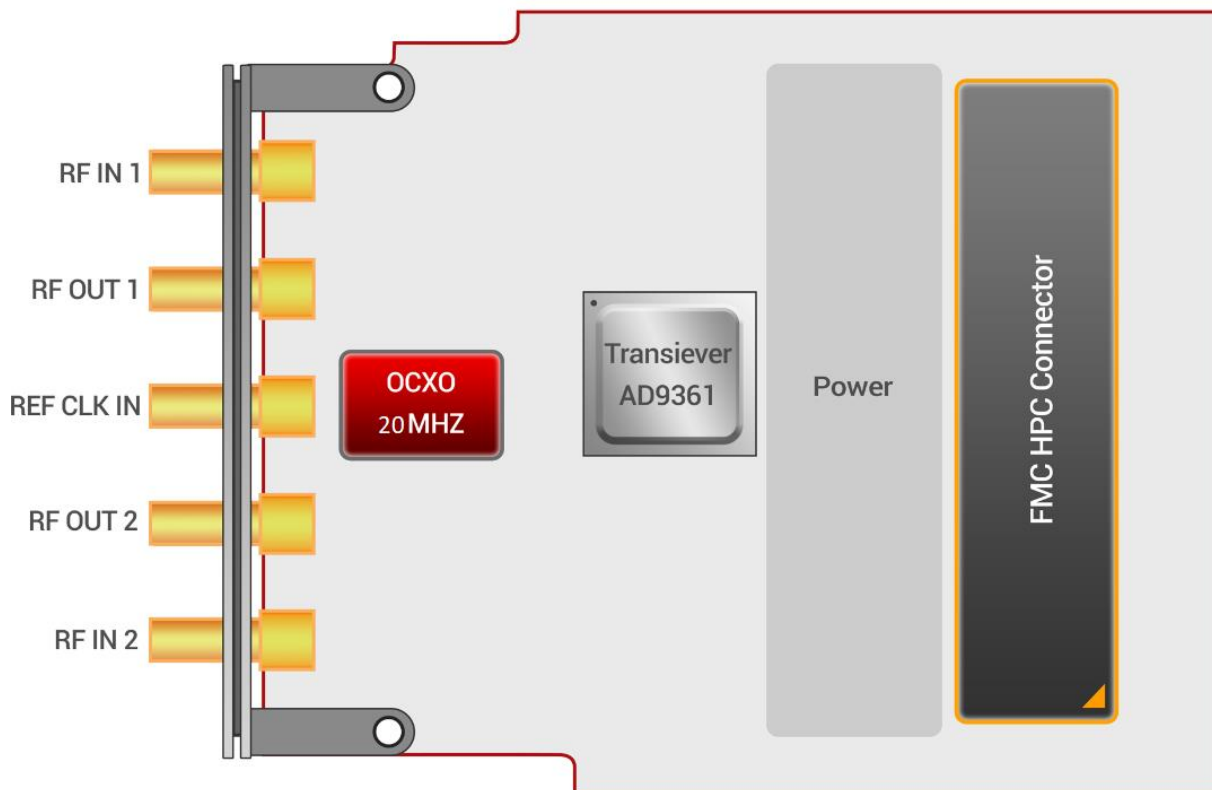
2 BOARD DESCRIPTION

2.1 Block Diagram

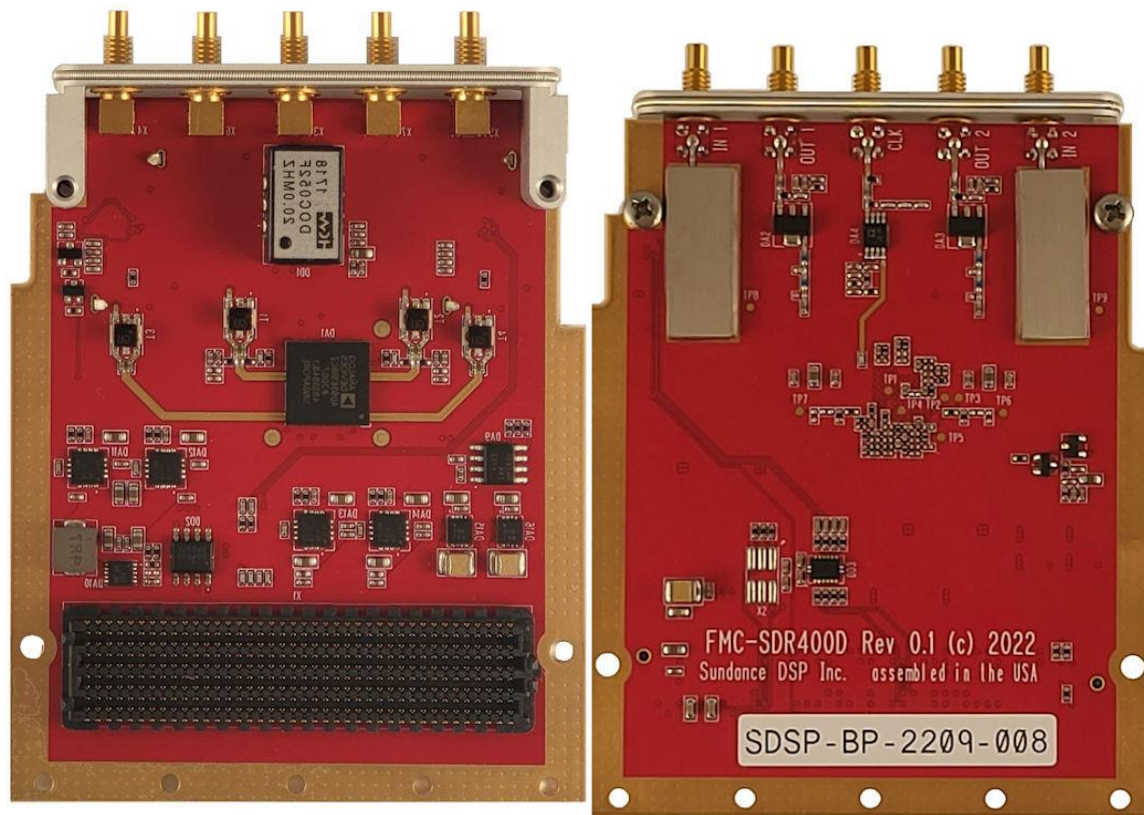


2.2 Board Images

2.2.1 FMC-SDR400D Placement



2.2.2 FMC-SDR400D Images



2.3 FMC LPC

A low pin count FMC connector is used to interface the ADC/DAC data to the carrier card. The ADC uses high speed serial links to transfer the data. The LA bank is used for the SPI interface and other controls to configure the ADC/DAC. The card is fully compliant with Vita 57.1 specifications.

2.4 RF Agile Transceiver (AD9361)

FMC-SDR400P uses an AD9361 RF Agile Transceiver from Analog Devices. AD9361 is a high-performance RF transceiver suitable for 3G, 4G base station applications. The device combines an RF front-end with a flexible mixed signal baseband section and integrated frequency synthesizers. The AD9361 receiver operates from 70 MHz to 6 GHz and the transmitter LO operates from 47 MHz to 6 GHz and supports a channel bandwidth from less than 200 KHz to 56 MHz

The key features of the transceiver are given below:

Receive:

- Supports up to 2 direct conversion RF receive channels
- Input frequency range: 70 – 6000MHz
- Input Gain: 0 to 72 dB, gain step 1 dB
- Noise figure: 2 dB at 800MHz, 3 dB at 2400MHz, 3.8 dB at 5500MHz
- Channel isolation: 70 dB at 800MHz, 65 dB at 2400MHz, 52 dB at 5500MHz

- Local Oscillator leakage: -122 dB at 800MHz, -110 dB at 2400MHz, -95 dB at 5500MHz
- Third-Order Input intercept point IIP3: -18 dB at 800MHz, -14 dB at 2400MHz, -17dB at 5500MHz
- Fully Integrated synthesizers (Including loop filters)
- Data paths consists of LNA, ADC and digital filters
- AGC, Quadrature calibration and DC offset calibration
- NF: 2.5dB @1GHz
- Digital filters: 128 complex taps, decimation between 2 and 48
- On-chip sensor for temperature-corrected RSSI

Transmit:

- Supports up to 2 RF transmit channels
- Fully Integrated synthesizers (Including loop filters)
- Data path consists of digital filters, DAC, and modulators
- Digital filters: 128 complex taps, interpolation between 2 and 48
- Resolution: 12-Bit
- Output power control range: 90 dB
- Output power maximum: 8 dBm
- Output frequency range: 70 – 6000 MHz
- Channel isolation: 50 dB at 800MHz, 50 dB at 2400MHz, 50 dB at 5500MHz
- TX EVM \leq - 40 dB
- Power Dissipation: max 1.5W

For more information, please refer to the link below

https://www.analog.com/media/en/technical-documentation/data-sheets/AD9631_9632.pdf

2.5 Clock Distribution

This board has an OCXO or a TCXO (as build option) and has a connector to provide an external user clock.

Note: When an external reference input is selected, the power to the OCXO (or TCXO) is turned OFF. When going back to using the internal clock, the OCXO needs time to warm up, approximately 60 seconds (at 25C ambient temperature).

There is a SYNC signal that connects both transceiver ICs, this signal is used for synchronizing the internal clocks in the ICs.

All 4 channels are coherent, and all the transceiver ICs use the same reference clock. This allows for the module to be used in applications that require coherent receiving and transmitting.

2.6 External Clock Input

The external clock input is used to feed a sampling clock directly to the AD9361 module via an SSMC connector. The clock input parameters are given below:

- Input type: AC – coupled, single ended

- Input impedance: 50 Ohm
- Frequency range: 10 – 80 MHz
- Maximum input voltage – 1.4V peak-peak single ended

2.7 Dimensions

- Weight: 45G
- Vita 57.1 form-factor

3 OPERATION

The FMC module is operational when it is populated on an FPGA carrier card. Initialization of the Transceiver, ADC/DAC, and clock are configured via the SPI interface over the FMC connector. The following factors need to be considered for proper operation of the module

3.1 AD9361 part parameters from the datasheet

3.1.1 Transmitter section

- Resolution: 12-Bit
- Output power control range: 90 dB
- Output power maximum: 8 dB
- Output frequency range: 70 – 6000 MHz
- Channel isolation: 50 dB at 800MHz, 50 dB at 2400MHz, 50 dB at 5500MHz
- TX EVM \leq - 40 dB
- Power Dissipation: max 1.5W

3.1.2 Receiver section

- Input frequency range: 70 – 6000MHz
- Input Gain: 0 to 72 dB, gain step 1 dB
- Noise figure: 2 dB at 800MHz, 3 dB at 2400MHz, 3.8 dB at 5500MHz
- Channel isolation: 70 dB at 800MHz, 65 dB at 2400MHz, 52 dB at 5500MHz
- Local Oscillator leakage: -122 dB at 800MHz, -110 dB at 2400MHz, -95 dB at 5500MHz
- Third-Order Input intercept point IIP3: -18 dB at 800MHz, -14 dB at 2400MHz, -17dB at 5500MHz

3.1.3 TX AMPLIFIER IC parameter

- At 140MHz
 - Gain – 18.9 dB
 - Output 1 dB Compression Point – 16.3 dBm
 - NF – 3.3 dB
- At 900 MHz
 - Gain – 22.2 dB
 - Output 1 dB Compression Point – 21 dBm
 - NF – 2.1 dB
- At 2140 MHz
 - Gain – 21.2 dB
 - Output 1 dB Compression Point – 20.6 dBm
 - NF – 2.6 dB
- At 3500 MHz

- Gain – 20.3 dB
- Output 1 dB Compression Point – 17.4 dBm
- NF – 3.1 dB
- At 5000 MHz
 - Gain – 16.3 dB
 - Output 1 dB Compression Point – 16 dBm
 - NF – 4.4 dB
- At 5800 MHz
 - Gain – 14.3 dB
 - Output 1 dB Compression Point – 12.8 dBm
 - NF – 6 dB

For more information, please visit the AD9361 User Guide (Section 2.4 of this document).

3.2 LNA Power Sequencing

The input stage includes an LNA. This LNA requires a special sequence for powering on/off. The following two signals drive the LNA power supply:

Signal	Comment
LNA_PWR_ON	Main power to LNA, default is OFF
VGG1_SET_-2V	In(PU10k) Drives the bias voltage of LNA, default is -2.5V

Note: See section 4.1 for the pinout of the signals on the FMC connector

3.2.1 LNA power ON sequence

1. LNA_PWR_ON and VGG1_SET_-2V signals must be at default states, or at Hi-Z without pull-ups
2. Turn on the main LNA power by applying LNA_PWR_ON – “1”
3. Change the bias voltage to -0.55V, by driving “0” to VGG1_SET_-2V

3.2.2 LNA power OFF sequence

1. Change the bias voltage to -2V, by driving “1” to VGG1_SET_-2V, or by switching the buffer to a hi— state, with NO pull down
2. Turn off the main LNA power, by applying LNA_PWR_ON – “0”
3. Change the bias voltage to -0.55V, by driving “0” to VGG1_SET_-2V
4. Turn off board or supplies

3.3 Clocking and Synchronization

The board carries an OCXO or a TCXO (as a build option), and has a connector to provide an external user clock.

Please note, when the user chooses an external reference input, power to OCXO (or TCXO) is always ON.

For detailed clock path, see [FMC-SDR400D Block Diagram](#)



Note: See section 4.1 for the pinout of the signals on the FMC connector

3.4 ESD Protection

ESD protection is provided by components intended for use with high-speed signals with minimum impact on signal quality.

3.5 VADJ

FMC-SDR400D supports VADJ voltages: 1.8V, 2.5V. Contact Sundance DSP customer support for the VADJ voltage supported by your carrier card.

Note: Customers should make sure their carrier card supports one of the above VADJ voltages to work with this module.

3.6 Operating Sequence

To initialize the module to an operating state, use the following procedure

1. Connect the module to an appropriate carrier card with the right VADJ voltage mentioned above.
2. Program AD9361 transceiver and integrated ADC's and DAC's via the SPI interface
3. Power up the LNA's
4. Capture the data from the receiver, process it, and transmit it

4 PINOUTS

4.1 FMC connector pinout

AD9361

Net name (AD9361 pin name)	Dir	FMC Pin	FMC pair name	Comment
CTRL_IN0	IN	C15	FMC_LA10-	Used for manual RX and TX attenuation control
CTRL_IN1		C14	FMC_LA10+	
CTRL_IN2		D14	FMC_LA09+	
CTRL_IN3		D15	FMC_LA09-	
CTRL_OUT0	OUT	G13	FMC_LA08-	Various purposes
CTRL_OUT1		G15	FMC_LA12+	
CTRL_OUT2		G16	FMC_LA12-	
CTRL_OUT3	OUT	G12	FMC_LA08+	Various purposes
CTRL_OUT4		G19	FMC_LA16-	
CTRL_OUT5		H17	FMC_LA11-	
CTRL_OUT6		H16	FMC_LA11+	
CTRL_OUT7		G18	FMC_LA16+	
EN_AGC	IN	H19	FMC_LA15+	Manual control of the AGC
ENABLE	IN	H20	FMC_LA15-	Control input to IC
TXNRX	IN	C26	FMC_LA27+	“1” – TX, “0” – RX data bus mode
RECEIVE DATA PATH				
DATA_CLK_P	OUT	H4	FMC_CLK0_ M2C+	Clock to the Carrier
DATA_CLK_N		H5	FMC_CLK0_ M2C-	
RX_FRAME_P		D20	FMC_LA17_ CC+	Valid data indicator, or the start of the frame
RX_FRAME_N		D21	FMC_LA17_ CC-	
RX_D0_P	OUT	H25	FMC_LA21+	Received data output to the carrier
RX_D0_N		H26	FMC_LA21-	
RX_D1_P		G24	FMC_LA22+	
RX_D1_N		G25	FMC_LA22-	
RX_D2_P		D23	FMC_LA23+	
RX_D2_N		D24	FMC_LA23-	
RX_D3_P		C22	FMC_LA18+	
RX_D3_N		C23	FMC_LA18-	
RX_D4_P		H22	FMC_LA19+	
RX_D4_N		H23	FMC_LA19-	
RX_D5_P		G21	FMC_LA20+	
RX_D5_N		G22	FMC_LA20-	
TRANSMIT DATA PATH				

FB_CLK_P	IN	G6	FMC_LA00_ CC+	Looped version of DATA_CLK, provided by the Carrier
FB_CLK_N		G7	FMC_LA00_ CC-	
TX_FRAME_P		D8	FMC_LA01_ CC+	Valid data indicator, or the start of the frame
TX_FRAME_N		D9	FMC_LA01_ CC-	
TX_D0_P		H7	FMC_LA02+	Transmitted data from the carrier
TX_D0_N		H8	FMC_LA02-	
TX_D1_P		G9	FMC_LA03+	
TX_D1_N		G10	FMC_LA03-	
TX_D2_P		H10	FMC_LA04+	
TX_D2_N		H11	FMC_LA04-	
TX_D3_P		C10	FMC_LA06+	
TX_D3_N		C11	FMC_LA06-	
TX_D4_P		D11	FMC_LA05+	
TX_D4_N		D12	FMC_LA05-	
TX_D5_P		H13	FMC_LA07+	
TX_D5_N		H14	FMC_LA07-	

***Direction is related to the FMC mezzanine (IN – the signal comes from the carrier to the mezzanine, Out – the signal comes from the mezzanine to the carrier)**

Control Signals for the AD9361

Net name	Direction	FMC Pin	FMC pair name	Comment
AD_SPI_DI	In	D26	FMC_LA26+	SPI Data input
AD_SPI_DO	Out	H29	FMC_LA24-	SPI Data Output
AD_SPI_CLK	In	G27	FMC_LA25+	SPI Clock
AD_SPI_CS#	In (PU10k)	H28	FMC_LA24+	SPI chip select
AD_RST#	In	G28	FMC_LA25-	AD9361 Reset Signal

SPI Control Signals for the HMC624A Input Attenuators

Net name	Direction	FMC Pin	FMC pair name	Comment
ATT_SPI_DIN_VADJ	In	C19	FMC_LA14-	Data input to the attenuators
ATT_SPI_CLK_VADJ		C18	FMC_LA14+	Clock for the attenuators
ATT1_SPI_LE_VADJ		D18	FMC_LA13-	Latch Enable for the attenuators. IF High - DIN ignored.
ATT2_SPI_LE_VADJ		D17	FMC_LA13+	

				Must be toggled from 0 to 1 to the new latch value.
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Control Signals for the LNA

Net name	Direction	FMC Pin	FMC pair name	Comment
LNA_PWR_ON	In(PD10k)	C27	FMC_LA27-	Main power to LNA, default is OFF
VGG1_SET_-2V	In(PU10k)	D27	FMC_LA26-	Drives bias voltage of LNA, default is -2.5V

Clock Select Signal

Net name	Dir	FMC Pin	FMC name	Comment
CLKSEL_EXT/INT#	IN(PD10k)	H31	FMC_LA28+	“1” – selects external clock, “0” – selects an internal clock source

4.2 EEPROM Programming Connector Pinout (X2)

Signal Name	X2 Pin	FMC Signal (if relevant)
WP	1	
VCC_3V3_AUX_FMC	2	
SCL	3	FMC_SCL
GND	4	
SDA	5	FMC_SDA
GND	6	

5 SIMULATION DATA SECTION

5.1 TX Path simulation results

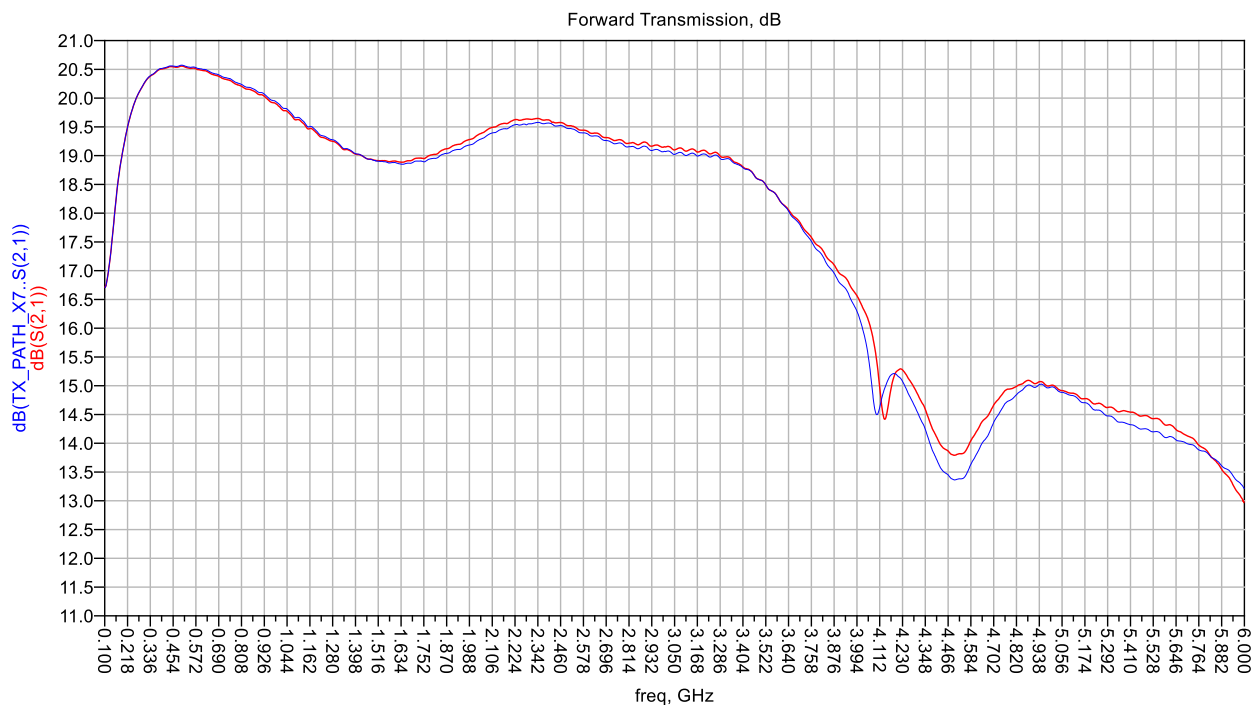


Figure 1. S21 POST layout parameters, red –channel 1, blue – channel 2.

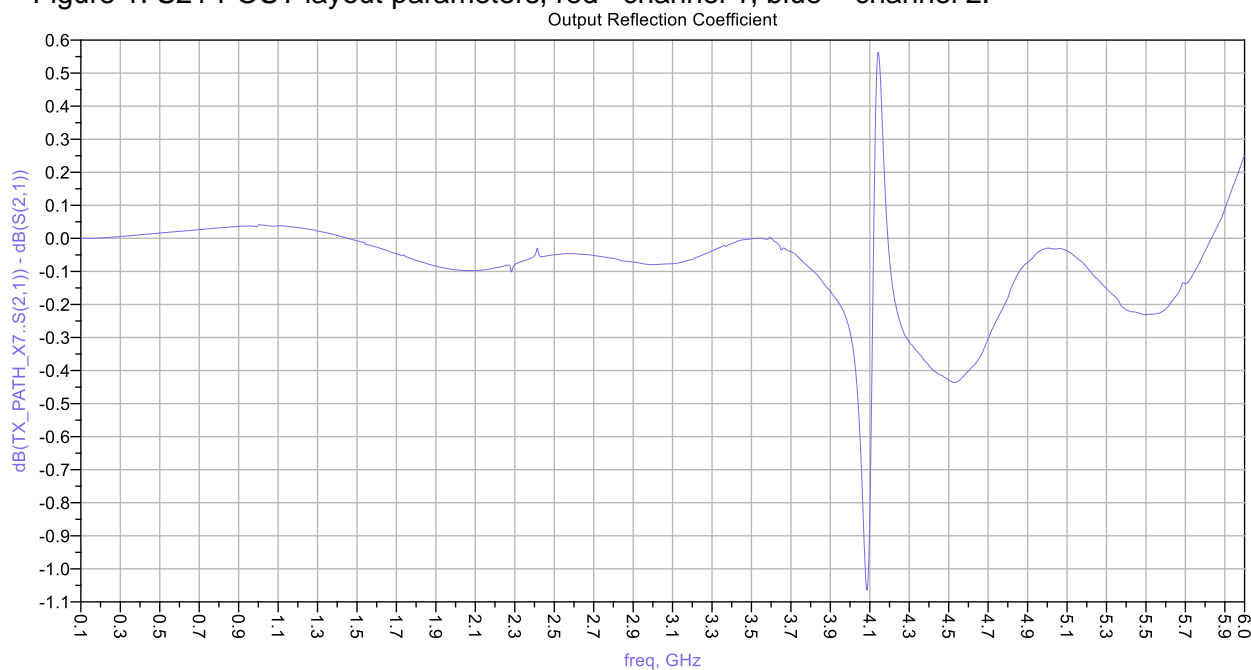


Figure 2. TX S21 channel difference dB(ch. 2) – dB(ch. 1)

5.2 RX Path simulation results

Rx path results simulated with 3.5 dB attenuator setting.

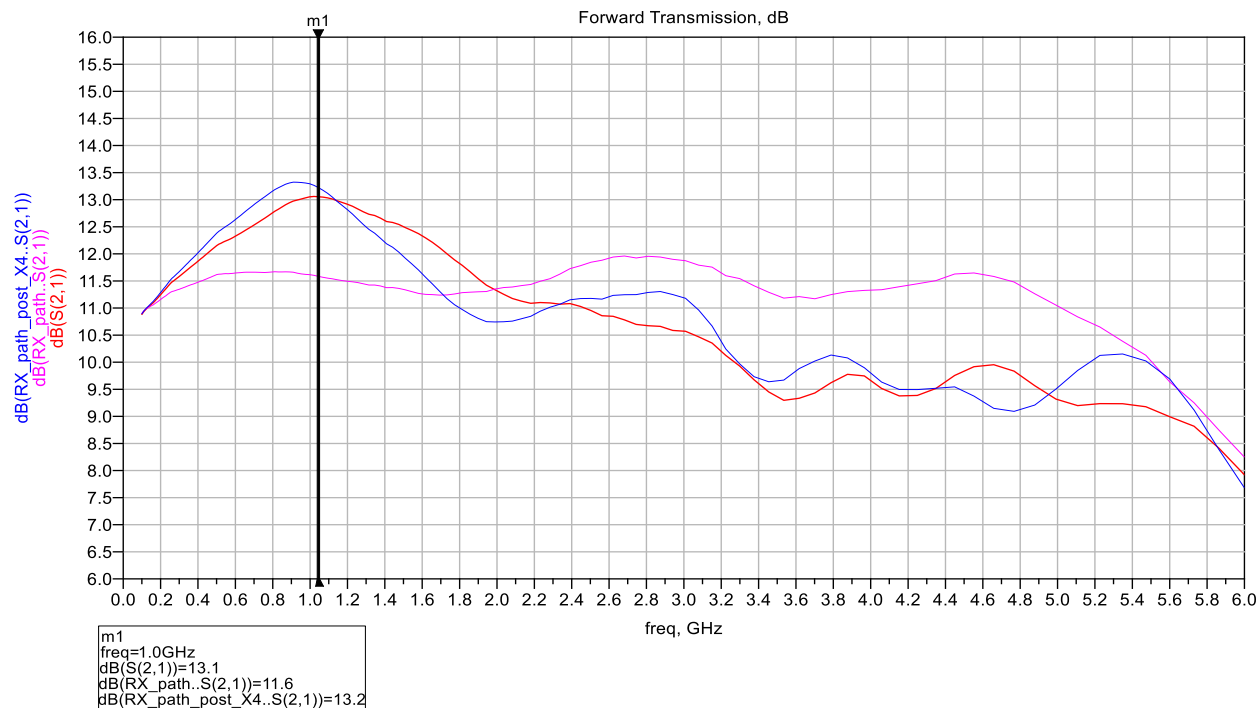


Figure 3. S21 POST layout parameters, red – channel 2, blue – channel 1, pink – PRE layout S21.

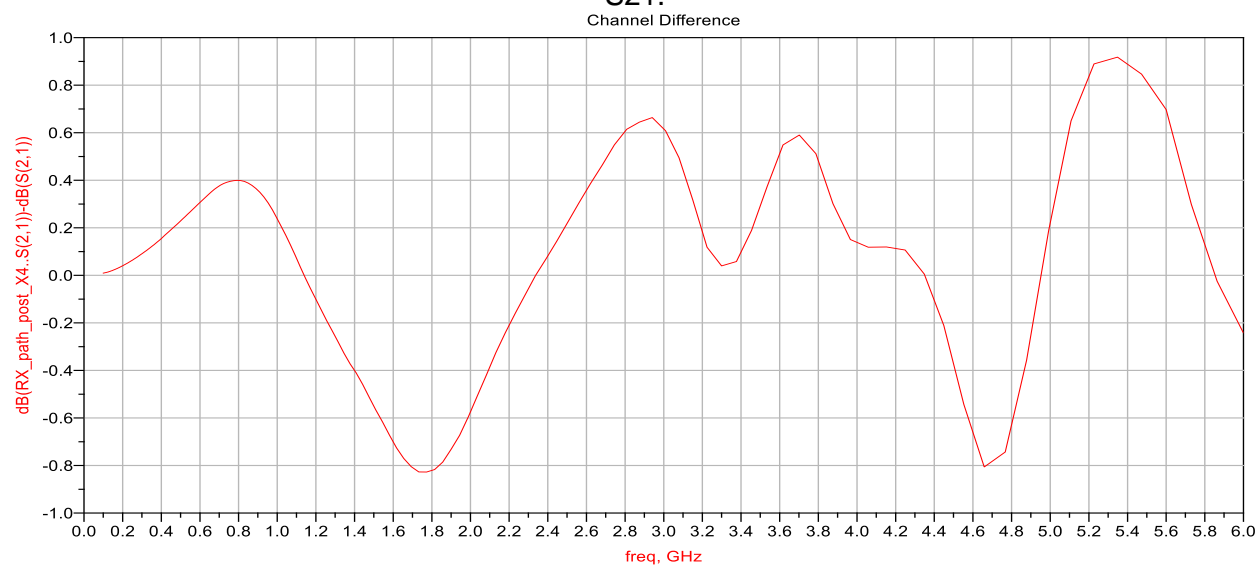


Figure 4. S21 channel difference dB(ch. 1) – dB(ch. 2)

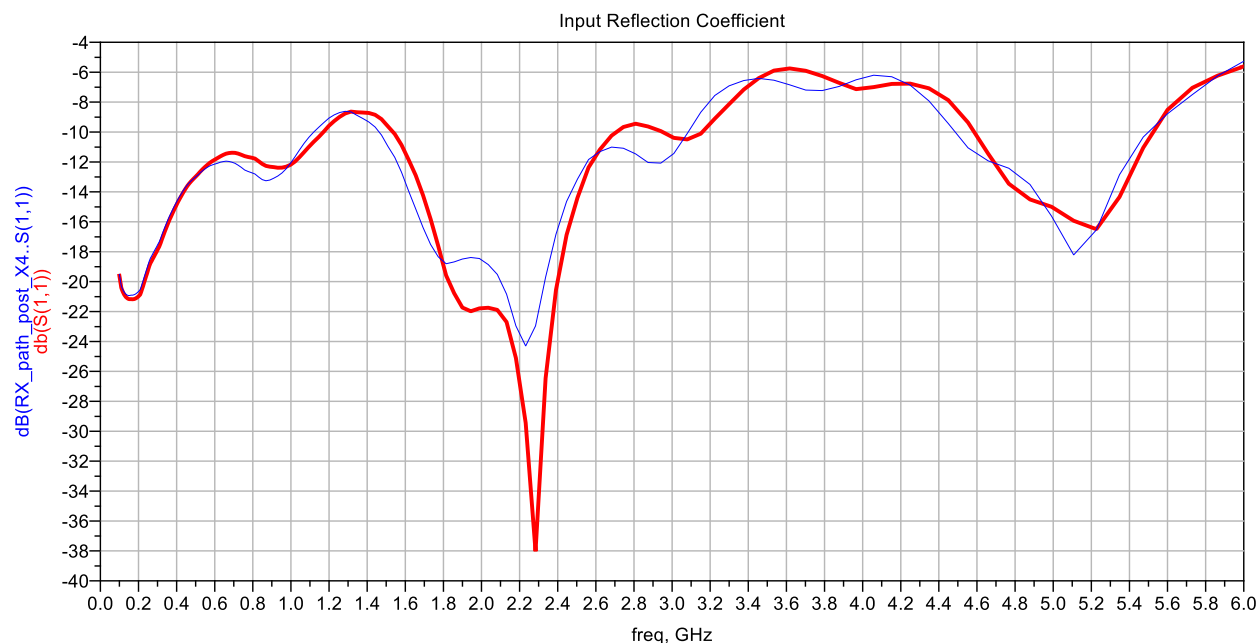


Figure 5. S11 POST layout parameters, red – channel 2, blue – channel 1.

6 BOARD SUPPORT PACKAGE

FMC-SDR400D board support package is available using an FPGA carrier card as reference design:

1. **PCIe104z** carrier card (Zynq Ultrascale + MPSoC board from Sundance DSP Inc.)

Note: The FMC-SDR400D can be used by any Vita 57.1 compliant carrier cards with the ability to assert the correct VADJ values via firmware.

7 COOLING

User must make sure that adequate air flow and cooling is provided for using this module and/or make use of its conduction cooling feature.

8 SAFETY

The module presents no hazard to the user.

9 EMC

The module is designed to operate within an enclosed host system that provides adequate EMC shielding. Operation within the EU EMC guidelines is only guaranteed when the module is installed within an appropriate host system. The module is protected from damage by fast voltage transients introduced along output cables from outside the host system. Short-circuiting any output to ground does not cause the host PC system to lock up or reboot.



10 ORDERING INFORMATION

FMC-SDR400D-xx

Where xx= means TXCO is installed, blank means no TXCO installed

11 SUPPORT

For technical support please either call Sundance DSP on +1-(775)-827-3103 or write to support@sundancedsp.com