Unit / Module Description:	4, 8 or 16 Channels ADC @ 125MHz on an FMC Module – 12/14-bits – LPC or HPC
Unit / Module Number:	SMT-FMC116-xxx
Document Issue Number:	1.2
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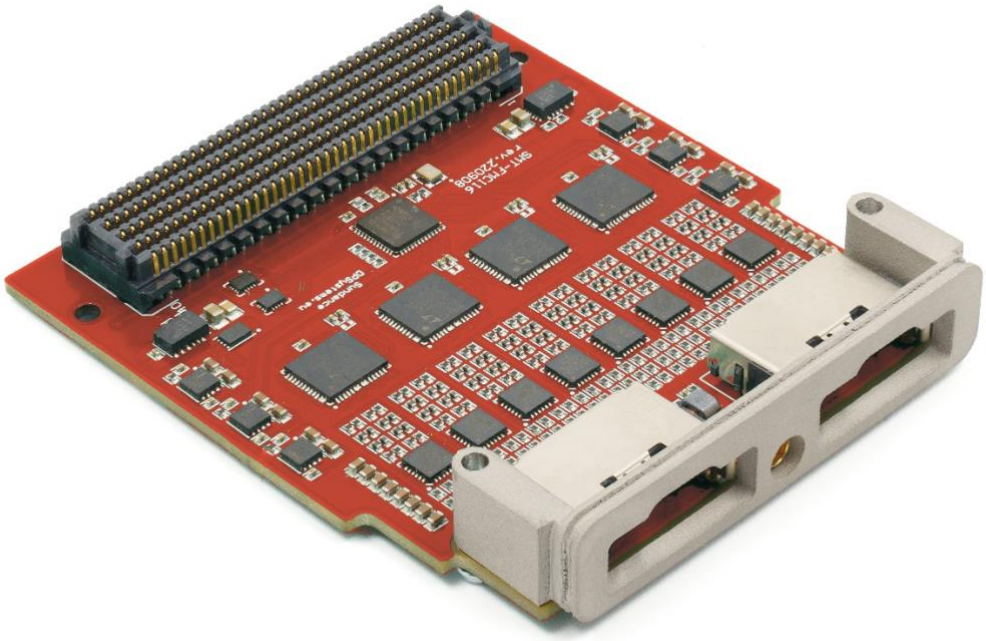
Product Specification for *SMT-FMC116*



LPC/HPC FMC Module
4, 8 & 16 ADC channels

Revision History

Issue	Changes Made	Date	Initials
1	Initial Version	9.12.2021	WJ
1.1	Added comments	14.12.2021	FC
1.2	Added photos and updated diagrams	26.09.2024	FC

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1 Introduction

The document describes the specification of the SMT-FMC116 module. This is a general-purpose digitizer card equipped with 4, 8, or 16 fully differential channels using 14-bit 125 MSPS ADCs. The module is equipped with dedicated clock distribution and uses the VITA57.1 FMC-HPC standard interface to connect to compatible carrier boards for the 16-channel version and FMC-LPC for the 4 and 8-channel versions.

2 Related Documents

2.1 Referenced Documents

Full details of circuits and datasheet of individual components on request

2.2 Applicable Documents

3 Acronyms, Abbreviations and Definitions

3.1 Acronyms and Abbreviations

ADC - Analog-to-Digital Converter

FMC - FPGA Mezzanine Card

LPC - Low Pin Count

HPC - High Pin Count

SMT - Surface-Mount Technology

MSPS - Mega Samples Per Second

VITA - VMEbus International Trade Association

FPGA - Field-Programmable Gate Array

LVDS - Low Voltage Differential Signaling

PLL - Phase-Locked Loop

Gbps - Gigabits per Second

LED - Light Emitting Diode

ANSI - American National Standards Institute

VHDL - VHSIC (Very High-Speed Integrated Circuit) Hardware Description Language

MTBF - Mean Time Between Failures

EMC - Electromagnetic Compatibility

MHz - Megahertz

SMA - SubMiniature version A (connector type)

3.2 Definitions

To Be Defined Later

4 Functional Description

4.1 Block Diagram

The Figure presents general block diagram of all elements of the board. Individual sub modules are described in more detailed way in next chapters.

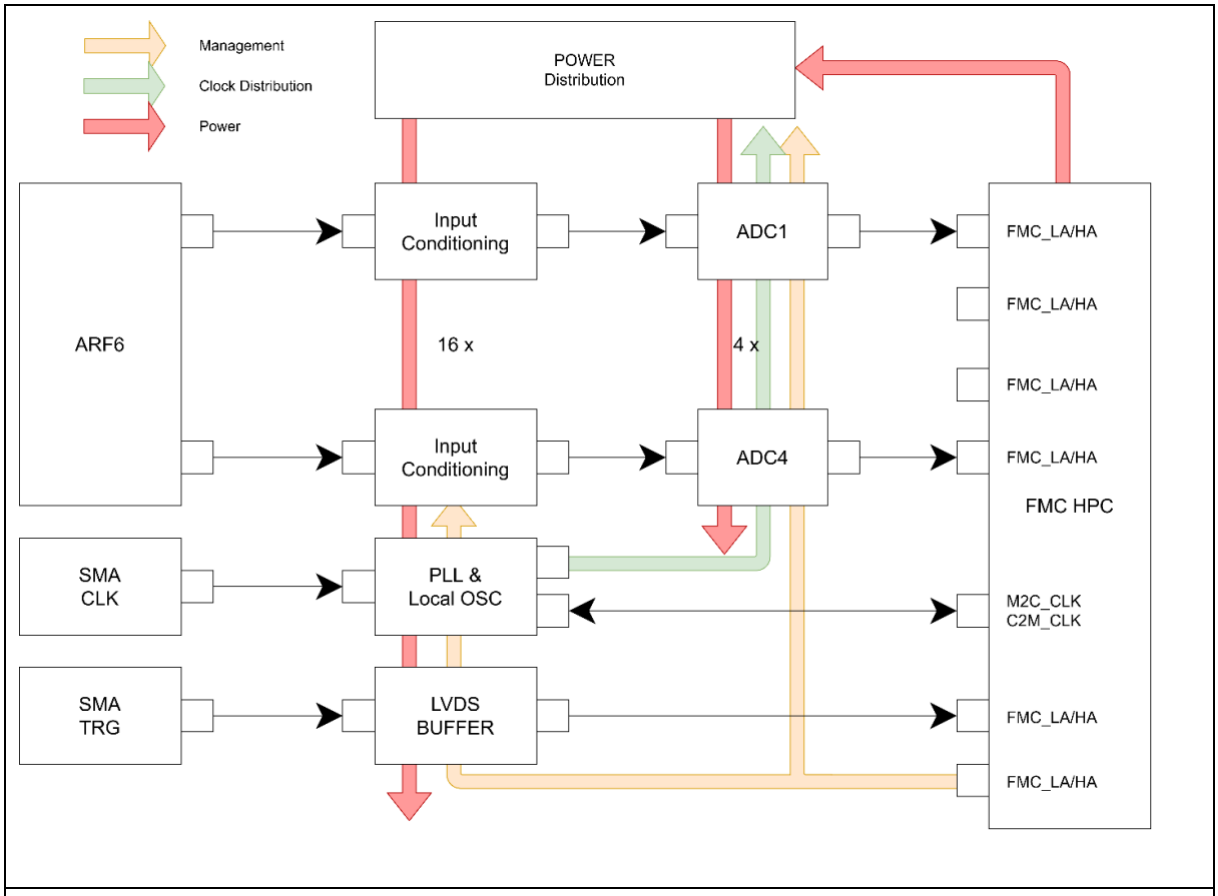

Figure: General block diagram of the board

4.2 Module Description

4.2.1 ARF6-RA AcceleRate® Right-Angle

ARF6-RA is high density Samtec connector, which has performance suitable for analog application. It allows to fit 16 differential channels on a single FMC module. For ease of operation, the dedicated signal adapters are offered as separate product (single ended SMA -> ARF6, differential SMA -> ARF6)

Picture 1 - Samtec ARF6-RA Connector

Full measurement results for attenuation and crosstalk between adjacent channels on request

4.2.2 Clock and Trigger Inputs

The board is equipped with two front-panel SMA connectors. They are used to provide an external signal connection for the clock (routed to the clock distribution part) and trigger (general purpose signal routed to FPGA on the carrier). Both interfaces contain a dedicated signal conditioning stage to adjust their levels to be compatible with clock distribution and FPGA interface (LVDS signalling).

4.2.3 Clock Distribution

The clock distribution part allows the configuration of various aspects of clocking of internal components. First of all, it allows one to select a source clock out of 4 possible sources:

- On board 125 MHz oscillator (frequency adjusted in case of lower sampling options)
- Front Panel Clock connector
- FMC_CLK2_C2M clock generated on the carrier (16-channel version only)
- LA33_P/N data lines (low-performance FPGA generated clock used for debugging and internal tests)

The board is equipped with a dedicated PLL (Analog Devices LTC6951), which can synthesize (based on selected input) the output clock for each ADC (possibility of different frequencies, delays, phases) and output clock for FPGA routed through FMC_CLK0_M2C lines.

4.2.4 ADC

The ADC used on board is LTC2175-14. It provides an efficient data transmission interface (1 Gbps with a small amount of data lines) and the possibility of dynamic reconfiguration of data properties. The ADC family can be easily scaled in terms of resolution (12- and 14-bit versions available) and sampling frequency (can be selected as one of 80, 105, 125).

4.2.5 On-Board LEDs

The board is equipped with a set of 4 diagnostic and 12 general-purpose LEDs. Diagnostic LEDs indicate power supply status and PLL locking information. General purpose ones can be used by user applications to communicate internal status.

4.3 Interface Description

The module is implemented as an HPC FMC-compatible mezzanine (4 and 8-channel versions are LPC compatible without loss of other functionality). The pinout of the interface is presented in Chapter 11.

4.3.1 Mechanical Interface

The mechanical interface is compatible with ANSI-VITA-57-1 – the module is implemented as a single-width FMC module with a standard FMC front panel bezel. The general view of mechanics is presented below.

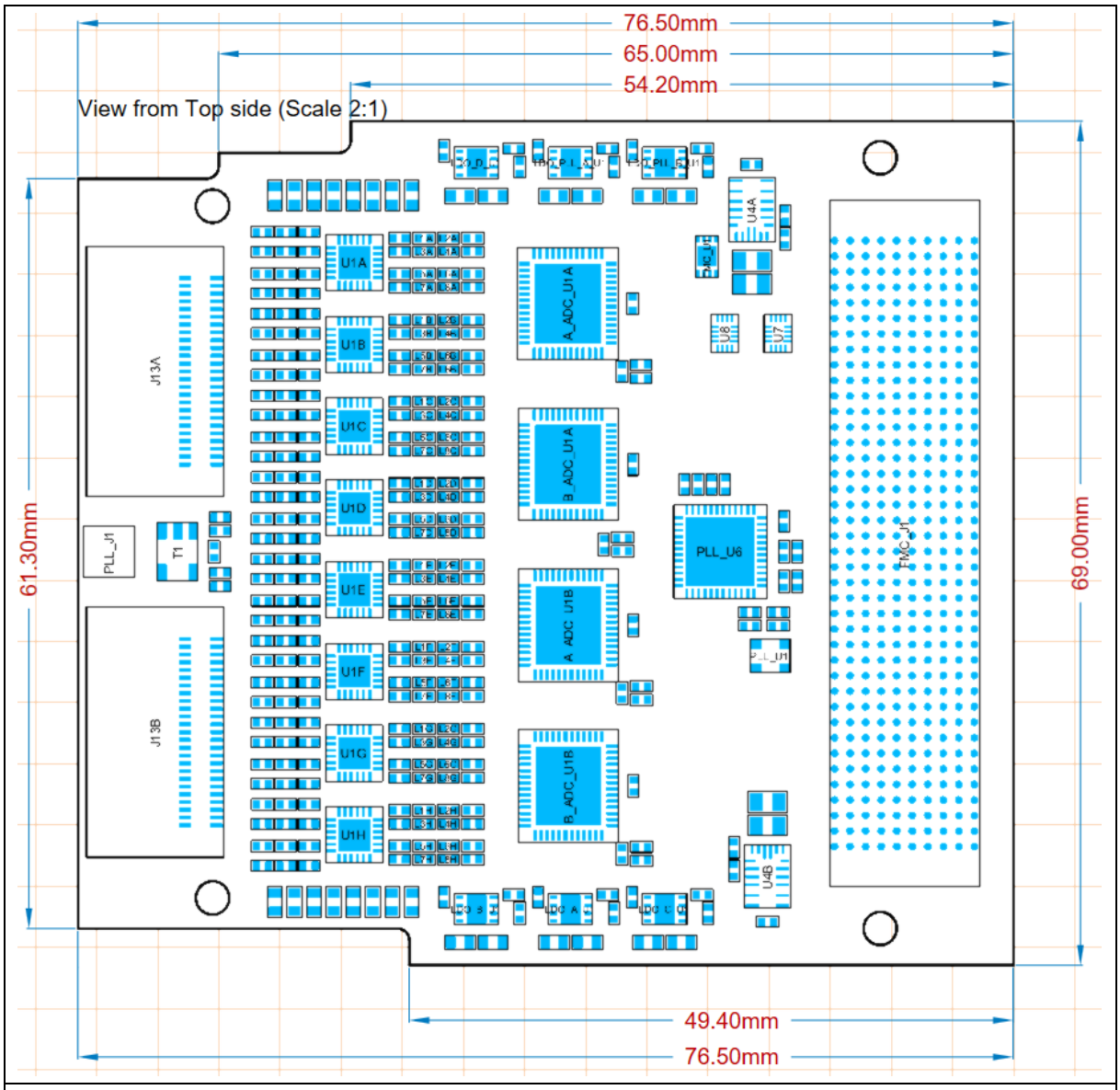

Figure: Mechanical interface

5 Verification Procedures

A comprehensive verification procedure is necessary to ensure that the SMT-FMC116 performs as promised. This process will help confirm that the module meets its design specifications, functions correctly under all intended operating conditions, and reliably interfaces with other components and systems. The suggested verification procedure for the ADC FMC module should include:

1. Preliminary Checks
- Visual Inspection: Conduct a thorough visual inspection of the ADC FMC module for any physical damage, incorrect component placements, solder joint issues, or other manufacturing defects.
- Documentation Review: Verify that the module's documentation (datasheets, user manuals, etc.) is up-to-date and matches the module's hardware and firmware versions.

2. Power-Up and Initialization Testing
- Power Supply Verification: Check that the power supply voltages (e.g., +12V, +3.3V, VADJ) are within the specified range and remain stable during operation.
- Power-On Self-Test (POST): Ensure that the module successfully completes a power-on self-test (if applicable), with all diagnostic LEDs functioning as expected (e.g., power status and PLL lock indicators).
- Current Consumption Check: Measure the power consumption of the module at different stages of operation to ensure it is within specified limits. Check for unexpected current draws that might indicate a short or faulty component.

3. Functional Testing

ADC Performance Validation:

- Input Signal Testing: Apply known analog signals (e.g., sine wave, square wave, and white noise) of varying frequencies and amplitudes to the ADC inputs through the SMA connectors.
- Sampling Rate Verification: Verify the ADC operates at the specified sampling rates (e.g., 125 MSPS, and any lower frequencies if supported) and that the sampling rate can be dynamically adjusted if applicable.
- Resolution Verification: Ensure the ADC outputs digital data at the specified resolution (e.g., 12-bit or 14-bit), and validate that the resolution can be changed if the module supports different configurations.
- Dynamic Range and SNR Testing: Measure the dynamic range and signal-to-noise ratio (SNR) of the ADC using a standard test signal (such as a full-scale sine wave) and verify that these parameters meet or exceed the specifications.

Clock and Synchronization Testing

- Clock Source Selection: Verify the module can select and switch between different clock sources (on-board oscillator, external clock via front panel, FMC_CLK2_C2M, etc.) as described in the specifications.
- PLL Functionality: Test the PLL's ability to synthesize various output frequencies, phases, and delays based on different input clocks. Ensure the PLL locks correctly and that any phase noise or jitter is within acceptable limits.
- Clock Distribution Network: Verify that the internal clock distribution network delivers the correct clock signals to all ADCs and the FPGA interface.

Data Interface Testing

- Data Integrity Check: Use a known test pattern or ramp signal to verify that data captured from the ADC is transmitted accurately to the FPGA or host system without errors or data corruption.
- Interface Compatibility: Confirm that the module's FMC interface (HPC or LPC) functions correctly and is compatible with various carrier boards (e.g., Xilinx Evaluation Boards).
- Signal Quality Assessment: Use an oscilloscope or logic analyzer to inspect the quality of the digital data signals (e.g., LVDS lines) at the FMC interface. Check for proper voltage levels, signal integrity, and timing.

Environmental and Stress Testing

- Thermal Testing: Perform tests at various operating temperatures to ensure the module functions correctly across its specified temperature range. Monitor ADC performance for any degradation (e.g., increased noise or reduced accuracy) at temperature extremes.
- Power Cycling: Repeatedly power-cycle the module to ensure reliable startup and operation without faults or errors.
- Long-Term Stability Testing: Run the module continuously under normal and extreme conditions to test for long-term stability and reliability, looking for signs of drift or failure.

Interference and EMC Testing

- EMC Compliance: Test the module in a shielded environment to ensure it meets electromagnetic compatibility standards. Verify that it does not emit excessive electromagnetic interference (EMI) and is immune to external electromagnetic disturbances.
- Crosstalk and Interference Testing: Measure crosstalk between adjacent ADC channels and ensure it meets specified isolation levels. Verify that external signals do not induce errors in the ADC outputs.

Firmware and Software Verification

- Firmware Functionality Testing: Verify the correct operation of any on-board firmware (e.g., configuration routines for ADCs and clock distribution). Ensure that firmware updates can be applied without causing malfunction.
- Driver and Software Interface Testing: Test any drivers or software libraries provided for interfacing with the ADC FMC module. Ensure they function correctly with the host system and accurately configure the module as required.

Review and Documentation

- Test Report Compilation: Document all test procedures, results, and any anomalies or failures encountered during verification.
- Failure Analysis: For any test failures, perform a root cause analysis to determine the source of the issue (e.g., hardware defect, design flaw, or software bug) and implement corrective actions.

User Acceptance Testing

- End-User Simulation: Simulate typical end-user scenarios to ensure the module performs as expected in practical, real-world applications.
- User Feedback: If possible, obtain feedback from early users or beta testers to identify any unforeseen issues or areas for improvement.

6 Review Procedures

To conduct a thorough PCB design review for the SMT-FMC116, it is essential to follow a structured plan that covers all critical aspects of the design. This review ensures that the PCB meets all functional, performance, and reliability requirements before proceeding to mass manufacturing.

1. Preparation Phase
    1.1. Gather Design Documentation
- Schematic Diagrams: Complete and up-to-date schematics of the ADC FMC module.
- PCB Layout Files: Latest version of the PCB layout (Gerber files, layout views, and design files).
- Bill of Materials (BOM): Comprehensive list of all components, including manufacturer part numbers, quantities, and component specifications.
- Datasheets: Relevant datasheets for all critical components (e.g., ADC, clock sources, connectors).
- Design Requirements and Specifications: Document outlining the design goals, electrical specifications, mechanical constraints, and standards compliance (e.g., VITA57.1, EMC).
- PCB Stack-up and Layer Information: Details of the PCB layer stack-up, including material properties, layer order, thicknesses, and impedance requirements.

    1.2. Set Review Objectives and Agenda
- Identifying design errors or omissions.
- Verifying compliance with design specifications and standards.
- Ensuring manufacturability and testability.
- Prepare a detailed agenda for the review meeting, including specific areas of focus and time allocations.

2. Review Process
    2.1. Schematic Review
    - Component Selection and Placement: Ensure all components are correctly selected according to the design requirements. Verify that critical components (e.g., ADCs, PLLs) have appropriate specifications.
    - Circuit Functionality: Check the functionality of each circuit block (e.g., ADC input stage, clock distribution, power supply circuits).
    - Signal Flow and Integrity: Verify that signal flow is logical and optimal, minimizing unnecessary routing and potential signal degradation.
    - Power Supply Design: Review power distribution network (PDN) for proper decoupling, filtering, and power integrity. Ensure correct voltage levels are provided to all components.
    - Component Interfaces and Interconnects: Confirm that all component interfaces are properly designed (e.g., differential pairs for ADC inputs, LVDS lines for data transfer).
    - Test Points and Debug Interfaces: Verify adequate test points and debug interfaces are included for key signals and power rails.
    - Design Rule Compliance: Check that the schematic complies with all design rules and constraints (e.g., voltage ratings, current capacities).

    2.2. PCB Layout Review
    - Layer Stack-Up and Impedance Control: Confirm that the PCB layer stack-up is appropriate for signal integrity and power integrity, with controlled impedance for high-speed signals.

- Component Placement: Ensure strategic placement of components to minimize signal path lengths, optimize thermal management, and facilitate easy assembly and testing.
- Signal Integrity: Review routing of high-speed signals (e.g., ADC data interface, clock signals) for controlled impedance, minimal crosstalk, and reduced EMI. Verify that differential pairs are routed with proper spacing and symmetry.
- Power Integrity: Check the power plane layout for proper distribution, minimal impedance, and effective decoupling. Ensure power and ground planes are continuous and have minimal splits.
- Thermal Management: Evaluate thermal considerations, including heat dissipation paths, placement of thermal vias, and proximity of heat-sensitive components.
- Design for Manufacturability (DFM): Review the layout for manufacturability issues, such as component spacing, via sizes, solder mask alignment, and clearance requirements.
- Mechanical Fit and Form: Verify the PCB layout matches mechanical drawings and constraints (e.g., mounting holes, edge connectors, front panel interfaces).

2.3. Compliance and Standards Check

- Electrical Standards: Ensure the design meets relevant electrical standards (e.g., VITA57.1 for FMC modules, voltage and current ratings).
- EMC Compliance: Verify that design practices for electromagnetic compatibility are followed (e.g., shielding, filtering, proper grounding).
- Safety and Reliability: Check that the design adheres to safety standards (e.g., proper clearance and creepage distances, overcurrent protection).

2.4. Signal Integrity and Power Analysis

- Signal Integrity Simulation: Use simulation tools to analyze critical high-speed signals for reflections, crosstalk, and signal degradation.
- Power Integrity Simulation: Simulate the power distribution network to ensure stable power delivery with minimal noise and voltage drops.

3. Post-Review Actions
   - Issue Log: Maintain a detailed log of all identified issues, their severity, and assigned actions.
   - Review Report: Compile a comprehensive review report summarizing findings, decisions, and next steps.
   - Implement Changes: Address all issues identified during the review by making necessary revisions to the schematic and layout.
   - Re-Verification: After revisions, perform a re-verification of the design to ensure all changes have been correctly implemented and no new issues have been introduced.

7 Validation Procedures

*A **validation procedure** is a set of processes and activities performed to ensure that a product, system, or component meets the needs and expectations of the end-users or stakeholders and performs its intended function in the real-world environment. It answers the question, "Are we building the right product?" Validation is concerned with the overall performance and usability of the system, confirming that it fulfills its intended purpose and requirements as defined by the stakeholders.*

8 Timing Diagrams

Full extracts from data sheet of ADC and PLL to show exact data protocol (ADC->FPGA), ADC's configuration interface and PLL's configuration interface to be released on request

9 Circuit Description / Diagrams

9.1 Analog input frontend

The input stage is designed around a differential amplifier, based on either the ADA4930 or ADA4940, depending on the application requirements. This stage features an optional 50-ohm termination, which can be configured during the assembly stage to match the input impedance as necessary. The default input configuration is set for a 1V peak-to-peak signal, but this can be adjusted to accommodate different signal levels. Additionally, the input stage accepts common-mode voltage on the inputs up to 1V, ensuring compatibility with various signal sources. When the ADA4930 is used, an additional passive filter is incorporated to attenuate signals down to the Nyquist frequency of the connected ADC, improving overall signal fidelity by minimizing noise and unwanted high-frequency components. This combination of flexible input configuration, termination options, and filtering ensures robust signal processing in a wide range of applications.

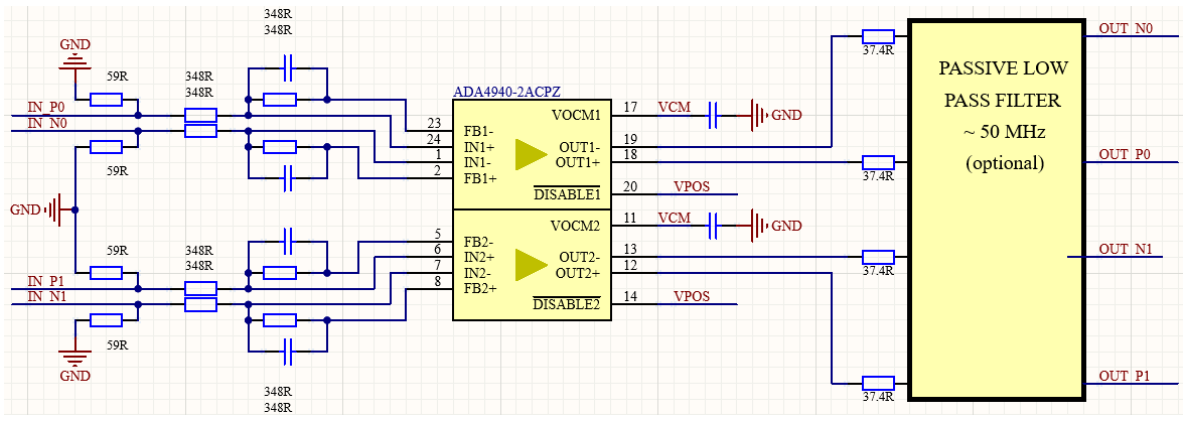

Figure: Schematic View of Analog Inputs

9.2 FMC Interface

9.2.1 Slow Control Signals

All signals listed in the table are configured as single-ended connections and reference a VADJ FMC voltage. Their primary purpose is to provide operational parameters over the Serial Peripheral Interface (SPI) to both the ADC and PLL chips.

Signal	Pin Number	Pin Name	Type
SCLK	h26	LA21_N	ADC
SDI	d23	LA23_P	ADC
SDO	g25	LA22_N	ADC
CS0	g21	LA20_P	ADC

CS1	g22	LA20_N	ADC
CS2	g24	LA22_P	ADC
CS3	h25	LA21_P	ADC
SCLK	d27	LA26_N	PLL
SDO	h31	LA28_P	PLL
SDIO	h32	LA28_N	PLL
CS	c27	LA27_N	PLL
Power Down	c26	LA27_P	PLL

9.2.2 ADC Data Interface

The ADC data interface features a high-speed serial architecture that utilizes two lanes per channel, enabling efficient data transmission. It operates at speeds of up to 1 Gbps, ensuring rapid data transfer rates to meet demanding application requirements. The interface is synchronized to the Data Clock Output (DCO), which provides a precise timing reference for the data signals. Additionally, the Frame (FR) signal plays a crucial role in detecting word boundaries within the data stream, ensuring that the received information is correctly aligned and interpreted. This combination of high-speed operation, synchronization, and boundary detection allows for robust and reliable data communication in complex systems.

The table presents mapping of the signals to FMC connector.

ADC0			
Data Lane 0	P_DATA_N0/P_DATA_P0	c22/c23	LA18_P_CC/LA18_N_CC
Data Lane 1	P_DATA_N1/P_DATA_P1	d20/d21	LA17_P_CC/LA17_N_CC
Data Lane 2	P_DATA_N2/P_DATA_P2	h22/h23	LA19_P/LA19_N
Data Lane 3	P_DATA_N3/P_DATA_P3	c18/c19	LA14_P/LA14_N
Data Lane 4	P_DATA_N4/P_DATA_P4	g18/g19	LA16_P/LA16_N
Data Lane 5	P_DATA_N5/P_DATA_P5	d17/d18	LA13_P/LA13_N
Data Lane 6	P_DATA_N6/P_DATA_P6	h16/h17	LA11_P/LA11_N
Data Lane 7	P_DATA_N7/P_DATA_P7	g15/g16	LA12_P/LA12_N
DCO Signal 0	P_DCO_N0/P_DCO_P0	d9/d8	LA01_N_CC/LA01_P_CC
FR Signal 0	P_FR_N0/P_FR_P0	h19/h20	LA15_P/LA15_N
ADC1			
Data Lane 8	P_DATA_N8/P_DATA_P8	d14/d15	LA09_P/LA09_N

Data Lane 9	P_DATA_N9/P_DATA_P9	h13/h14	LA07_P/LA07_N
Data Lane 10	P_DATA_N10/P_DATA_P10	g12/g13	LA08_P/LA08_N
Data Lane 11	P_DATA_N11/P_DATA_P11	c15/c14	LA10_N/LA10_P
Data Lane 12	P_DATA_N12/P_DATA_P12	g9/g10	LA03_P/LA03_N
Data Lane 13	P_DATA_N13/P_DATA_P13	d11/d12	LA05_P/LA05_N
Data Lane 14	P_DATA_N14/P_DATA_P14	h7/h8	LA02_P/LA02_N
Data Lane 15	P_DATA_N15/P_DATA_P15	c10/c11	LA06_P/LA06_N
DCO Signal 1	P_DCO_N1/P_DCO_P1	g7/g6	LA00_N_CC/LA00_P_CC
FR Signal 1	P_FR_N1/P_FR_P1	h10/h11	LA04_P/LA04_N
ADC2			
Data Lane 16	P_DATA_N16/P_DATA_P16	f19/f20	HA19_P/HA19_N
Data Lane 17	P_DATA_N17/P_DATA_P17	f16/f17	HA15_P/HA15_N
Data Lane 18	P_DATA_N18/P_DATA_P18	j18/j19	HA18_P/HA18_N
Data Lane 19	P_DATA_N19/P_DATA_P19	e15/e16	HA16_P/HA16_N
Data Lane 20	P_DATA_N20/P_DATA_P20	j15/j16	HA14_P/HA14_N
Data Lane 21	P_DATA_N21/P_DATA_P21	f13/f14	HA12_P/HA12_N
Data Lane 22	P_DATA_N22/P_DATA_P22	k13/k14	HA10_P/HA10_N
Data Lane 23	P_DATA_N23/P_DATA_P23	j12/j13	HA11_P/HA11_N
DCO Signal 2	P_DCO_N2/P_DCO_P2	f5/f4	HA00_N_CC/HA00_P_CC
FR Signal 2	P_FR_N2/P_FR_P2	k16/k17	HA17_P_CC/HA17_N_CC
ADC3			

Data Lane 24	P_DATA_N24/P_DATA_P24	e12/e13	HA13_P/HA13_N
Data Lane 25	P_DATA_N25/P_DATA_P25	k10/k11	HA06_P/HA06_N
Data Lane 26	P_DATA_N26/P_DATA_P26	f10/f11	HA08_P/HA08_N
Data Lane 27	P_DATA_N27/P_DATA_P27	j9/j10	HA07_P/HA07_N
Data Lane 28	P_DATA_N28/P_DATA_P28	e9/e10	HA09_P/HA09_N
Data Lane 29	P_DATA_N29/P_DATA_P29	j6/j7	HA03_P/HA03_N
Data Lane 30	P_DATA_N30/P_DATA_P30	f7/f8	HA04_P/HA04_N
Data Lane 31	P_DATA_N31/P_DATA_P31	e6/e7	HA05_P/HA05_N
DCO Signal 3	P_DCO_N3/P_DCO_P3	e3/e2	HA01_N_CC/HA01_P_CC
FR Signal 3	P_FR_N3/P_FR_P3	k7/k8	HA02_P/HA02_N

10 Footprint

10.1 Top View

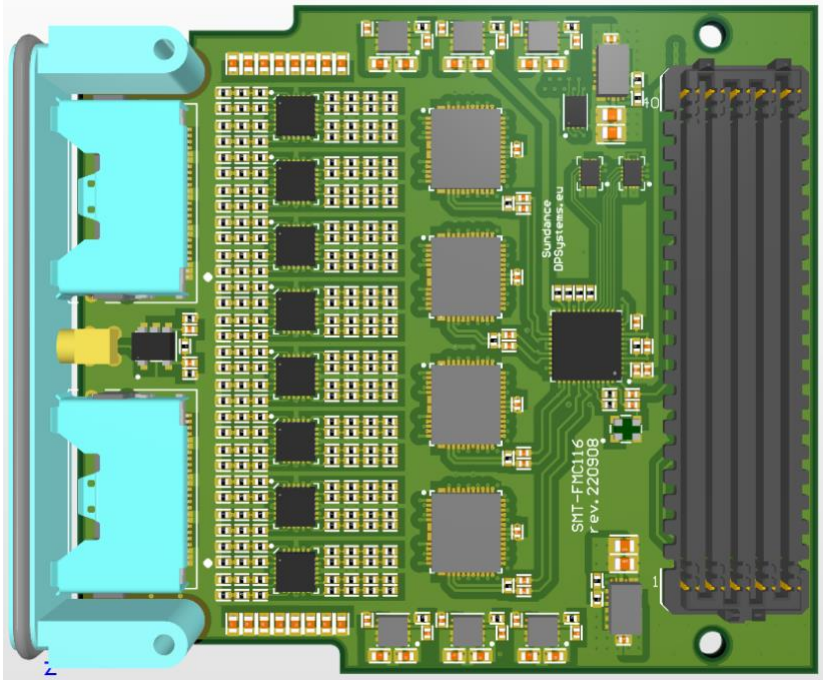

Figure Top View of the Module

10.2 Bottom View

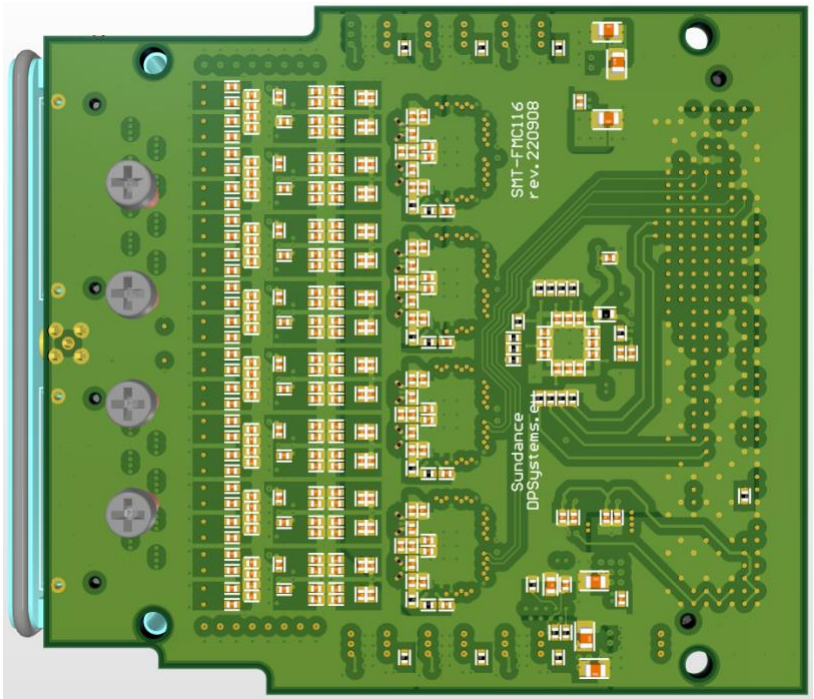

Figure: Bottom View of the Module

11 Pinout

The chapter presents a complete pin-out of the FMC HPC connector with additional remarks with LPC compatibility (4 and 8 channels versions only)

FMC Pin Number	SMT-FMC116 Function	Compatibility Info

The following table describes exact pinout of front-panel analog connector with additional info of limitations of 4 and 8 channel versions.

ARF6 Pin Number	SMT-FMC116 Function	Compatibility Info

12 Support Packages

The board is delivered with VHDL-implemented board support packages, which are used for example on selected Xilinx Evaluation Boards (7-series and Ultrascale Family). The support package contains elements to configure an interface to a fast data stream of ADCs, control on-board clock distribution, and interface with trigger inputs.

13 Physical Properties

Dimensions		Typical	Max
Weight			
Supply Voltages			
Supply Current	+12V		
	+3.3V		
	VADJ		
MTBF			

14 Safety

This module presents no hazard to the user when used normally.

15 EMC

This module is designed to operate from within an enclosed host system built to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless installed within an adequate host system.

This module is protected from damage by fast voltage transients from outside the host system, which may be introduced through the output cables.

Short-circuiting any output to the ground does not cause the host PC system to lock up or reboot.