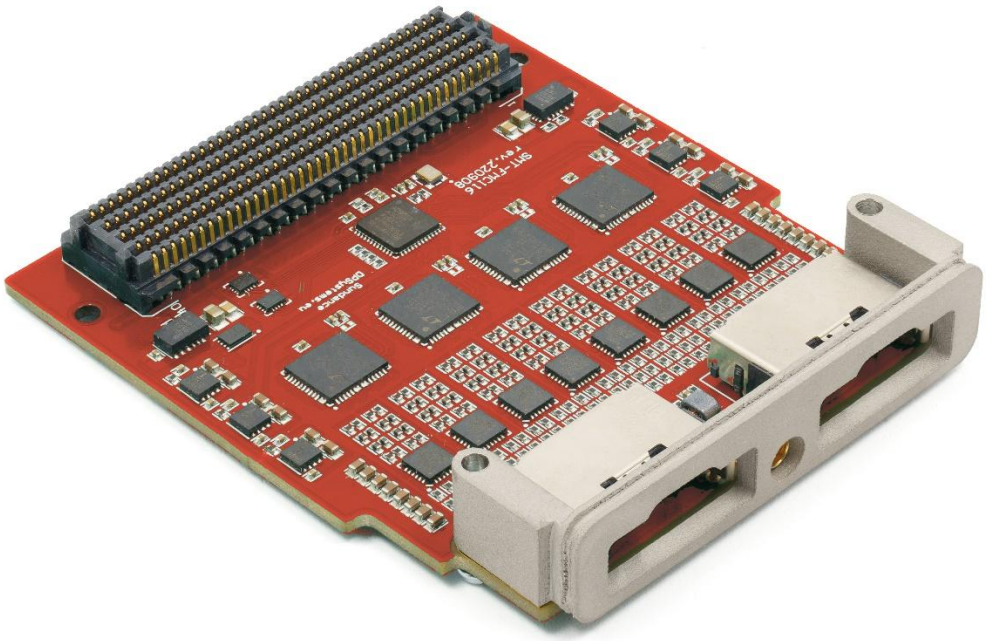
Unit / Module Description:	4, 8 or 16 Channels ADC @ 125MHz on an FMC Module – 12/14-bits – LPC or HPC
Unit / Module Number:	SMT-FMC116-xxx
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Product Specification for *SMT-FMC116*



LPC/HPC FMC Module
4, 8 & 16 ADC channels

Revision History

Issue	Changes Made	Date	Initials
1	Initial Version	9.12.2021	WJ
1.1	Added comments	14.12.2021	FC
1.2	Added photos and updated diagrams	26.09.2024	FC
1.3	Updated diagrams, pictures and technical details after rework of the board	26.06.2025	WJ
1.4	Updates around clock sections	1.11.2026	WJ

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Table of Contents

1 Introduction 4
2 Related Documents 5
2.1 Referenced Documents 5
2.2 Applicable Documents 5
3 Acronyms, Abbreviations and Definitions 5
3.1 Acronyms and Abbreviations 5
3.2 Definitions 5
4 Functional Description 5
4.1 Block Diagram 6
4.2 Module Description 6
4.2.1 ARF6-RA AcceleRate® Right-Angle 6
4.2.2 Clock and Trigger Inputs 7
4.2.3 Clock Distribution 7
4.2.4 ADC 7
4.2.5 On-Board LEDs 7
4.3 Interface Description 7
4.3.1 Mechanical Interface 9
5 Verification Procedures 9
6 Review Procedures 11
7 Validation Procedures 13
8 Timing Diagrams 13
9 Circuit Description / Diagrams 14
9.1 Analog input frontend 14
9.2 FMC Interface 15
9.2.1 Slow Control Signals 15
9.2.2 ADC Data Interface 16
10 Footprint 19
10.1 Top View 19
10.2 Bottom View 19
11 Pinout 20
12 Support Packages 24
13 Physical Properties 24
14 Safety 24

15 EMC.....25

Table of Figures

Not Defined

1 Introduction

The document outlines the specifications of the SMT-FMC116 module, a general-purpose digitizer card available in configurations with 4, 8, or 16 fully differential input channels. Each channel utilizes a 14-bit, 125 MSPS ADC. The module features dedicated clock distribution circuitry and adheres to the VITA 57.1 FMC standard: it uses the FMC-HPC interface for the 16-channel version and the FMC-LPC interface for the 4- and 8-channel versions, enabling compatibility with a range of carrier boards.

2 Related Documents

2.1 Referenced Documents

Full details of circuits and datasheet of individual components on request

2.2 Applicable Documents

3 Acronyms, Abbreviations and Definitions

3.1 Acronyms and Abbreviations

ADC - Analog-to-Digital Converter

FMC - FPGA Mezzanine Card

LPC - Low Pin Count

HPC - High Pin Count

SMT - Surface-Mount Technology

MSPS - Mega Samples Per Second

VITA - VMEbus International Trade Association

FPGA - Field-Programmable Gate Array

LVDS - Low Voltage Differential Signaling

PLL - Phase-Locked Loop

Gbps - Gigabits per Second

LED - Light Emitting Diode

ANSI - American National Standards Institute

VHDL - VHSIC (Very High-Speed Integrated Circuit) Hardware Description Language

MTBF - Mean Time Between Failures

EMC - Electromagnetic Compatibility

MHz - Megahertz

SMA - SubMiniature version A (connector type)

3.2 Definitions

To Be Defined Later

4 Functional Description

4.1 Block Diagram

The figure presents a general block diagram of all the elements on the board. Individual submodules are described in greater detail in the following chapters.

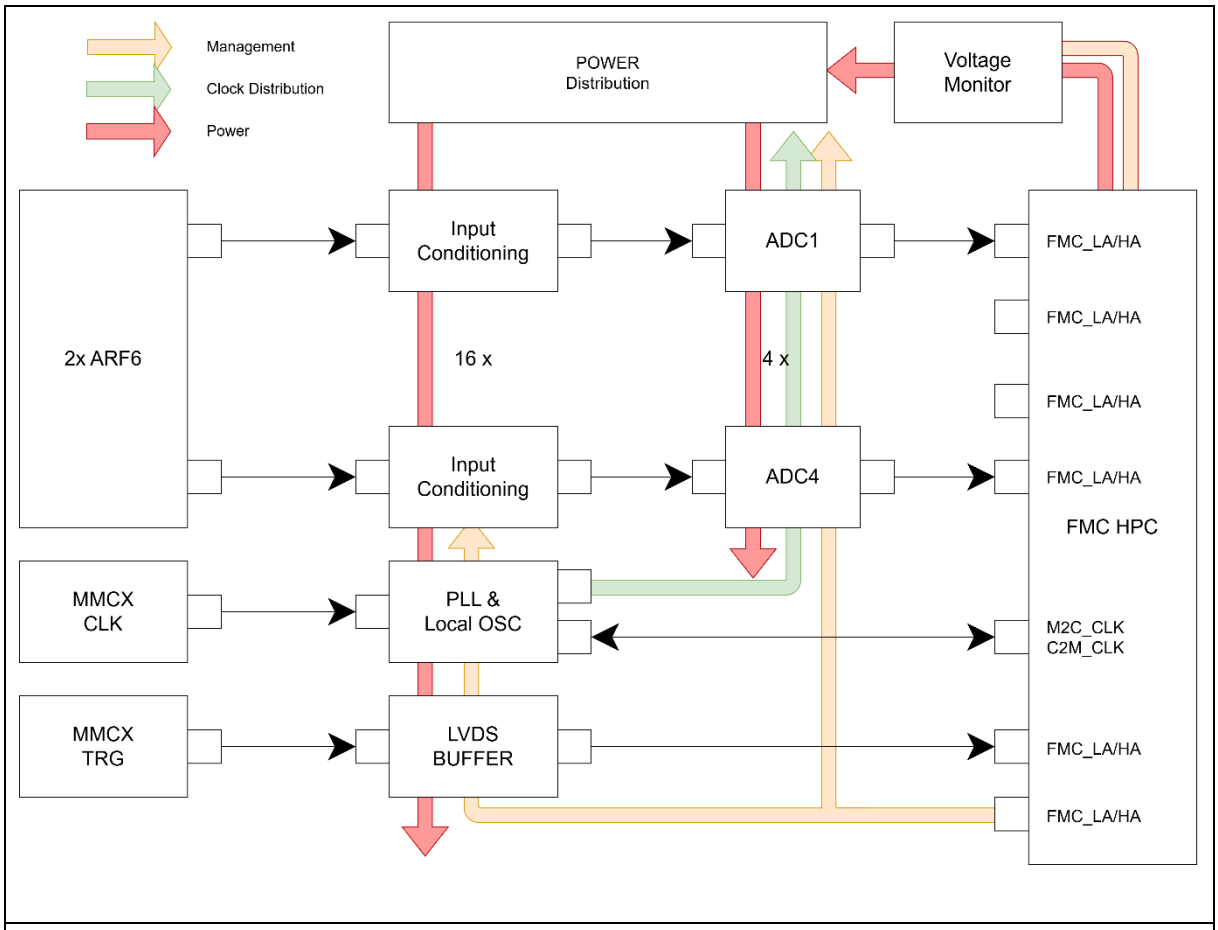


Figure: General block diagram of the board

4.2 Module Description

4.2.1 ARF6-RA AcceleRate® Right-Angle

The ARF6-RA is a high-density Samtec connector originally designed to meet digital performance requirements. However, under certain conditions—such as proper channel separation—it also satisfies the demands of analog applications. This connector enables the integration of 16 differential channels on a single FMC module. To simplify system integration and operation, dedicated signal adapters are available as separate products: single-ended SMA to ARF6, and differential SMA to ARF6.



Picture 1 - Samtec ARF6-RA Connector

Full measurement results for attenuation and crosstalk between adjacent channels on request

4.2.2 Clock and Trigger Inputs

The board provides a **front-panel MMCX clock input** and a **U.FL trigger input located near the FMC connector**. The 50 Ω clock input connects through a transformer to the differential input of the clock distribution circuitry.

The trigger input supports high-impedance or 50 Ω termination and feeds an LVDS driver, which routes the differential trigger signal to the carrier FPGA through the FMC connector. For front-panel access, the U.FL input can be connected to a **panel-mounted MMCX bulkhead connector using a U.FL-to-MMCX patch cable**.

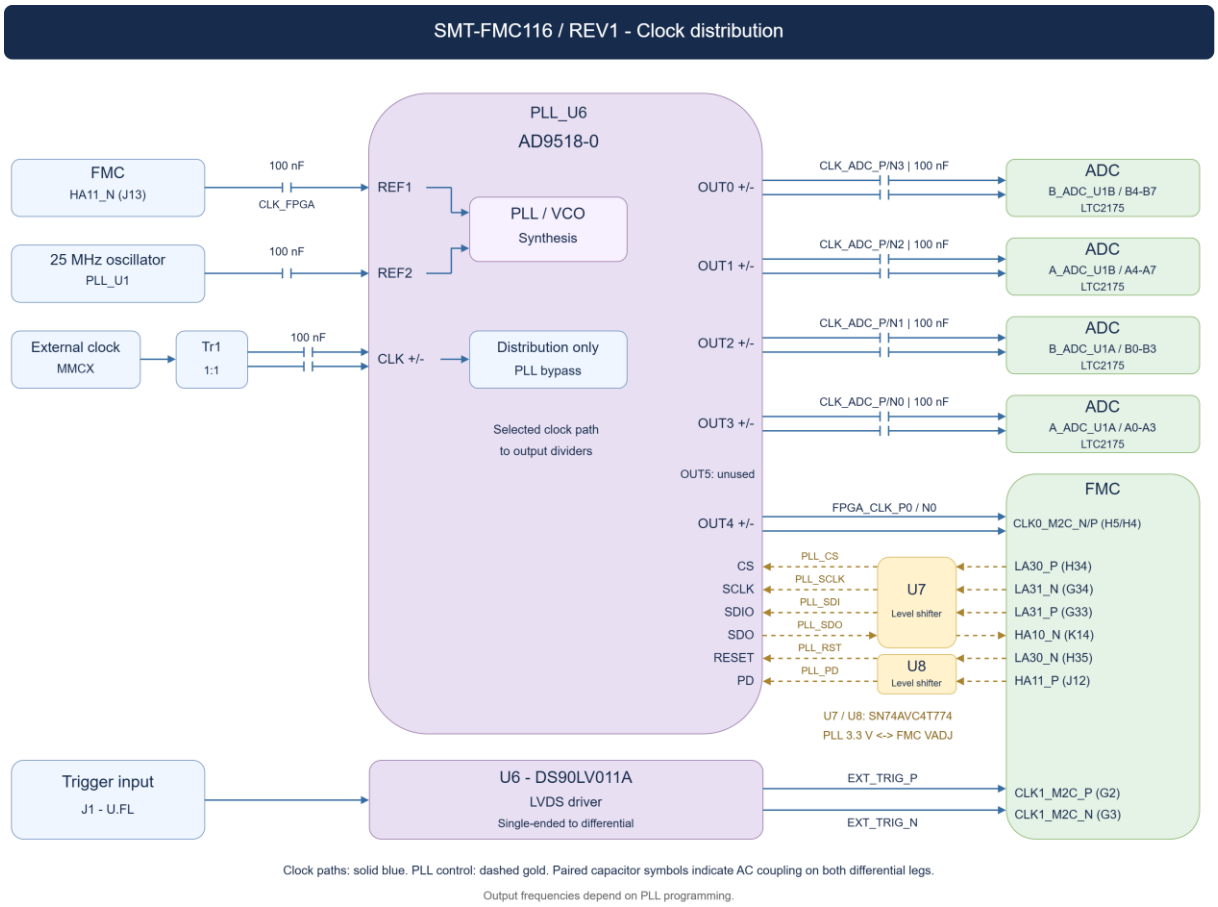
4.2.3 Clock Distribution

The block diagram below shows the board's clock distribution, PLL control, and trigger input paths. The **Analog Devices AD9518-0ABCPZ** supports three clock sources:

1. **On-board 25 MHz oscillator** — Connected to REF2 and used as the default reference for PLL clock synthesis.
2. **Front-panel MMCX clock input** — Connected through a transformer to the differential CLK input for clock distribution with the PLL bypassed.
3. **FPGA-generated clock on HA11_N** — Connected to REF1 for PLL clock synthesis, primarily for debugging and internal testing. **This clock source is available only when VADJ = 2.5 V.**

The AD9518 provides four differential clock pairs to the ADCs and one differential clock pair to the FPGA through **CLK0_M2C**. Output frequencies, phases, and delays depend on the device's programmable settings. PLL control signals connect to the FMC interface through the **U7 and U8 level shifters**.

The diagram also shows the separate trigger path: the **J1 U.FL input** feeds the **U6 LVDS driver**, which sends a differential trigger signal to the FPGA through **CLK1_M2C_P/N**.



The PLL configuration can be defined using the **Analog Devices** [AD9516/AD9517/AD9518 Evaluation Software](). Select the **AD9518-0** device to configure the reference input, PLL parameters, output dividers, and clock outputs. The resulting register settings can then be applied by the carrier FPGA through the board's PLL control interface.

4.2.4 ADC

The board uses the **LTC2175-14** ADC, which offers an efficient high-speed serial data interface operating at 1 Gbps, minimizing the number of required data lines. It also supports dynamic reconfiguration of data output properties, allowing for flexible system integration. The LTC2175 belongs to a scalable ADC family, available in both 12-bit and 14-bit resolution options, with selectable sampling frequencies of 80, 105, or 125 MSPS.

4.2.5 On-Board LEDs

The board is equipped with **2 diagnostic LEDs** and **4 general-purpose LEDs**. The diagnostic LEDs indicate the status of the board power supplies: one LED signals that the intermediate power supplies are within specification, while the other indicates that all required power supplies are operating correctly. The four general-purpose LEDs are connected to the FMC connector and can be controlled by the FMC carrier for user-defined status indication or debugging.

4.3 Interface Description

The module is implemented as an **HPC FMC-compatible mezzanine card**. The 4- and 8-channel and 12-channel versions are also **LPC-compatible**, with no loss of functionality. The pinout of the FMC interface is detailed in **Chapter 11**.

4.3.1 Mechanical Interface

The mechanical interface complies with the **ANSI/VITA 57.1** standard. The module is implemented as a **single-width FMC** mezzanine card and includes a **standard FMC front panel bezel**. A general mechanical overview of the module is presented below.

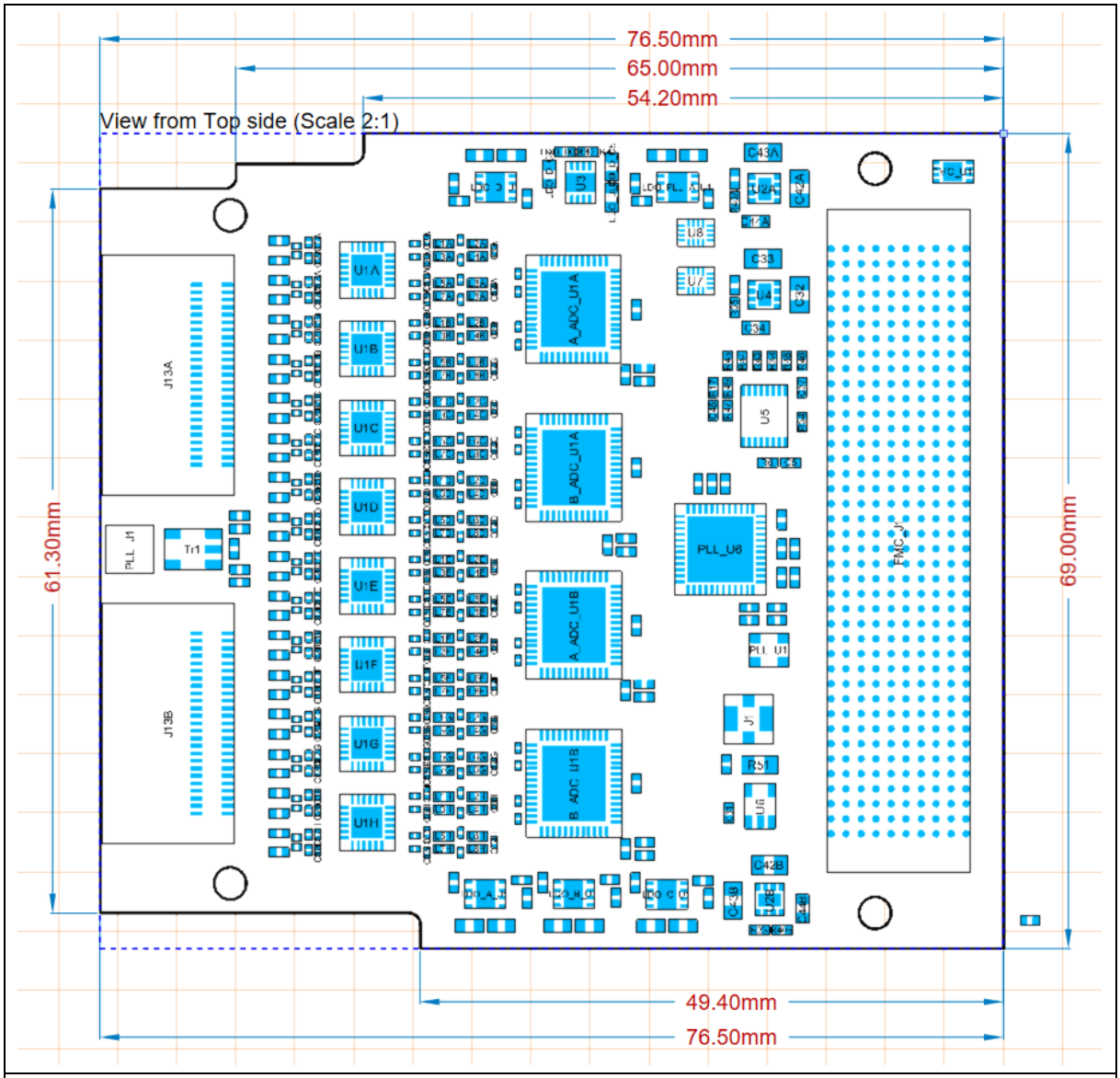


Figure: Mechanical interface

5 Verification Procedures

A comprehensive verification procedure is necessary to ensure that the SMT-FMC116 performs as promised. This process will help confirm that the module meets its design specifications, functions correctly under all intended operating conditions, and reliably interfaces with other components and systems. The suggested verification procedure for the ADC FMC module should include:

1. Preliminary Checks

- Visual Inspection: Conduct a thorough visual inspection of the ADC FMC module for any physical damage, incorrect component placements, solder joint issues, or other manufacturing defects.
- Documentation Review: Verify that the module's documentation (datasheets, user manuals, etc.) is up-to-date and matches the module's hardware and firmware versions.

2. Power-Up and Initialization Testing

- Power Supply Verification: Check that the power supply voltages (e.g., +12V, +3.3V, VADJ) are within the specified range and remain stable during operation.
- Power-On Self-Test (POST): Ensure that the module successfully completes a power-on self-test (if applicable), with all diagnostic LEDs functioning as expected (e.g., power status and PLL lock indicators).
- Current Consumption Check: Measure the power consumption of the module at different stages of operation to ensure it is within specified limits. Check for unexpected current draws that might indicate a short or faulty component.

3. Functional Testing

ADC Performance Validation:

- Input Signal Testing: Apply known analog signals (e.g., sine wave, square wave, and white noise) of varying frequencies and amplitudes to the ADC inputs through the SMA connectors.
- Sampling Rate Verification: Verify the ADC operates at the specified sampling rates (e.g., 125 MSPS, and any lower frequencies if supported) and that the sampling rate can be dynamically adjusted if applicable.
- Resolution Verification: Ensure the ADC outputs digital data at the specified resolution (e.g., 12-bit or 14-bit), and validate that the resolution can be changed if the module supports different configurations.
- Dynamic Range and SNR Testing: Measure the dynamic range and signal-to-noise ratio (SNR) of the ADC using a standard test signal (such as a full-scale sine wave) and verify that these parameters meet or exceed the specifications.

Clock and Synchronization Testing

- Clock Source Selection: Verify the module can select and switch between different clock sources (on-board oscillator, external clock via front panel, FMC_CLK2_C2M, etc.) as described in the specifications.
- PLL Functionality: Test the PLL's ability to synthesize various output frequencies, phases, and delays based on different input clocks. Ensure the PLL locks correctly and that any phase noise or jitter is within acceptable limits.
- Clock Distribution Network: Verify that the internal clock distribution network delivers the correct clock signals to all ADCs and the FPGA interface.

Data Interface Testing

- Data Integrity Check: Use a known test pattern or ramp signal to verify that data captured from the ADC is transmitted accurately to the FPGA or host system without errors or data corruption.
- Interface Compatibility: Confirm that the module's FMC interface (HPC or LPC) functions correctly and is compatible with various carrier boards (e.g., Xilinx Evaluation Boards).
- Signal Quality Assessment: Use an oscilloscope or logic analyzer to inspect the quality of the digital data signals (e.g., LVDS lines) at the FMC interface. Check for proper voltage levels, signal integrity, and timing.

Environmental and Stress Testing

- Thermal Testing: Perform tests at various operating temperatures to ensure the module functions correctly across its specified temperature range. Monitor ADC performance for any degradation (e.g., increased noise or reduced accuracy) at temperature extremes.
- Power Cycling: Repeatedly power-cycle the module to ensure reliable startup and operation without faults or errors.
- Long-Term Stability Testing: Run the module continuously under normal and extreme conditions to test for long-term stability and reliability, looking for signs of drift or failure.

Interference and EMC Testing

- EMC Compliance: Test the module in a shielded environment to ensure it meets electromagnetic compatibility standards. Verify that it does not emit excessive electromagnetic interference (EMI) and is immune to external electromagnetic disturbances.
- Crosstalk and Interference Testing: Measure crosstalk between adjacent ADC channels and ensure it meets specified isolation levels. Verify that external signals do not induce errors in the ADC outputs.

Firmware and Software Verification

- Firmware Functionality Testing: Verify the correct operation of any on-board firmware (e.g., configuration routines for ADCs and clock distribution). Ensure that firmware updates can be applied without causing malfunction.
- Driver and Software Interface Testing: Test any drivers or software libraries provided for interfacing with the ADC FMC module. Ensure they function correctly with the host system and accurately configure the module as required.

Review and Documentation

- Test Report Compilation: Document all test procedures, results, and any anomalies or failures encountered during verification.
- Failure Analysis: For any test failures, perform a root cause analysis to determine the source of the issue (e.g., hardware defect, design flaw, or software bug) and implement corrective actions.

User Acceptance Testing

- End-User Simulation: Simulate typical end-user scenarios to ensure the module performs as expected in practical, real-world applications.
- User Feedback: If possible, obtain feedback from early users or beta testers to identify any unforeseen issues or areas for improvement.

6 Review Procedures

To conduct a thorough PCB design review for the SMT-FMC116, it is essential to follow a structured plan that covers all critical aspects of the design. This review ensures that the PCB meets all functional, performance, and reliability requirements before proceeding to mass manufacturing.

1. Preparation Phase
    1.1. Gather Design Documentation
- Schematic Diagrams: Complete and up-to-date schematics of the ADC FMC module.
- PCB Layout Files: Latest version of the PCB layout (Gerber files, layout views, and design files).
- Bill of Materials (BOM): Comprehensive list of all components, including manufacturer part numbers, quantities, and component specifications.
- Datasheets: Relevant datasheets for all critical components (e.g., ADC, clock sources, connectors).
- Design Requirements and Specifications: Document outlining the design goals, electrical specifications, mechanical constraints, and standards compliance (e.g., VITA57.1, EMC).
- PCB Stack-up and Layer Information: Details of the PCB layer stack-up, including material properties, layer order, thicknesses, and impedance requirements.

    1.2. Set Review Objectives and Agenda
- Identifying design errors or omissions.
- Verifying compliance with design specifications and standards.
- Ensuring manufacturability and testability.
- Prepare a detailed agenda for the review meeting, including specific areas of focus and time allocations.

2. Review Process
    2.1. Schematic Review
    - Component Selection and Placement: Ensure all components are correctly selected according to the design requirements. Verify that critical components (e.g., ADCs, PLLs) have appropriate specifications.
    - Circuit Functionality: Check the functionality of each circuit block (e.g., ADC input stage, clock distribution, power supply circuits).
    - Signal Flow and Integrity: Verify that signal flow is logical and optimal, minimizing unnecessary routing and potential signal degradation.
    - Power Supply Design: Review power distribution network (PDN) for proper decoupling, filtering, and power integrity. Ensure correct voltage levels are provided to all components.
    - Component Interfaces and Interconnects: Confirm that all component interfaces are properly designed (e.g., differential pairs for ADC inputs, LVDS lines for data transfer).
    - Test Points and Debug Interfaces: Verify adequate test points and debug interfaces are included for key signals and power rails.
    - Design Rule Compliance: Check that the schematic complies with all design rules and constraints (e.g., voltage ratings, current capacities).

    2.2. PCB Layout Review

- Layer Stack-Up and Impedance Control: Confirm that the PCB layer stack-up is appropriate for signal integrity and power integrity, with controlled impedance for high-speed signals.
- Component Placement: Ensure strategic placement of components to minimize signal path lengths, optimize thermal management, and facilitate easy assembly and testing.
- Signal Integrity: Review routing of high-speed signals (e.g., ADC data interface, clock signals) for controlled impedance, minimal crosstalk, and reduced EMI. Verify that differential pairs are routed with proper spacing and symmetry.
- Power Integrity: Check the power plane layout for proper distribution, minimal impedance, and effective decoupling. Ensure power and ground planes are continuous and have minimal splits.
- Thermal Management: Evaluate thermal considerations, including heat dissipation paths, placement of thermal vias, and proximity of heat-sensitive components.
- Design for Manufacturability (DFM): Review the layout for manufacturability issues, such as component spacing, via sizes, solder mask alignment, and clearance requirements.
- Mechanical Fit and Form: Verify the PCB layout matches mechanical drawings and constraints (e.g., mounting holes, edge connectors, front panel interfaces).

2.3. Compliance and Standards Check

- Electrical Standards: Ensure the design meets relevant electrical standards (e.g., VITA57.1 for FMC modules, voltage and current ratings).
- EMC Compliance: Verify that design practices for electromagnetic compatibility are followed (e.g., shielding, filtering, proper grounding).
- Safety and Reliability: Check that the design adheres to safety standards (e.g., proper clearance and creepage distances, overcurrent protection).

2.4. Signal Integrity and Power Analysis

- Signal Integrity Simulation: Use simulation tools to analyze critical high-speed signals for reflections, crosstalk, and signal degradation.
- Power Integrity Simulation: Simulate the power distribution network to ensure stable power delivery with minimal noise and voltage drops.

3. Post-Review Actions
   - Issue Log: Maintain a detailed log of all identified issues, their severity, and assigned actions.
   - Review Report: Compile a comprehensive review report summarizing findings, decisions, and next steps.
   - Implement Changes: Address all issues identified during the review by making necessary revisions to the schematic and layout.
   - Re-Verification: After revisions, perform a re-verification of the design to ensure all changes have been correctly implemented and no new issues have been introduced.

7 Validation Procedures

*A **validation procedure** is a set of processes and activities performed to ensure that a product, system, or component meets the needs and expectations of the end-users or stakeholders and performs its intended function in the real-world environment. It answers the question, "Are we building the right product?" Validation is concerned with the overall performance and usability of the system, confirming that it fulfills its intended purpose and requirements as defined by the stakeholders.*

8 Timing Diagrams

Full extracts from the ADC and PLL datasheets—detailing the ADC-to-FPGA data protocol, the ADC configuration interface, and the PLL configuration interface—are available upon request.

The documents are avialable online on the vendor's webpages:

Analog Devices: LTC217x-XX datasheet

Analog Devices: AD9518-0 datasheet

9 Circuit Description / Diagrams

9.1 Analog input frontend

The input stage is based on the **ADA4938-2ACPZ**, a dual, fully differential amplifier optimized for driving high-speed ADCs. Each channel is DC-coupled and features a passive resistive network for signal scaling and impedance matching. The input stage is designed to operate from a symmetric power supply. The supply voltage can be adjusted to meet application-specific requirements, allowing the trade-off between input signal range, dynamic performance, and power dissipation to be optimized.

The design supports both differential and single-ended input configurations:

- In differential mode, both input lines (positive and negative) are actively driven and processed symmetrically.
- For single-ended operation, one input (e.g., IN_Px) is driven with the signal, while the complementary input (IN_Nx) is terminated to ground. The amplifier internally converts the single-ended signal into a differential output suitable for the ADC.

After amplification, signals are passed to a PI-type LC low-pass filter, which attenuates high-frequency noise and harmonics above the Nyquist frequency, improving signal fidelity.

Each channel includes a common-mode voltage reference (VCM) to ensure compatibility with ADC input levels, and the power supply is locally decoupled to maintain analog integrity.

This flexible input architecture—supporting both signal types—makes the design suitable for a wide range of data acquisition and RF front-end applications.

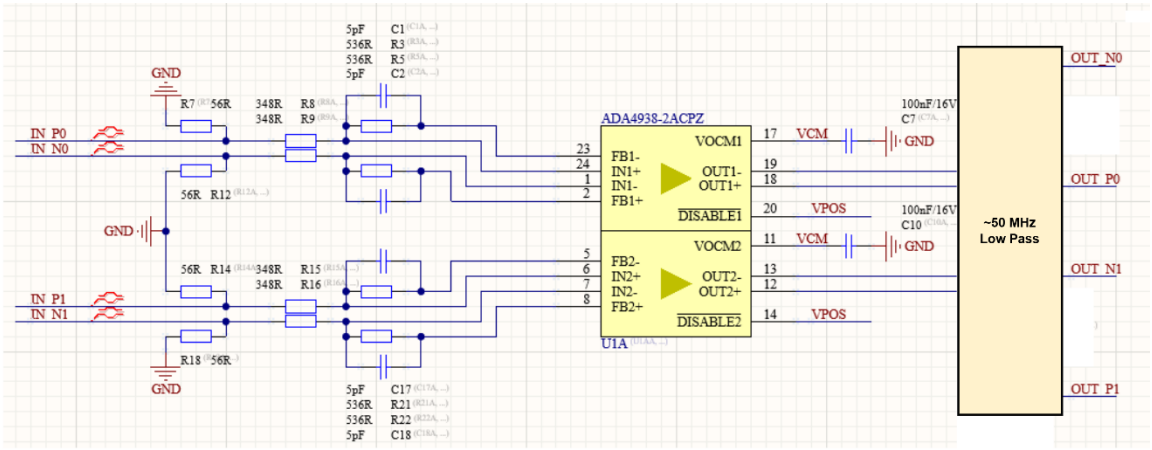


Figure: Schematic View of Analog Inputs

9.2 FMC Interface

9.2.1 Slow Control Signals

All signals listed in the table are configured as single-ended connections and reference a VADJ FMC voltage. Their primary purpose is to provide operational parameters over the Serial Peripheral Interface (SPI) to both the ADC and PLL chips.

Signal	Pin Number	Pin Name
EXT_TRIG_P	G2	CLK1_M2C_P
EXT_TRIG_N	G3	CLK1_M2C_N
FPGA_CLK_N0	H4	CLK0_M2C_P
FPGA_CLK_P0	H5	CLK0_M2C_N
CLK_FPGA	J13	HA11_N
P_SCLK	G34	LA31_N
P_SDI	G33	LA31_P
P_SDO	K13	HA10_P
P_CS0	H38	LA32_N
P_CS1	G37	LA33_N
P_CS2	H37	LA32_P
P_CS3	G36	LA33_P

FMC_CS_N	H34	LA30_P
FMC_SDO	K14	HA10_N
FMC_RESET_N	H35	LA30_N
FMC_PD_N	J12	HA11_P

9.2.2 ADC Data Interface

The ADC data interface features a high-speed serial architecture that utilizes two lanes per channel, enabling efficient data transmission. It operates at speeds of up to 1 Gbps, ensuring rapid data transfer rates to meet demanding application requirements. The interface is synchronized to the Data Clock Output (DCO), which provides a precise timing reference for the data signals. Additionally, the Frame (FR) signal plays a crucial role in detecting word boundaries within the data stream, ensuring that the received information is correctly aligned and interpreted. This combination of high-speed operation, synchronization, and boundary detection allows for robust and reliable data communication in complex systems.

The table presents mapping of the signals to FMC connector.

Interface	Signal Names	Pin names
Data Lane 0	P_DATA_P0/P_DATA_N0	LA29_N/LA29_P
Data Lane 0	P_DATA_P1/P_DATA_N1	LA28_N/LA28_P
Data Lane 0	P_DATA_P2/P_DATA_N2	LA24_N/LA24_P
Data Lane 0	P_DATA_P3/P_DATA_N3	LA27_N/LA27_P
Data Lane 0	P_DATA_P4/P_DATA_N4	LA26_N/LA26_P
Data Lane 0	P_DATA_P5/P_DATA_N5	LA22_N/LA22_P
Data Lane 0	P_DATA_P6/P_DATA_N6	LA21_N/LA21_P
Data Lane 0	P_DATA_P7/P_DATA_N7	LA23_N/LA23_P
DCO 0	P_DCO_P0/P_DCO_N0	LA17_P_CC/LA17_N_CC
FR 0	P_FR_P0/P_FR_N0	LA25_N/LA25_P
Data Lane 1	P_DATA_P8/P_DATA_N8	LA19_N/LA19_P
Data Lane 1	P_DATA_P9/P_DATA_N9	LA20_N/LA20_P

Data Lane 1	P_DATA_P10/P_DATA_N10	LA15_N/LA15_P
Data Lane 1	P_DATA_P11/P_DATA_N11	LA18_N_CC/LA18_P_CC
Data Lane 1	P_DATA_P12/P_DATA_N12	LA14_N/LA14_P
Data Lane 1	P_DATA_P13/P_DATA_N13	LA11_N/LA11_P
Data Lane 1	P_DATA_P14/P_DATA_N14	LA13_P/LA13_N
Data Lane 1	P_DATA_P15/P_DATA_N15	LA12_N/LA12_P
DCO 1	P_DCO_P1/P_DCO_N1	LA01_P_CC/LA01_N_CC
FR 1	P_FR_P1/P_FR_N1	LA16_N/LA16_P
Data Lane 2	P_DATA_P16/P_DATA_N16	LA08_N/LA08_P
Data Lane 2	P_DATA_P17/P_DATA_N17	LA03_N/LA03_P
Data Lane 2	P_DATA_P18/P_DATA_N18	LA09_N/LA09_P
Data Lane 2	P_DATA_P19/P_DATA_N19	LA07_N/LA07_P
Data Lane 2	P_DATA_P20/P_DATA_N20	LA05_N/LA05_P
Data Lane 2	P_DATA_P21/P_DATA_N21	LA04_N/LA04_P
Data Lane 2	P_DATA_P22/P_DATA_N22	LA06_N/LA06_P
Data Lane 2	P_DATA_P23/P_DATA_N23	LA02_N/LA02_P
DCO 2	P_DCO_P2/P_DCO_N2	LA00_P_CC/LA00_N_CC
FR 2	P_FR_P2/P_FR_N2	LA10_N/LA10_P
Data Lane 3	P_DATA_P24/P_DATA_N24	HA06_N/HA06_P
Data Lane 3	P_DATA_P25/P_DATA_N25	HA05_N/HA05_P
Data Lane 3	P_DATA_P26/P_DATA_N26	HA07_N/HA07_P
Data Lane 3	P_DATA_P27/P_DATA_N27	HA08_N/HA08_P
Data Lane 3	P_DATA_P28/P_DATA_N28	HA02_N/HA02_P
Data Lane 3	P_DATA_P29/P_DATA_N29	HA03_N/HA03_P
Data Lane 3	P_DATA_P30/P_DATA_N30	HA09_N/HA09_P

Data Lane 3	P_DATA_P31/P_DATA_N31	HA04_N/HA04_P
DCO 3	P_DCO_P3/P_DCO_N3	HA00_P_CC/HA00_N_CC
FR 3	P_FR_P3/P_FR_N3	HA01_N_CC/HA01_P_CC

10 Footprint

10.1 Top View

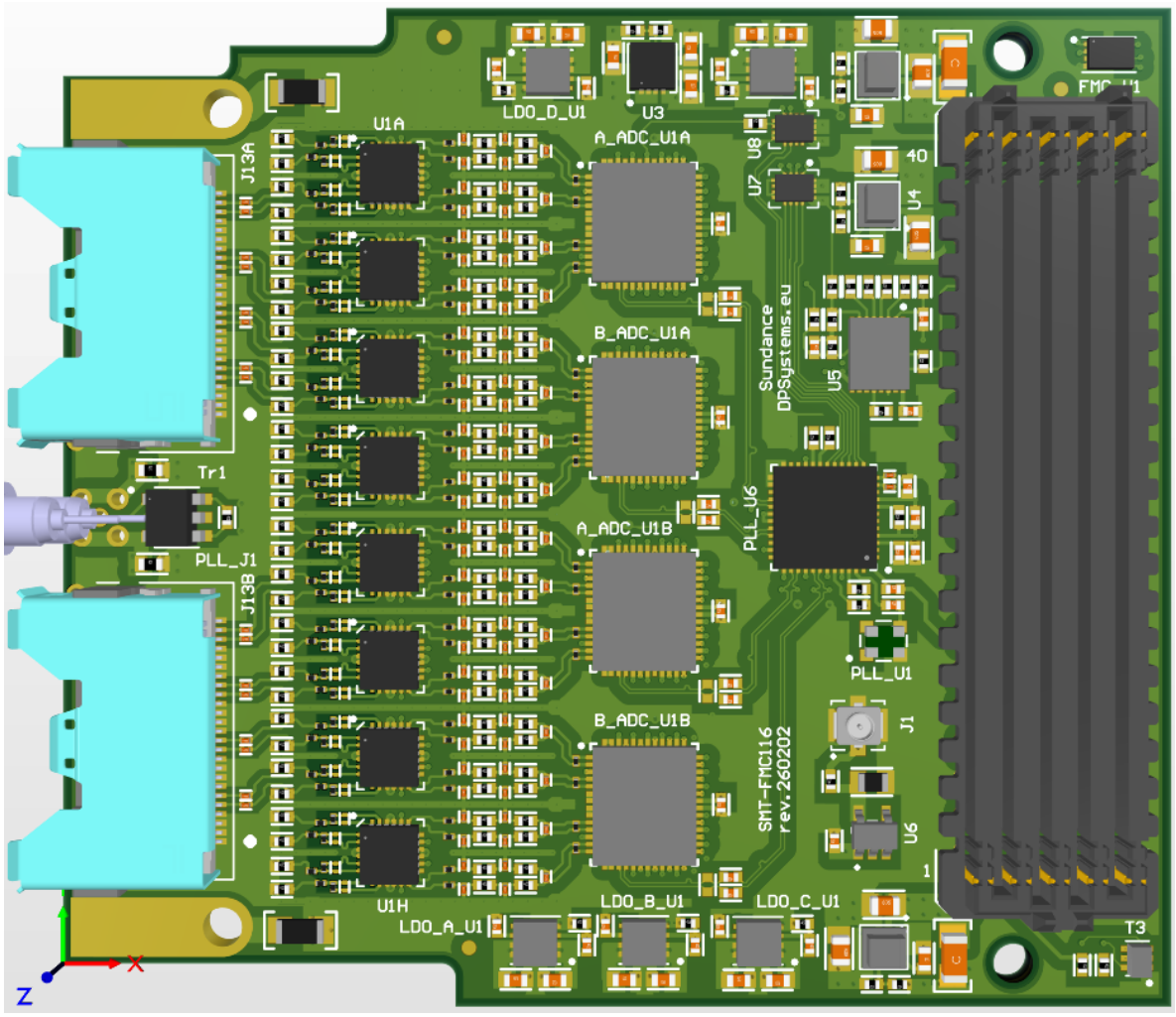


Figure Top View of the Module

10.2 Bottom View

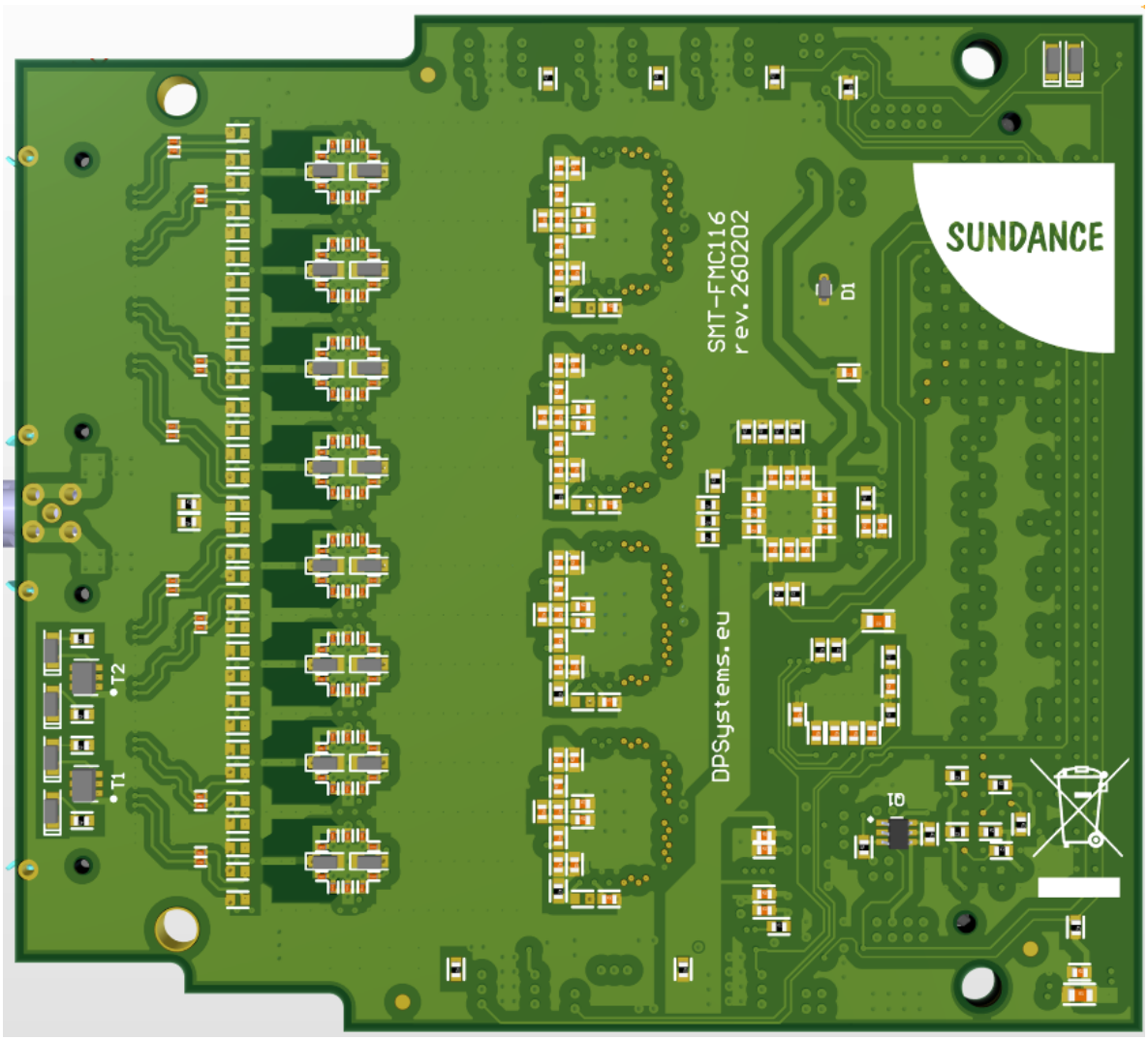


Figure: Bottom View of the Module

11 Pinout

The chapter presents a complete pin-out of the FMC HPC connector with additional remarks with LPC compatibility (4, 8 and 12 channels versions only)

Pin	FMC Pin Name	SMT-FMC116 Function	Compatibility Info
C34	GA0	GA0	Managment signal
D35	GA1	GA1	Managment signal
D1	PG_C2M	P_PG_C2M	Managment signal
F1	PG_M2C	P_PG_M2C	Managment signal
C30	SCL	SCL	Managment signal
C31	SDA	SDA	Managment signal

D30	TDI	TDI-TDO pass through	Managment signal
J13	HA11_N	CLK_FPGA	HPC only
G2	CLK1_M2C_P	EXT_TRIG_P	CLK
G3	CLK1_M2C_N	EXT_TRIG_N	CLK
H5	CLK0_M2C_N	FPGA_CLK_P0	CLK
H4	CLK0_M2C_P	FPGA_CLK_N0	CLK
H34	LA30_P	FMC_CS_N	PLL Slow Controls
J12	HA11_P	FMC_PD_N	PLL Slow Controls
H35	LA30_N	FMC_RESET_N	PLL Slow Controls
K14	HA10_N	FMC_SDO	PLL Slow Controls
H38	LA32_N	P_CS0	ADC Slow Controls
G37	LA33_N	P_CS1	ADC Slow Controls
H37	LA32_P	P_CS2	ADC Slow Controls
G36	LA33_P	P_CS3	ADC Slow Controls
G34	LA31_N	P_SCLK	PLL/ADC Slow Controls
G33	LA31_P	P_SDI	PLL/ADC Slow Controls
K13	HA10_P	P_SDO	ADC Slow Controls
F13	HA12_P	LED0	GP LED
F14	HA12_N	LED1	GP LED
E12	HA13_P	LED2	GP LED
E13	HA13_N	LED3	GP LED
G31	LA29_N	P_DATA_P0	ADC Serial LVDS
G30	LA29_P	P_DATA_N0	ADC Serial LVDS
H32	LA28_N	P_DATA_P1	ADC Serial LVDS
H31	LA28_P	P_DATA_N1	ADC Serial LVDS
H29	LA24_N	P_DATA_P2	ADC Serial LVDS
H28	LA24_P	P_DATA_N2	ADC Serial LVDS
C27	LA27_N	P_DATA_P3	ADC Serial LVDS
C26	LA27_P	P_DATA_N3	ADC Serial LVDS
D27	LA26_N	P_DATA_P4	ADC Serial LVDS
D26	LA26_P	P_DATA_N4	ADC Serial LVDS
G25	LA22_N	P_DATA_P5	ADC Serial LVDS
G24	LA22_P	P_DATA_N5	ADC Serial LVDS
H26	LA21_N	P_DATA_P6	ADC Serial LVDS
H25	LA21_P	P_DATA_N6	ADC Serial LVDS
D24	LA23_N	P_DATA_P7	ADC Serial LVDS
D23	LA23_P	P_DATA_N7	ADC Serial LVDS
H23	LA19_N	P_DATA_P8	ADC Serial LVDS
H22	LA19_P	P_DATA_N8	ADC Serial LVDS
G22	LA20_N	P_DATA_P9	ADC Serial LVDS
G21	LA20_P	P_DATA_N9	ADC Serial LVDS
H20	LA15_N	P_DATA_P10	ADC Serial LVDS
H19	LA15_P	P_DATA_N10	ADC Serial LVDS

C23	LA18_N_CC	P_DATA_P11	ADC Serial LVDS
C22	LA18_P_CC	P_DATA_N11	ADC Serial LVDS
C19	LA14_N	P_DATA_P12	ADC Serial LVDS
C18	LA14_P	P_DATA_N12	ADC Serial LVDS
H17	LA11_N	P_DATA_P13	ADC Serial LVDS
H16	LA11_P	P_DATA_N13	ADC Serial LVDS
D17	LA13_P	P_DATA_P14	ADC Serial LVDS
D18	LA13_N	P_DATA_N14	ADC Serial LVDS
G16	LA12_N	P_DATA_P15	ADC Serial LVDS
G15	LA12_P	P_DATA_N15	ADC Serial LVDS
G13	LA08_N	P_DATA_P16	ADC Serial LVDS
G12	LA08_P	P_DATA_N16	ADC Serial LVDS
G10	LA03_N	P_DATA_P17	ADC Serial LVDS
G9	LA03_P	P_DATA_N17	ADC Serial LVDS
D15	LA09_N	P_DATA_P18	ADC Serial LVDS
D14	LA09_P	P_DATA_N18	ADC Serial LVDS
H14	LA07_N	P_DATA_P19	ADC Serial LVDS
H13	LA07_P	P_DATA_N19	ADC Serial LVDS
D12	LA05_N	P_DATA_P20	ADC Serial LVDS
D11	LA05_P	P_DATA_N20	ADC Serial LVDS
H11	LA04_N	P_DATA_P21	ADC Serial LVDS
H10	LA04_P	P_DATA_N21	ADC Serial LVDS
C11	LA06_N	P_DATA_P22	ADC Serial LVDS
C10	LA06_P	P_DATA_N22	ADC Serial LVDS
H8	LA02_N	P_DATA_P23	ADC Serial LVDS
H7	LA02_P	P_DATA_N23	ADC Serial LVDS
K11	HA06_N	P_DATA_P24	ADC Serial LVDS (16 channel only)
K10	HA06_P	P_DATA_N24	ADC Serial LVDS (16 channel only)
E7	HA05_N	P_DATA_P25	ADC Serial LVDS (16 channel only)
E6	HA05_P	P_DATA_N25	ADC Serial LVDS (16 channel only)
J10	HA07_N	P_DATA_P26	ADC Serial LVDS (16 channel only)
J9	HA07_P	P_DATA_N26	ADC Serial LVDS (16 channel only)
F11	HA08_N	P_DATA_P27	ADC Serial LVDS (16 channel only)
F10	HA08_P	P_DATA_N27	ADC Serial LVDS (16 channel only)
K8	HA02_N	P_DATA_P28	ADC Serial LVDS (16 channel only)
K7	HA02_P	P_DATA_N28	ADC Serial LVDS (16 channel only)
J7	HA03_N	P_DATA_P29	ADC Serial LVDS (16 channel only)
J6	HA03_P	P_DATA_N29	ADC Serial LVDS (16 channel only)
E10	HA09_N	P_DATA_P30	ADC Serial LVDS (16 channel only)
E9	HA09_P	P_DATA_N30	ADC Serial LVDS (16 channel only)
F8	HA04_N	P_DATA_P31	ADC Serial LVDS (16 channel only)
F7	HA04_P	P_DATA_N31	ADC Serial LVDS (16 channel only)
D20	LA17_P_CC	P_DCO_P0	ADC Serial LVDS
D21	LA17_N_CC	P_DCO_N0	ADC Serial LVDS
D8	LA01_P_CC	P_DCO_P1	ADC Serial LVDS
D9	LA01_N_CC	P_DCO_N1	ADC Serial LVDS
G6	LA00_P_CC	P_DCO_P2	ADC Serial LVDS

G7	LA00_N_CC	P_DCO_N2	ADC Serial LVDS
F4	HA00_P_CC	P_DCO_P3	ADC Serial LVDS (16 channel only)
F5	HA00_N_CC	P_DCO_N3	ADC Serial LVDS (16 channel only)
G28	LA25_N	P_FR_P0	ADC Serial LVDS
G27	LA25_P	P_FR_N0	ADC Serial LVDS
G19	LA16_N	P_FR_P1	ADC Serial LVDS
G18	LA16_P	P_FR_N1	ADC Serial LVDS
C15	LA10_N	P_FR_P2	ADC Serial LVDS
C14	LA10_P	P_FR_N2	ADC Serial LVDS
E3	HA01_N_CC	P_FR_P3	ADC Serial LVDS (16 channel only)
E2	HA01_P_CC	P_FR_N3	ADC Serial LVDS (16 channel only)

The following table describes exact pinout of front-panel analog connector with additional info of limitations of 4 and 8 channel versions.

ARF6 Pin	Name	Compatibility Info
39	A_IN_P0	Analog Channel 0
41	A_IN_N0	Analog Channel 0
46	A_IN_P1	Analog Channel 1
48	A_IN_N1	Analog Channel 1
27	A_IN_P2	Analog Channel 2
29	A_IN_N2	Analog Channel 2
34	A_IN_P3	Analog Channel 3
36	A_IN_N3	Analog Channel 3
22	A_IN_P4	Analog Channel 4
24	A_IN_N4	Analog Channel 4
10	A_IN_P5	Analog Channel 5
12	A_IN_N5	Analog Channel 5
15	A_IN_P6	Analog Channel 6
17	A_IN_N6	Analog Channel 6
3	A_IN_P7	Analog Channel 7
5	A_IN_N7	Analog Channel 7
1	GND	Signal Ground
2	GND	Signal Ground
4	GND	Signal Ground
6	GND	Signal Ground
7	GND	Signal Ground
8	GND	Signal Ground
9	GND	Signal Ground
11	GND	Signal Ground
13	GND	Signal Ground
14	GND	Signal Ground
16	GND	Signal Ground
18	GND	Signal Ground
19	GND	Signal Ground

20	GND	Signal Ground
21	GND	Signal Ground
23	GND	Signal Ground
25	GND	Signal Ground
26	GND	Signal Ground
28	GND	Signal Ground
30	GND	Signal Ground
31	GND	Signal Ground
32	GND	Signal Ground
33	GND	Signal Ground
35	GND	Signal Ground
37	GND	Signal Ground
38	GND	Signal Ground
40	GND	Signal Ground
42	GND	Signal Ground
43	GND	Signal Ground
44	GND	Signal Ground
45	GND	Signal Ground
47	GND	Signal Ground
49	GND	Signal Ground
50	GND	Signal Ground

ARF6 Pin Number	SMT-FMC116 Function	Compatibility Info

12 Support Packages

The board is delivered with **VHDL-based board support packages (BSPs)**, compatible with selected **Xilinx Evaluation Boards** from the **7-Series** and **UltraScale** families. The BSP includes modules for configuring the high-speed data interface to the ADCs, controlling the on-board clock distribution system, and interfacing with the trigger inputs.

13 Physical Properties

Dimensions		Typical	Max
Weight			
Supply Voltages			
Supply Current	+12V		
	+3.3V		
	VADJ		
MTBF			

14 Safety

This module presents no hazard to the user when used normally.

15 EMC

This module is intended for operation within an **enclosed host system** that provides proper **EMC shielding**. Compliance with **EU EMC regulations** is not guaranteed unless the module is installed in a suitably shielded enclosure.

The module includes protection circuitry against **fast voltage transients** that may be introduced through external cables connected to the outputs.

Additionally, **short-circuiting any output to ground** does not cause the host PC system to lock up or reboot, ensuring robust system behavior under fault conditions.