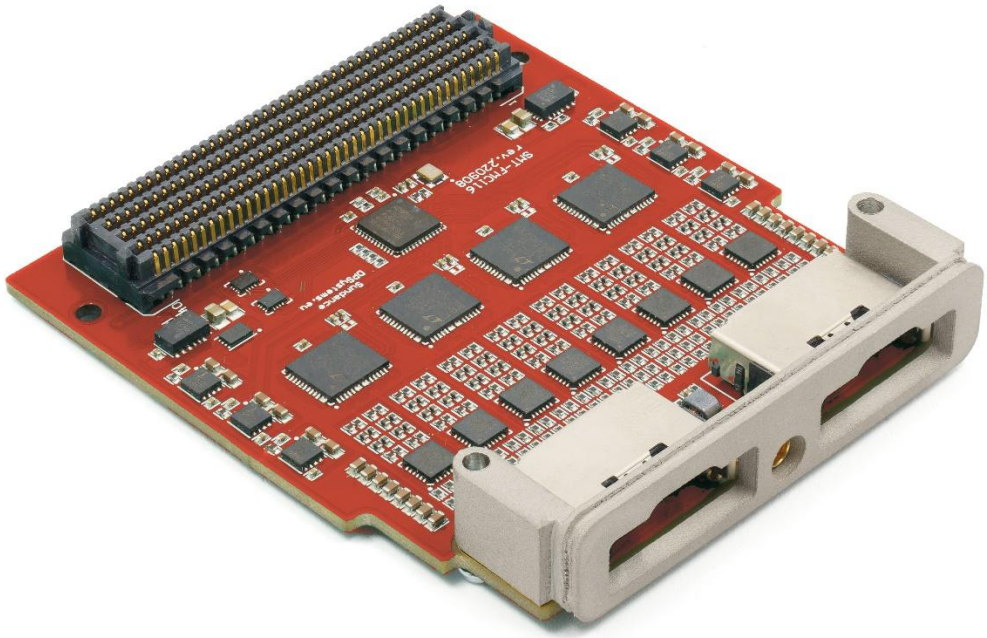
Unit / Module Description:	16-channel, 14-bit ADC FMC module (VITA 57.1)
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User Guide for *SMT-FMC116*



16-channel ADC FMC Module
Hardware revision Rev1

Revision History

Issue	Changes Made	Date	Initials
1.0	First release	06.11.2026	WJ
1.1	Standard assembly LTC2175-14, variant table and assembly options; PLL configuration notes; serialization modes; figure updates; corrected power-status LED assignments and shared clock-divider phase description; clarified startup, voltage monitoring, analog input limits and bandwidth, and 12-bit serialization; added BSP overview with ZCU102/ZCU104 and Trenz TE0813 full-HPC, 16-channel examples	07.11.2026	WJ
1.11	Added Sundance GitHub HyperLink	08.11.2026	FC

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1 Introduction

The SMT-FMC116 is a general-purpose multi-channel digitizer on an FPGA Mezzanine Card (FMC, ANSI/VITA 57.1). Rev1 provides up to 16 fully differential analog inputs, DC or AC coupled. Four quad-channel ADCs sample them, and an AD9518 PLL / clock distribution device clocks the ADCs. The carrier FPGA receives the samples over high-speed serial LVDS links on the FMC connector. It configures the ADCs and the clock generator over SPI.

Product variants scale the board to the intended application in resolution and sample rate. The ADC footprint takes any member of the pin-compatible LTC217x quad ADC family:

Sample rate	14 bit	12 bit
125 MSPS	LTC2175-14	LTC2175-12
105 MSPS	LTC2174-14	LTC2174-12
80 MSPS	LTC2173-14	LTC2173-12
65 MSPS	LTC2172-14	LTC2172-12
40 MSPS	LTC2171-14	LTC2171-12
25 MSPS	LTC2170-14	LTC2170-12

The standard Rev1 assembly uses LTC2175-14 (14 bit, 125 MSPS).

1.1 Key features

The table summarizes the main features of the Rev1 module.

Feature	Rev1 implementation
Analog inputs	16 differential channels on two Samtec ARF6-RA connectors (J13A: A0–A7, J13B: B0–B7)
Input coupling	DC or AC (10 nF), selected by assembly
Front end	ADA4938-2 fully differential amplifiers, gain ≈ 1.5 V/V, ~50 MHz anti-alias low-pass filter
ADC	4 × LTC2175-14 (quad, 14 bit, 125 MSPS). Other LTC217x variants: 12 or 14 bit, 25–125 MSPS.
Data interface	2-lane serial LVDS per channel, 32 data pairs + 4 DCO + 4 frame pairs
Clocking	AD9518-0 PLL with integrated VCO. Sources: 25 MHz on-board oscillator, external MMCX clock (PLL bypass) or a reference from the FPGA (only with VADJ ≥ 2.5 V, HPC).
Trigger	U.FL trigger input, forwarded to the FPGA as LVDS on CLK1_M2C
Control	SPI (ADCs and PLL) from the carrier through VADJ-referenced FMC pins
Management	FMC I²C: ID EEPROM (M24C02) and voltage monitor (LTC2991)
Indicators	2 power-status LEDs, 4 user LEDs driven by the carrier
FMC	HPC connector. 12 channels (ADC0–ADC2) are usable on an LPC carrier (see 6.6).
Supplies used	12P0V, 3P3VAUX, VADJ (the FMC 3P3V pins are not used)

1.2 Block diagram

Figure 1 shows the main functional blocks and the signal paths between the analog inputs, the ADCs, the clock generator and the FMC connector. The following chapters describe each block in detail.

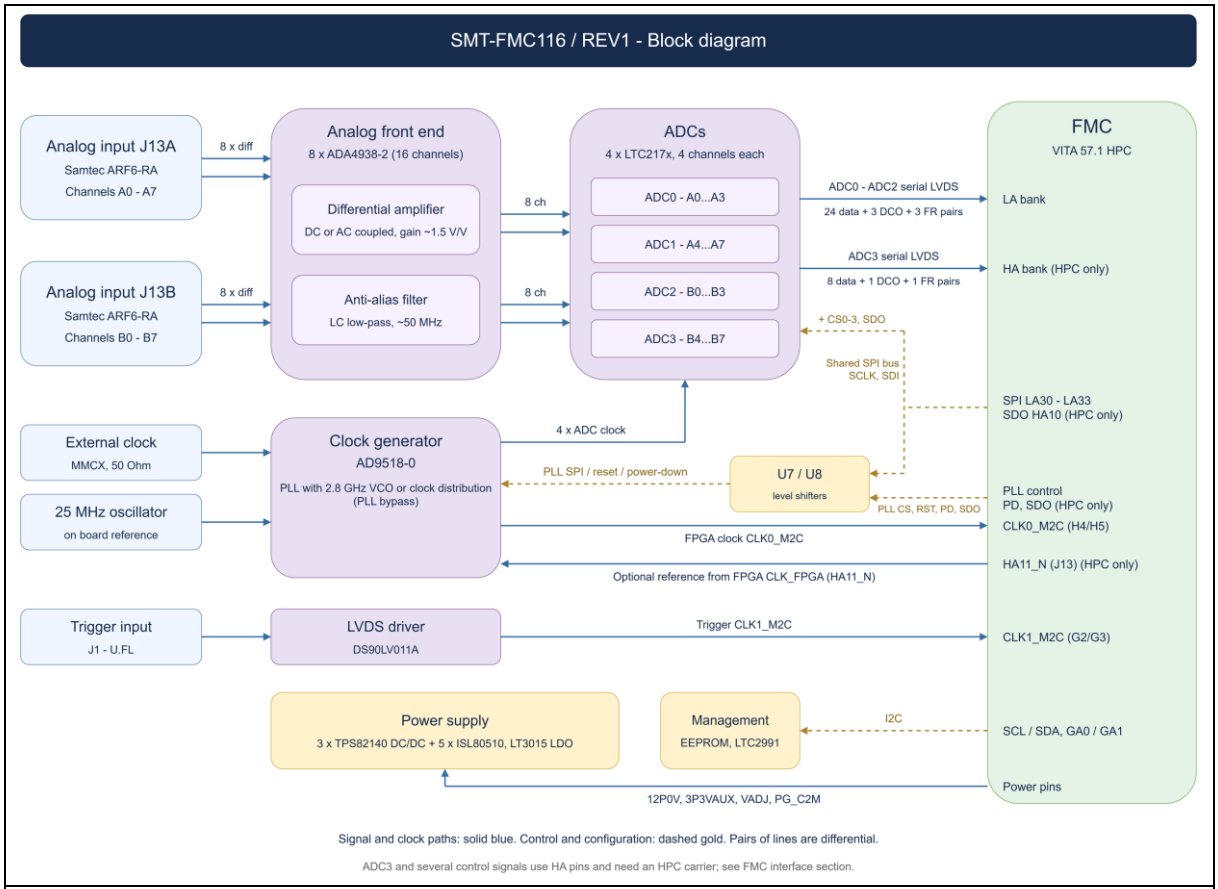


Figure 1 - Block diagram

Signal flow:

1. The analog signals enter on the two front-panel ARF6 connectors. Adapters from ARF6 to SMA (single-ended or differential) are available as separate products.
2. Each channel is buffered, scaled and low-pass filtered by a fully differential amplifier stage.
3. Four quad ADCs convert the 16 channels. Each ADC streams its data over 8 LVDS lanes, together with a bit clock (DCO) and a frame signal (FR). ADC0–ADC2 use the FMC LA bank; ADC3 uses the HA bank, which is available on HPC carriers only.
4. The AD9518 generates the four ADC sample clocks and one clock to the FPGA.
5. The carrier FPGA configures the ADCs and the AD9518 over **one shared SPI bus**. SCLK and SDI are common to all devices, and separate chip selects pick the device (P_CS0–P_CS3 for the ADCs, FMC_CS_N for the PLL). The ADCs are connected directly at VADJ levels. The PLL runs at 3.3 V and is reached through the U7/U8 level shifters, which also carry the PLL reset, power-down and SDO signals.
6. The carrier receives the serial data and reads board status over I²C.

1.3 Getting started

To bring up the module:

1. Install the module on an FMC HPC carrier (LPC: see 6.6). VADJ must suit the FPGA bank receiving the LVDS data (typically 1.8 V or 2.5 V). The module's ID

EEPROM holds a VITA 57.1 FRU record with the supply requirements in the MultiRecord area, so a carrier that reads it can set VADJ automatically. Otherwise set VADJ manually.

2. Power the carrier. The module's DC/DC converters start only when the carrier asserts **PG_C2M**. When all rails are up, the two status LEDs light (see 2.4).
3. Configure the AD9518 over SPI: select the clock source, PLL settings and output dividers (section 3). In PLL mode, allow the PLL to settle and verify lock through SPI where read-back is available. In external-clock distribution mode, no PLL lock is required.
4. Configure the four ADCs over SPI (section 5). Optionally enable an ADC test pattern to align the LVDS receivers in the FPGA.
5. Apply the analog signals and capture data.

The board support package (VHDL, for selected AMD/Xilinx 7-Series and UltraScale evaluation boards) contains the ADC data-interface, clock-configuration and trigger modules.

2 Power section

The module is powered entirely from the FMC connector. On-board converters derive all analog, ADC and clock supplies from the carrier's 12 V rail. Figure 2 shows the power distribution.

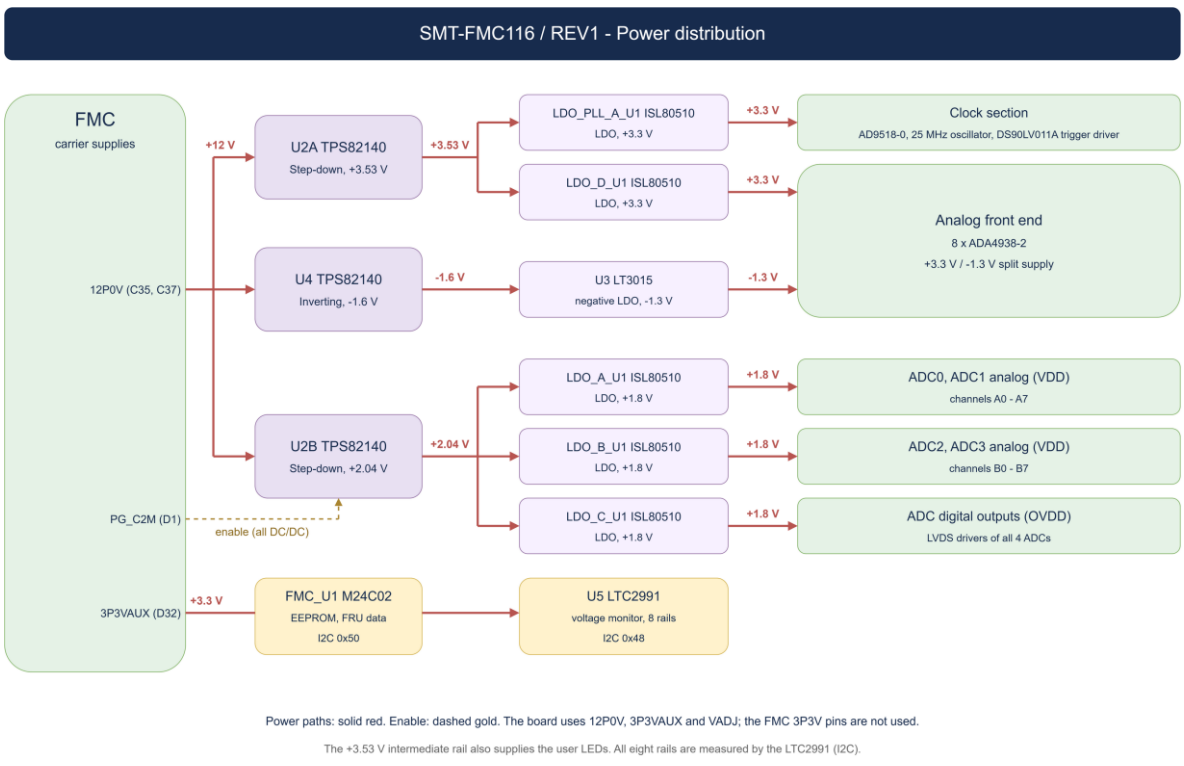


Figure 2 - Power distribution

2.1 Supplies from the carrier

The module uses the following FMC supplies:

FMC supply	Pins	Used for
12P0V	C35, C37	Input of all on-board DC/DC converters, power-status LEDs

FMC supply	Pins	Used for
3P3VAUX	D32	FRU EEPROM (M24C02, VITA 57.1 module ID), LTC2991 voltage monitor
VADJ	E39, F40, G39, H40	FMC I/O level of the SPI and control signals
3P3V	D36, D38, D40, C39	**Not used**

The carrier must provide 12P0V. All analog and ADC supplies come from it.

2.2 Power-up control

The three TPS82140 converters are enabled by **PG_C2M** (FMC pin D1). A pull-down on the module keeps them off until the carrier drives PG_C2M high. That happens after the carrier's own supplies, including VADJ, are valid.

The module does not provide the VREF_x_M2C and VIO_B_M2C voltages to the carrier, so PG_M2C (FMC pin F1), which signals that they are valid, is not used. To check the on-board supplies, use the LTC2991 monitor (2.5) or the status LEDs.

2.3 On-board rails

Power is converted in two stages. Three TPS82140 step-down modules convert 12 V into intermediate rails. Low-noise LDOs then produce the rails used by the analog and mixed-signal circuits.

Stage 1 (DC/DC)	Intermediate rail	Stage 2 (LDO)	Final rail	Supplies
U2A TPS82140	+3.53 V	LDO_PLL_A_U1 ISL80510	+3.3 V	AD9518, 25 MHz oscillator, trigger LVDS driver
		LDO_D_U1 ISL80510	+3.3 V	Front-end amplifiers, positive supply
		(direct)	+3.53 V	User LEDs
U4 TPS82140 (inverting)	–1.6 V	U3 LT3015	≈ –1.3 V	Front-end amplifiers, negative supply
U2B TPS82140	+2.04 V	LDO_A_U1 ISL80510	+1.8 V	ADC0 and ADC1 analog supply (channels A0–A7)
		LDO_B_U1 ISL80510	+1.8 V	ADC2 and ADC3 analog supply (channels B0–B7)
		LDO_C_U1 ISL80510	+1.8 V	Digital output supply (OVDD) of all four ADCs

The front-end amplifiers run from a split supply. In the standard assembly the negative rail is set to about –1.3 V, giving the amplifiers a total supply of about 4.6 V. The negative supply level is an assembly option. It trades input signal range and distortion against power dissipation.

2.4 Power-status LEDs

Two LEDs show the state of the on-board supplies:

LED	Lights when
FMC_D5	The +1.8 V ADC output supply (LDO_C) is present. It is the last rail in the chain, so the LED indicates that all supplies are up.

LED	Lights when
FMC_D6	Power-good of the two positive DC/DC converters (U2A, U2B): the intermediate supplies are within specification

2.5 Voltage monitoring

An LTC2991 (U5) on the FMC I²C bus measures eight on-board rails. Its I²C address is 0x48 (7-bit, ADR2..0 = 000). Some inputs are scaled by resistor dividers:

LTC2991 input	Rail	Scaling (rail voltage from reading V)
V1	≈ –1.3 V, front-end negative supply (U3)	Level-shifted from 3P3VAUX: V_rail = (139 × V – 100 × V_3P3VAUX) / 39
V2	+3.3 V, front-end positive supply (LDO_D)	V_rail = 2 × V
V3	+2.04 V, intermediate (U2B)	V_rail = V
V4	+1.8 V, ADC2/ADC3 analog (LDO_B)	V_rail = V
V5	+1.8 V, ADC0/ADC1 analog (LDO_A)	V_rail = V
V6	+1.8 V, ADC digital outputs (LDO_C)	V_rail = V
V7	+3.3 V, clock section (LDO_PLL_A)	V_rail = 2 × V
V8	+3.53 V, intermediate (U2A)	V_rail = 1.2 × V

Use single-ended voltage measurement mode. The LTC2991 is powered from 3P3VAUX, so it can be read before PG_C2M is asserted. Apply the scaling equations to recover rail voltages; the level-shifted V1 input does not itself read approximately zero when the negative rail is off.

3 Clock distribution

A single PLL / clock distribution device generates the sample clocks of all four ADCs. It can also supply a clock to the FPGA. Figure 3 shows the clock paths.

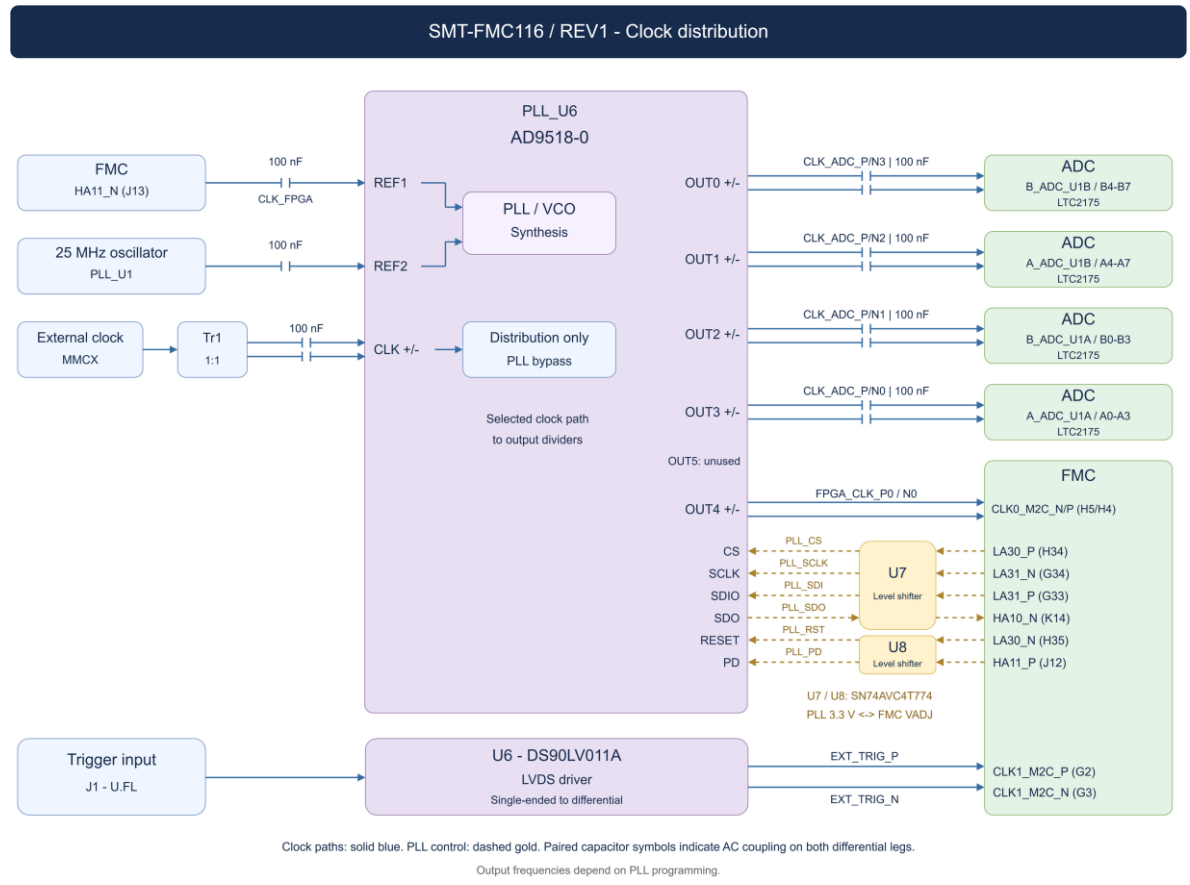


Figure 3 - Clock distribution

3.1 Overview

The Analog Devices AD9518-0 (PLL_U6) is the central clock device. It contains a PLL with an integrated VCO (2.55–2.95 GHz range), a VCO divider and three output divider groups with LVPECL outputs. It can either synthesize the sample clock from a reference (PLL mode) or divide and distribute an external clock directly (distribution mode, PLL bypassed).

The VCO range limits which sample clocks the PLL can synthesize: the clock must be the VCO frequency divided by the available VCO and output dividers. Analog Devices offers the AD9518 in several versions with different VCO ranges:

Device	VCO range
AD9518-0 (standard)	2.55–2.95 GHz
AD9518-1	2.30–2.65 GHz
AD9518-2	2.05–2.33 GHz
AD9518-3	1.75–2.25 GHz
AD9518-4	1.45–1.80 GHz

If your application needs a sample clock that the standard AD9518-0 cannot generate, contact sales about an assembly with another AD9518 version.

The on-board PLL loop filter is optimized for a phase-frequency detector (PFD) frequency of up to 10 MHz. When using a custom PLL configuration, choose the R

divider so that the PFD frequency (reference ÷ R) does not exceed 10 MHz. The supplied setup files use R = 5, i.e. 5 MHz from the 25 MHz oscillator.

3.2 Clock sources

The AD9518 can take its reference or clock from three sources:

Source	Connection	AD9518 input	Use
25 MHz on-board oscillator (PLL_U1)	AC coupled	REF2	Default reference for PLL synthesis
External clock, MMCX (PLL_J1), front panel	50 Ω, 1:1 transformer (Tr1), AC coupled, differential	CLK ±	Distribution mode: the external clock is divided and distributed with the PLL bypassed
FPGA clock CLK_FPGA (FMC HA11_N, J13)	AC coupled	REF1	Alternative PLL reference, mainly for debugging and testing. Usable only with VADJ ≥ 2.5 V. HPC only.

In distribution mode the external clock must be at the sample rate or an integer multiple of it, within the AD9518 CLK input range (see the AD9518-0 datasheet for level and frequency limits).

3.3 Clock outputs

The AD9518 outputs are assigned as follows:

AD9518 output	Signal	Source standard	Destination	Destination standard	Coupling
OUT3	CLK_ADC_P/N0	LVPECL	ADC0 (A_ADC_U1A), channels A0–A3	Differential encode input (self-biased)	AC, 100 nF
OUT2	CLK_ADC_P/N1	LVPECL	ADC1 (B_ADC_U1A), channels A4–A7	Differential encode input (self-biased)	AC, 100 nF
OUT1	CLK_ADC_P/N2	LVPECL	ADC2 (A_ADC_U1B), channels B0–B3	Differential encode input (self-biased)	AC, 100 nF
OUT0	CLK_ADC_P/N3	LVPECL	ADC3 (B_ADC_U1B), channels B4–B7	Differential encode input (self-biased)	AC, 100 nF
OUT4	FPGA_CLK_P0/N0	LVPECL, attenuated to LVDS levels	FPGA, FMC CLK0_M2C (H4/H5), **P/N swapped**	LVDS	DC
OUT5	—	—	Unused	—	—

The ADC clocks are arranged in two groups sharing output-divider frequency and phase settings: ADC0/ADC1 (OUT3/OUT2) and ADC2/ADC3 (OUT1/OUT0). OUT4 provides the FPGA with a clock that is frequency-locked to the ADC sample clock. Its LVPECL output is converted to LVDS-compatible levels on the module (series and shunt resistor divider, ≈ 1.25 V common mode, ≈ 0.5 V swing). There is no 100 Ω termination on the module, so enable the differential termination of the FPGA input (e.g. DIFF_TERM on AMD/Xilinx devices). FPGA_CLK_P0 is routed to the CLK0_M2C_N pin and FPGA_CLK_N0 to CLK0_M2C_P, so invert it in the FPGA if the phase matters.

3.4 PLL control

The AD9518 is configured over SPI from the carrier. The PLL runs at 3.3 V and the FMC side at VADJ, so the control signals pass through two SN74AVC4T774 level shifters (U7, U8).

Function	AD9518 pin	FMC signal	FMC pin
Chip select	CS	FMC_CS_N	H34 (LA30_P)
Serial clock	SCLK	P_SCLK (shared with the ADCs)	G34 (LA31_N)
Serial data in	SDIO	P_SDI (shared with the ADCs)	G33 (LA31_P)
Serial data out	SDO	FMC_SDO	K14 (HA10_N), HPC only
Reset (active low)	RESET	FMC_RESET_N	H35 (LA30_N)
Power-down (active low)	PD	FMC_PD_N	J12 (HA11_P), HPC only

FMC_CS_N, FMC_RESET_N and FMC_PD_N are pulled up to VADJ on the module. If the carrier leaves them undriven, the PLL is deselected, out of reset and powered up. The SDIO path through the level shifter is one-way. To read registers back, configure the AD9518 for 4-wire SPI (SDO enabled in register 0x000) and read on FMC_SDO.

3.5 Configuration files

The PLL configuration can be prepared with the Analog Devices AD9516/AD9517/AD9518 evaluation software (select AD9518-0). Figure 4 shows the tool with the supplied 125 MHz configuration.

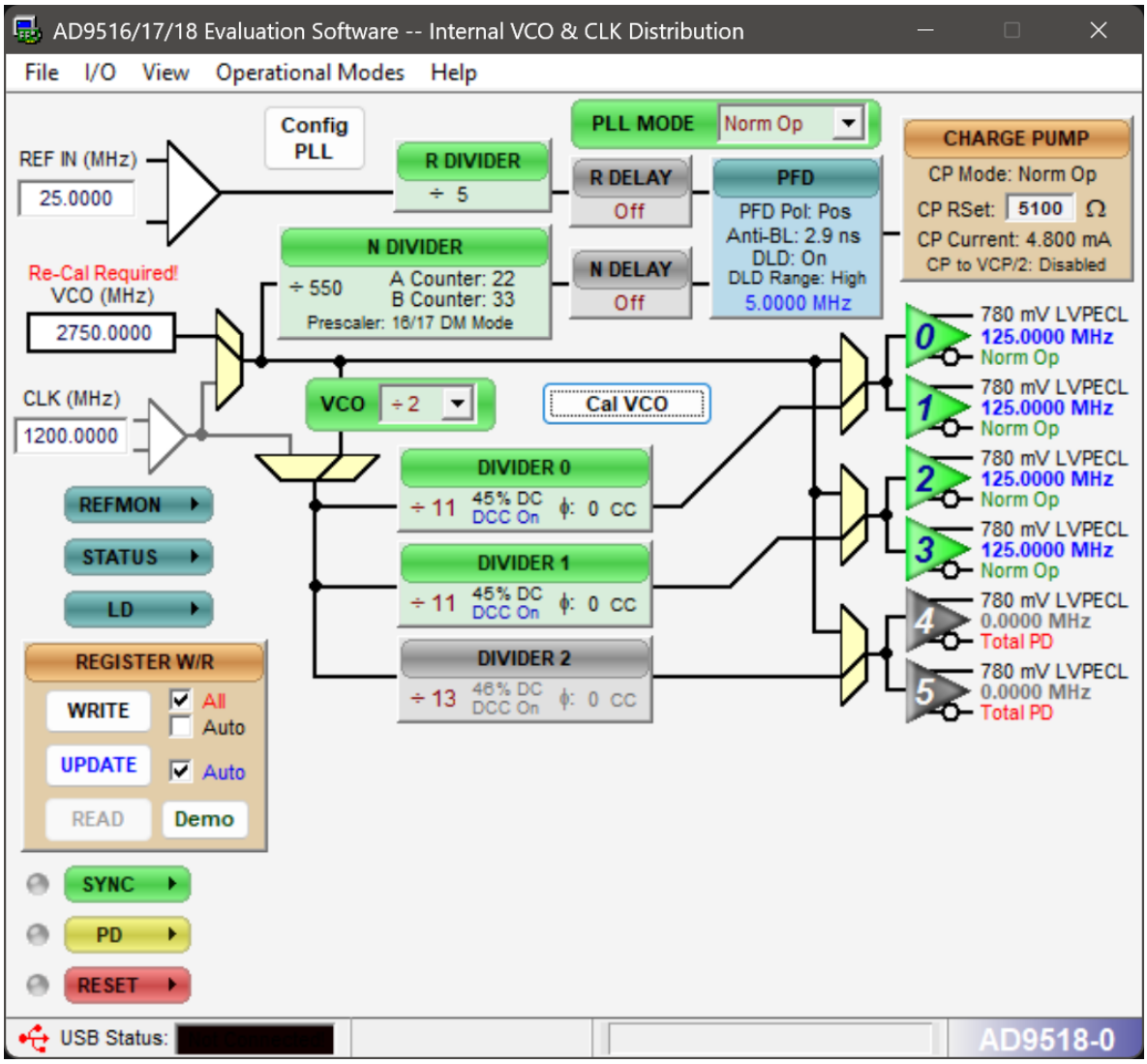


Figure 4 - AD9518 configuration in the evaluation software (125 MHz setup)

Setup files saved from the tool contain the register contents as HEX data (address and value per register). The carrier FPGA writes this data to the AD9518 over SPI. The board support package provides a function that shows how to send the register data to the PLL.

Two example setup files for the 25 MHz on-board reference are supplied with the design data:

File	VCO	ADC clock (OUT0–OUT3)
`fmc116.pll_100MHz.stp`	2600 MHz	100 MHz
`fmc116.pll_125MHz.stp`	2750 MHz	125 MHz

In both files OUT4 (FPGA clock) and OUT5 are powered down. OUT5 is not used on the board and must stay powered down at all times, including in custom configurations. To use the FPGA clock, enable OUT4 (register 0x0F4) and set divider 2 for the required frequency. The 125 MHz setting is the maximum for the standard LTC2175-14 assembly. On variants with slower ADCs, keep the ADC clock at or below the rated sample rate of the fitted part.

3.6 Trigger input

The trigger path is independent of the PLL:

- **Connector:** J1, U.FL, near the FMC connector. Use a U.FL-to-MMCX cable to bring it to the front panel.
- **Termination:** optional 50 Ω to ground. Input protected by an ESD diode.
- **Signal:** 3.3 V LVTTL/LVCMOS compatible. Do not exceed 3.3 V.
- **To the carrier:** U6 (DS90LV011A) converts the trigger to LVDS. It reaches the FPGA as EXT_TRIG_P/N on CLK1_M2C_P/N (G2/G3), with no polarity swap.

4 Analog input stage

Each of the 16 analog inputs passes through an identical front end that buffers and scales the signal, converts it to differential and filters it before the ADC. Figure 5 shows one channel.

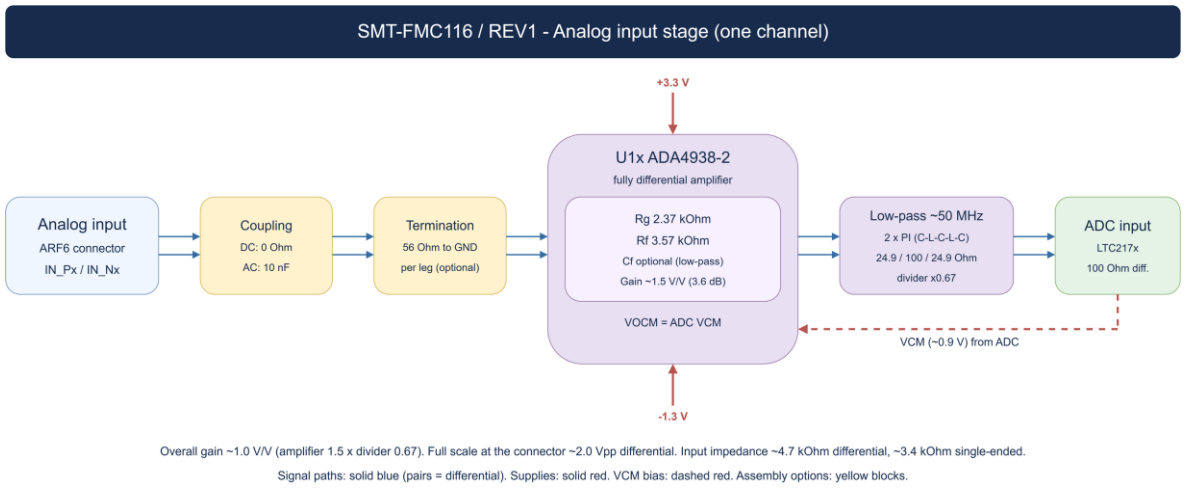


Figure 5 - Analog input stage, one channel

4.1 Description

All 16 channels are identical. Each channel uses one half of an ADA4938-2 dual fully differential amplifier (U1A–U1H: 8 devices for 16 channels):

1. **Coupling:** DC (0 Ω series links) or AC (10 nF series capacitors), selected by assembly option.
2. **Termination:** After the coupling element, each input leg has an optional 56 Ω shunt resistor to ground. Without it, the input is high impedance; with it, the input matches a 50 Ω system.
3. **Gain:** Rg = 2.37 kΩ and Rf = 3.57 kΩ give a gain of ≈ 1.5 V/V (3.6 dB).
4. **Common mode:** The ADC VCM output sets the amplifier output common mode (VOCM) to approximately 0.9 V. The applied signal must remain within the front end's permitted input common-mode and output-swing limits.
5. **Anti-alias filter:** 24.9 Ω series resistors followed by two cascaded PI sections (C-L-C-L-C, 5th order) with ~50 MHz cut-off. The series resistors and the 100 Ω load at the ADC form a 24.9 / 100 / 24.9 Ω divider (×0.67), so the overall gain from connector to ADC is ≈ 1.0 V/V. This suits the first Nyquist zone at 125 MSPS (62.5 MHz). At lower sample rates, restrict the input bandwidth or provide additional filtering appropriate to the selected Nyquist band.

6. **ADC load:** 100 Ω differential at the ADC input.

4.2 Input characteristics

The main input characteristics are:

Parameter	Value
Coupling	DC or AC (10 nF), assembly option
Input type	Differential, or single-ended with the unused input grounded
Input impedance	Unterminated: ≈ 4.7 kΩ differential, ≈ 3.4 kΩ single-ended. With 56 Ω termination: ≈ 110 Ω differential, ≈ 55 Ω single-ended.
Gain to ADC	≈ 1.0 V/V (amplifier 1.5 V/V × output divider 0.67)
Full-scale input	≈ 2.0 Vpp differential (ADC full scale 2 Vpp ÷ 1.0)
Bandwidth	DC-coupled: DC to approximately 50 MHz. AC-coupled: lower cutoff depends on coupling capacitors, termination and source impedance; upper cutoff approximately 50 MHz.
Input common mode	Ground-referenced signals expected

4.3 Using the inputs

- **Differential sources:** Drive IN_Px and IN_Nx symmetrically. Use the differential ARF6-to-SMA adapter.
- **Single-ended sources:** Drive IN_Px and connect IN_Nx to ground (the single-ended ARF6-to-SMA adapter does this). The amplifier converts the signal to differential. The full-scale amplitude on IN_Px is the same, ≈ 2.0 Vpp (±1 V around ground).
- **50 Ω systems:** With the 56 Ω termination option the input matches a 50 Ω source. Unterminated inputs are high impedance: a 50 Ω source then delivers twice its nominal (50 Ω-loaded) amplitude, and cable reflections are not absorbed. In that case terminate externally (e.g. a 50 Ω feed-through).
- **Overdrive:** Signals beyond full scale clip in the ADC. Keep the input within the amplifier supply rails (+3.3 V / ≈ –1.3 V) at all times.

4.4 Assembly options

The front end can be adapted to the application by assembly options:

Option	Choices
Input coupling	DC (0 Ω) or AC (10 nF series capacitors)
Input termination	None (high impedance) or 56 Ω per leg to ground (≈ 50 Ω system match)
Feedback capacitors	None, or a capacitor across Rf (amplifier low-pass)
Negative amplifier supply	≈ –1.3 V standard; adjustable for larger input range or better distortion, at higher power

4.5 Analog connector pinout

J13A carries channels A0–A7 and J13B channels B0–B7, with identical pin numbering. All other pins are ground.

Channel (J13A / J13B)	IN_P pin	IN_N pin
A0 / B0	39	41
A1 / B1	46	48
A2 / B2	27	29
A3 / B3	34	36
A4 / B4	22	24

Channel (J13A / J13B)	IN_P pin	IN_N pin
A5 / B5	10	12
A6 / B6	15	17
A7 / B7	3	5

4.6 Simulation models

LTspice simulation files of the analog input stage are provided as part of the board support package. Use them to evaluate gain, bandwidth and the effect of the assembly options (coupling, termination, feedback capacitors) for your application.

5 ADC

Four quad-channel ADCs digitize the 16 channels and send the samples to the FPGA over serial LVDS. Figure 6 shows the ADC section with its clock, data and control connections.

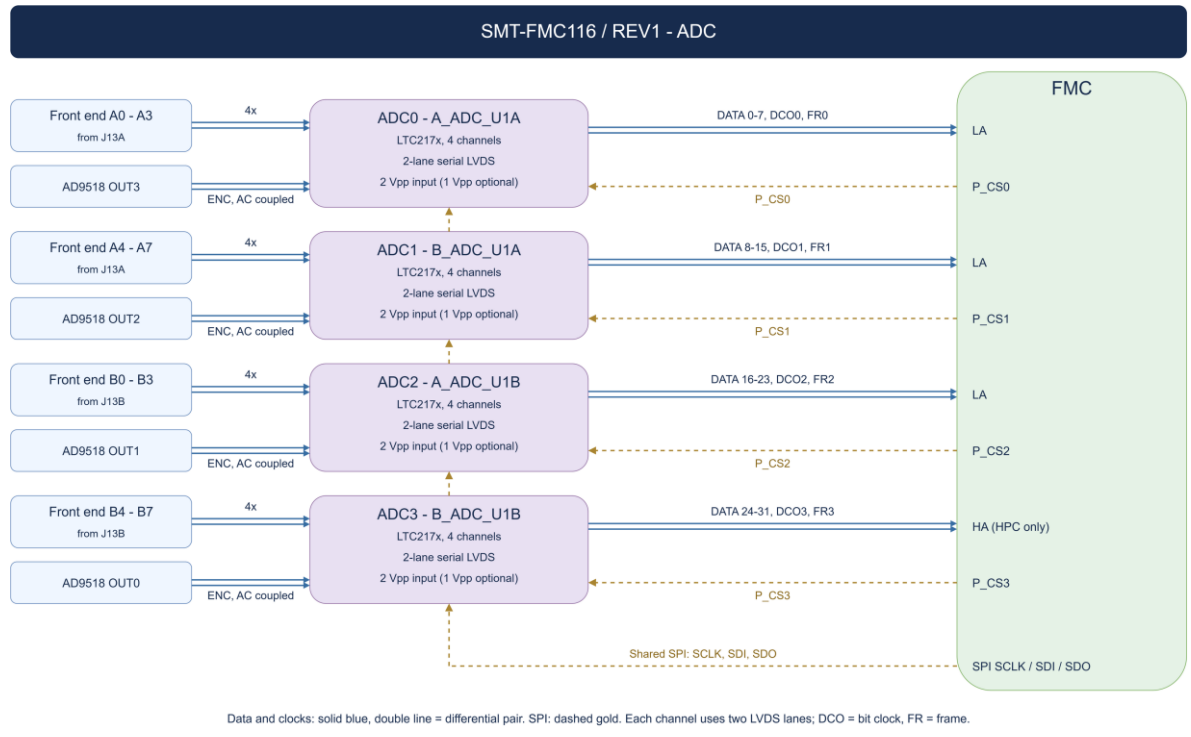


Figure 6 - ADC section

5.1 Devices

The standard module uses four LTC2175-14 quad-channel ADCs (14 bit, 125 MSPS). They belong to the LTC217x family, which shares one footprint. The board can be built with any family member, 12 or 14 bit, 25–125 MSPS (see the variant table in section 1). Check the assembly variant of your module.

ADC	Designator	Channels (ADC input 1–4)	Clock	SPI chip select	Analog supply
ADC0	A_ADC_U1A	A0, A1, A2, A3	AD9518 OUT3	P_CS0	+1.8 V (LDO_A)
ADC1	B_ADC_U1A	A4, A5, A6, A7	AD9518 OUT2	P_CS1	+1.8 V (LDO_A)

ADC	Designator	Channels (ADC input 1–4)	Clock	SPI chip select	Analog supply
ADC2	A_ADC_U1B	B0, B1, B2, B3	AD9518 OUT1	P_CS2	+1.8 V (LDO_B)
ADC3	B_ADC_U1B	B4, B5, B6, B7	AD9518 OUT0	P_CS3	+1.8 V (LDO_B)

5.2 Hardware configuration

Some ADC settings are fixed by hardware:

Setting	Configuration on Rev1
Programming mode	Serial (SPI). PAR/SER is tied to ground.
Input range	2 Vpp differential (SENSE tied to VDD, internal reference). 1 Vpp is an assembly option (SENSE to GND).
Encode clock	Differential, AC coupled from the AD9518
Output supply (OVDD)	1.8 V (LDO_C)

5.3 Data interface

Each channel is serialized onto two LVDS lanes (OUTxA and OUTxB, "2-lane mode"). Per ADC there are:

- 8 data lanes (4 channels × 2 lanes)
- DCO: the data clock output (DDR bit clock)
- FR: the frame signal marking sample word boundaries

The board support package uses 2-lane, 16-bit serialization (the ADC default). It has the highest lane rate of the 2-lane modes: 8 × f_s per lane, i.e. 1 Gb/s at 125 MSPS (DCO 500 MHz), and proportionally less for slower variants. User applications can select another serialization mode over SPI to lower the lane and DCO rates in the FPGA:

Mode (2-lane)	Lane rate	At 125 MSPS	DCO at 125 MSPS
16-bit serialization (BSP)	8 × f_s	1000 Mb/s	500 MHz
14-bit serialization	7 × f_s	875 Mb/s	437.5 MHz
12-bit serialization	6 × f_s	750 Mb/s	375 MHz

12-bit serialization is also available on the 14-bit ADC variants; in this mode, the two least-significant bits are omitted.

The FPGA receives each ADC as an independent source-synchronous link, deserializes using DCO and aligns words using FR. The ADC test patterns (fixed and alternating) are useful for link training.

Most data and frame pairs are routed with P and N swapped at the FMC connector (see 6.3). The BSP compensates for these swaps. Custom FPGA designs must invert the swapped lanes.

5.4 SPI control

The four ADCs share one SPI bus with the AD9518 (see 3.4). Each ADC has its own chip select:

Signal	Direction	FMC pin	Notes
P_SCLK	Carrier → ADCs, PLL	G34 (LA31_N)	Shared by all four ADCs and the AD9518
P_SDI	Carrier → ADCs, PLL	G33 (LA31_P)	Shared
P_CS0…P_CS3	Carrier → ADC0…ADC3	H38, G37, H37, G36 (LA32_N, LA33_N, LA32_P, LA33_P)	Active low, pulled up to VADJ
P_SDO	ADCs → carrier	K13 (HA10_P)	Shared open-drain read-back, 2.2 kΩ pull-up to VADJ. HPC only.

The ADC SPI pins are driven directly at VADJ levels. Select one ADC (or the PLL with FMC_CS_N) at a time. Configuration writes are possible on LPC carriers, but read-back needs HPC.

6 FMC interface

This chapter lists the module's connections to the carrier on the FMC connector. Figure 7 gives an overview of the signal groups and the FMC banks they use.

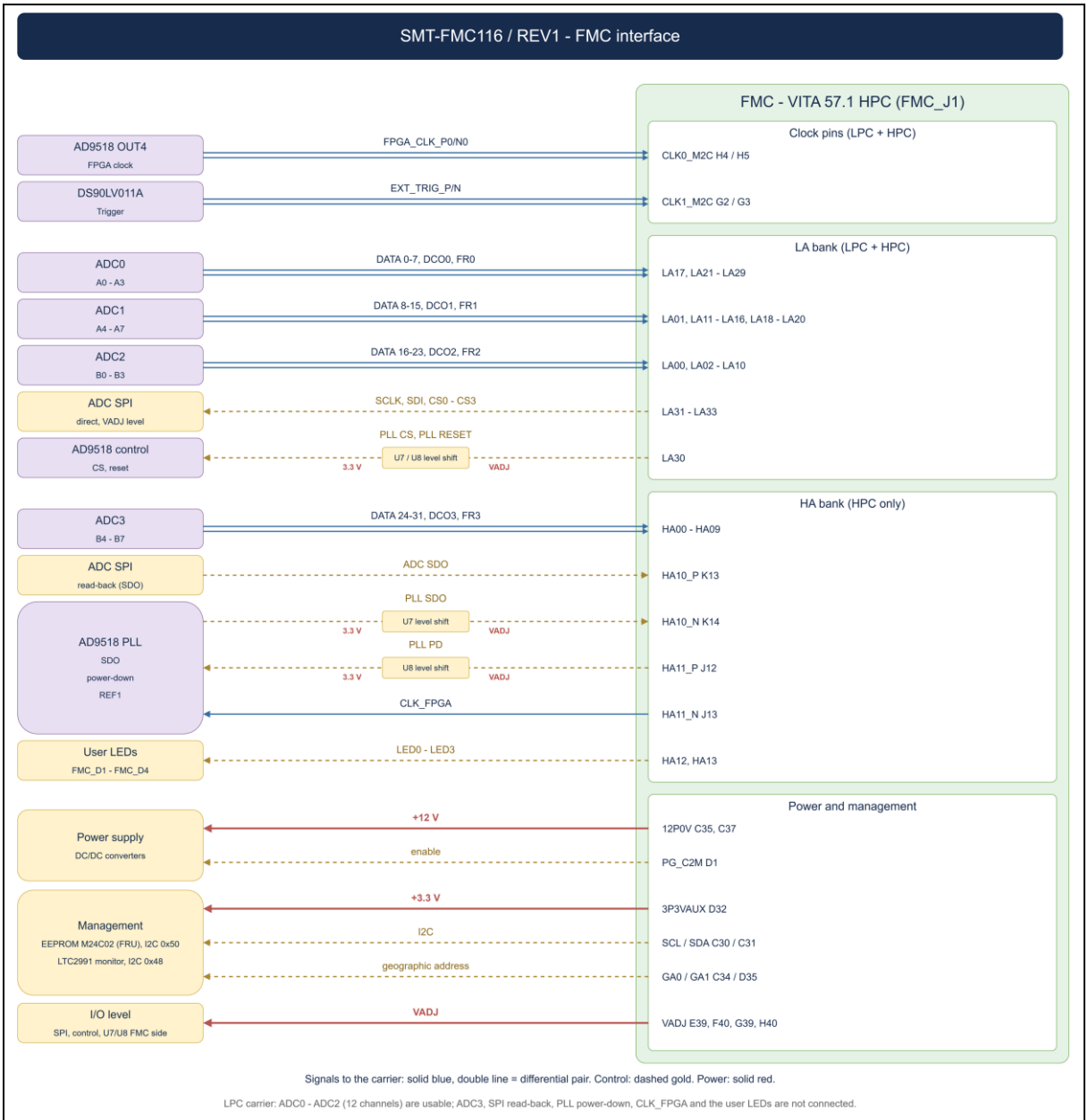


Figure 7 - FMC interface

6.1 General

The module is a single-width VITA 57.1 FMC with an HPC connector (Samtec ASP-134488-01, 10 mm stacking height) and a standard front-panel bezel. Other stacking heights are available on request as assembly options. All single-ended control signals use VADJ levels. The I²C bus and the ID EEPROM use 3P3VAUX.

6.2 Clock, trigger and control pins

The clock, trigger, SPI and other control signals use the following FMC pins:

Signal	FMC pin	FMC name	Direction	Function
FPGA_CLK_P0 / N0	H5 / H4	CLK0_M2C_N / P	Module → carrier	AD9518 OUT4 clock (**P/N swapped**)
EXT_TRIG_P / N	G2 / G3	CLK1_M2C_P / N	Module → carrier	Trigger, LVDS

Signal	FMC pin	FMC name	Direction	Function
CLK_FPGA	J13	HA11_N	Carrier → module	Optional PLL reference (REF1), VADJ ≥ 2.5 V only
FMC_CS_N	H34	LA30_P	Carrier → module	AD9518 chip select
FMC_RESET_N	H35	LA30_N	Carrier → module	AD9518 reset
FMC_PD_N	J12	HA11_P	Carrier → module	AD9518 power-down
FMC_SDO	K14	HA10_N	Module → carrier	AD9518 SPI data out
P_SCLK	G34	LA31_N	Carrier → module	SPI clock (ADCs and PLL)
P_SDI	G33	LA31_P	Carrier → module	SPI data (ADCs and PLL)
P_SDO	K13	HA10_P	Module → carrier	ADC SPI data out
P_CS0	H38	LA32_N	Carrier → module	ADC0 chip select
P_CS1	G37	LA33_N	Carrier → module	ADC1 chip select
P_CS2	H37	LA32_P	Carrier → module	ADC2 chip select
P_CS3	G36	LA33_P	Carrier → module	ADC3 chip select
LED0 … LED3	F13, F14, E12, E13	HA12_P, HA12_N, HA13_P, HA13_N	Carrier → module	User LEDs FMC_D1 … FMC_D4, active high
SCL / SDA	C30 / C31	SCL / SDA	Bidirectional	I²C: EEPROM and LTC2991
GA0 / GA1	C34 / D35	GA0 / GA1	Carrier → module	Geographic address of the EEPROM
PG_C2M	D1	PG_C2M	Carrier → module	Enables the on-board power supplies
TDI / TDO	D30 / D31	TDI / TDO	—	JTAG pass-through (looped on the module)

6.3 ADC data pinout

For each lane the table gives the pin on the Samtec ASP-134488-01 FMC connector (FMC_J1, row/column designator as printed on the connector and used in the VITA 57.1 pinout) and the FMC signal name on that pin, for both the ADC positive and negative output. Where **P/N swapped** is "yes", the ADC positive output lands on an FMC `_N` pin. The FPGA must invert that lane (or swap the polarity in the IOSERDES/IDELAY logic).

ADC0

Signal	Function	ADC+ Samtec pin	ADC+ FMC signal	ADC– Samtec pin	ADC– FMC signal	P/N swapped
DATA0	AIN1 lane A	G31	LA29_N	G30	LA29_P	**yes**
DATA1	AIN1 lane B	H32	LA28_N	H31	LA28_P	**yes**
DATA2	AIN2 lane A	H29	LA24_N	H28	LA24_P	**yes**
DATA3	AIN2 lane B	C27	LA27_N	C26	LA27_P	**yes**
DATA4	AIN3 lane A	D27	LA26_N	D26	LA26_P	**yes**
DATA5	AIN3 lane B	G25	LA22_N	G24	LA22_P	**yes**
DATA6	AIN4 lane A	H26	LA21_N	H25	LA21_P	**yes**
DATA7	AIN4 lane B	D24	LA23_N	D23	LA23_P	**yes**
DCO0	DCO (bit clock)	D20	LA17_P_CC	D21	LA17_N_CC	no
FR0	FR (frame)	G28	LA25_N	G27	LA25_P	**yes**

ADC1

Signal	Function	ADC+ Samtec pin	ADC+ FMC signal	ADC– Samtec pin	ADC– FMC signal	P/N swapped
DATA8	AIN1 lane A	H23	LA19_N	H22	LA19_P	**yes**
DATA9	AIN1 lane B	G22	LA20_N	G21	LA20_P	**yes**
DATA10	AIN2 lane A	H20	LA15_N	H19	LA15_P	**yes**
DATA11	AIN2 lane B	C23	LA18_N_CC	C22	LA18_P_CC	**yes**
DATA12	AIN3 lane A	C19	LA14_N	C18	LA14_P	**yes**
DATA13	AIN3 lane B	H17	LA11_N	H16	LA11_P	**yes**
DATA14	AIN4 lane A	D17	LA13_P	D18	LA13_N	no
DATA15	AIN4 lane B	G16	LA12_N	G15	LA12_P	**yes**
DCO1	DCO (bit clock)	D8	LA01_P_CC	D9	LA01_N_CC	no
FR1	FR (frame)	G19	LA16_N	G18	LA16_P	**yes**

ADC2

Signal	Function	ADC+ Samtec pin	ADC+ FMC signal	ADC– Samtec pin	ADC– FMC signal	P/N swapped
DATA16	AIN1 lane A	G13	LA08_N	G12	LA08_P	**yes**
DATA17	AIN1 lane B	G10	LA03_N	G9	LA03_P	**yes**
DATA18	AIN2 lane A	D15	LA09_N	D14	LA09_P	**yes**
DATA19	AIN2 lane B	H14	LA07_N	H13	LA07_P	**yes**
DATA20	AIN3 lane A	D12	LA05_N	D11	LA05_P	**yes**
DATA21	AIN3 lane B	H11	LA04_N	H10	LA04_P	**yes**
DATA22	AIN4 lane A	C11	LA06_N	C10	LA06_P	**yes**
DATA23	AIN4 lane B	H8	LA02_N	H7	LA02_P	**yes**
DCO2	DCO (bit clock)	G6	LA00_P_CC	G7	LA00_N_CC	no
FR2	FR (frame)	C15	LA10_N	C14	LA10_P	**yes**

ADC3 (HPC only)

Signal	Function	ADC+ Samtec pin	ADC+ FMC signal	ADC– Samtec pin	ADC– FMC signal	P/N swapped
DATA24	AIN1 lane A	K11	HA06_N	K10	HA06_P	**yes**
DATA25	AIN1 lane B	E7	HA05_N	E6	HA05_P	**yes**
DATA26	AIN2 lane A	J10	HA07_N	J9	HA07_P	**yes**
DATA27	AIN2 lane B	F11	HA08_N	F10	HA08_P	**yes**
DATA28	AIN3 lane A	K8	HA02_N	K7	HA02_P	**yes**
DATA29	AIN3 lane B	J7	HA03_N	J6	HA03_P	**yes**
DATA30	AIN4 lane A	E10	HA09_N	E9	HA09_P	**yes**
DATA31	AIN4 lane B	F8	HA04_N	F7	HA04_P	**yes**
DCO3	DCO (bit clock)	F4	HA00_P_CC	F5	HA00_N_CC	no
FR3	FR (frame)	E3	HA01_N_CC	E2	HA01_P_CC	**yes**

AIN1…AIN4 correspond to the channels listed for each ADC in 5.1. For example, ADC1 AIN1 is channel A4. All DCO clocks are on clock-capable (`_CC`) pairs.

6.4 I²C devices

Two devices are connected to the FMC I²C bus:

Device	Function	7-bit address
FMC_U1 M24C02	FMC ID EEPROM (FRU data)	0x50 with GA1 = GA0 = 0
U5 LTC2991	Voltage monitor (2.5)	0x48

The EEPROM holds the VITA 57.1 FRU record. Its MultiRecord area contains the DC load records (VADJ and the other supply requirements), which lets the carrier set VADJ automatically. The EEPROM address pins are wired E0 = GA1 and E1 = GA0. Carriers using non-zero geographic addresses should take this into account when locating the EEPROM.

6.5 User LEDs

LED0–LED3 drive the four user LEDs FMC_D1–FMC_D4 through MOSFET switches. A logic high (VADJ level) on an LED pin turns its LED on. The LEDs are free for application status or debugging.

6.6 LPC carriers

The ADC0–ADC2 data, the SPI write path, the PLL chip select and reset, and the clock and trigger pins all use LA and CLK pins, which exist on LPC connectors. The following functions use HA pins and are **not available on an LPC carrier**:

Function lost on LPC	Consequence
ADC3 data (channels B4–B7)	Module operates as a 12-channel digitizer
P_SDO, FMC_SDO	No SPI read-back from the ADCs or the PLL. Configuration is write-only and PLL lock cannot be read over SPI.
FMC_PD_N	PLL stays powered (pulled up on the module)
CLK_FPGA	FPGA reference for the PLL unavailable. Use the on-board oscillator or the external clock.
LED0–LED3	User LEDs stay off

7 Reference documents

The following documents give further details on the module and its components:

Document	Content
SMT-FMC116 Product Specification (QCF51) – Home Page	Specification, mechanical data, full FMC pinout
Analog Devices LTC2172/LTC2173/LTC2174/LTC2175 datasheet	ADC registers, serial data format, test patterns, timing
Analog Devices AD9518-0 datasheet	PLL and clock distribution registers, input/output specifications
Analog Devices ADA4938-2 datasheet	Front-end amplifier
AD9516/AD9517/AD9518 evaluation software	PLL configuration and `.stp` setup files
ANSI/VITA 57.1 (Samtec page)	FMC standard

8 Board support package (BSP)

The SMT-FMC116 board support package provides an FPGA reference design and a processor application for configuring the module, receiving ADC samples and checking the digital interface. It is a starting point for integrating the module into a carrier-based acquisition system. Sources are supplied via a GitHub repository covering the ZCU102 and ZCU104 evaluation boards and a Trenz TE0813-based carrier system, including a full 16-channel HPC design. The project variants share the same general receiver and control architecture.

8.1 Organization and example designs

The BSP separates the programmable logic (PL), which receives and aligns the high-speed ADC data, from the processing system (PS), which controls configuration and initialization.

Each project variant contains FPGA sources and processor software. Paths below are relative to the selected project directory.

Project area	Contents
`pl/hdl`	VHDL modules for ADC reception, alignment, calibration, SPI control and system integration
`pl/ip`	Carrier-specific clock and Integrated Logic Analyzer (ILA) IP configurations
`pl/xdc`	Common and carrier-specific pin and timing constraints
`pl/zcu102`, `pl/zcu104`, `pl/te0813` (depending on variant)	Carrier-specific Vivado projects, recreation scripts and debug probe setup
`ps`	C application and platform support for the processor side

The repository provides project variants for different channel counts and carrier systems:

Project	Carrier example	ADC coverage	Analog channels
`FMC116_ADC_0_1_2`	ZCU102, ZCU104, Trenz TE0813-based system	ADC0-ADC2	12: A0-A7 and B0-B3
`FMC116_ADC_0_1_2_3`	Trenz TE0813-based system, full HPC	ADC0-ADC3	16: A0-A7 and B0-B7

The Trenz full-HPC project is supplied under `FMC116_ADC_0_1_2_3/pl/te0813`, with its top level in `pl/hdl/top.vhd`, carrier constraints in `pl/xdc/TE0813.xdc` and processor application in `ps/src`. It receives all 32 ADC data pairs, four DCO pairs and four frame pairs. ADC3 uses the FMC HA bank, so all 16 channels require the HPC connections described in section 6.

The supplied projects target Vivado 2024.1; the repository README also describes the processor workflow using Vitis Classic 2024.1. Use the hardware project, constraints and software from the same project variant.

8.2 ADC reception and alignment

The receiver uses the ADC's DCO clock to capture the serial LVDS data and the FR signal to establish sample-word boundaries. It implements the two-lane, 16-bit serialization described in 5.3. The resulting parallel channel words can be connected to application-specific processing, buffering or data transfer logic.

Module	Role
top.vhd, top_zcu102.vhd, top_te0813.vhd (depending on project)	Connect the processor system, register interface, ADC receivers, SPI controller, calibration logic and trigger input
adc.vhd	Groups the data lanes, frame signal and clock handling for one quad ADC, and assembles the channel words
adc_bit.vhd	Captures and deserializes an individual serial input, with adjustable input delay and calibration support
ibufds_swap.vhd	Receives differential signals and supports compensation for routed P/N polarity swaps
bitslip16.vhd	Adjusts the position of the received bits to align sample words
autocalibration.vhd	Sequences receiver calibration using ADC test patterns, clock-phase adjustment, input delays and word alignment

The full-HPC Trenz variant extends this architecture to a fourth receiver and includes ADC3 in the delay adjustment, word alignment and automatic calibration controls. Its carrier-specific polarity settings account for the differential routing in that system.

Receiver calibration establishes a suitable sampling point and word alignment for the digital link. It is separate from analog gain or offset calibration. The design exposes calibration status and includes debug signals for inspecting the alignment process.

8.3 Configuration and control

The processor accesses the FPGA through the register bank in `registers.vhd`. These registers provide control and status for resets, ADC and PLL configuration, SPI transfers and receiver calibration. The SPI transmitter in `spit_tx.vhd` sends configuration words over the module's shared SPI bus.

The example C application, `fmc116.c`, contains PLL register tables for internal-reference and external-clock operation, along with functions for sending PLL and ADC configuration words. It demonstrates reset, clock configuration, ADC test-pattern setup and starting receiver calibration. Compile-time selections determine the clock source and whether the application stays in a test-pattern routine or proceeds to automatic calibration.

The full-HPC Trenz application in `FMC116_ADC_0_1_2_3/ps/src/fmc116.c` has `ADC_TEST` disabled and `PLL_INTERNAL` enabled, so its startup sequence proceeds to automatic receiver calibration using the internal-reference configuration. Select the required clock and test mode when adapting the example.

8.4 Trigger, debugging and integration

The top-level design receives the external LVDS trigger, synchronizes it into the ADC data clock domain and makes it available to the debug logic. ILA cores allow ADC samples, trigger activity, SPI transactions and calibration signals to be inspected in the FPGA.

For a new application, use the supplied carrier project as a reference, adapt the pin and timing constraints to the target hardware, select the required PLL and ADC settings, and verify receiver alignment with test patterns. Then connect the parallel ADC words and synchronized trigger to the application's acquisition logic. The supplied example focuses on configuration and interface verification; sample storage,

host transfer and application-specific trigger handling can be added around the receiver modules.

8.5 Using the Trenz full-HPC example

For all 16 channels, start with the `FMC116_ADC_0_1_2_3` TE0813 project. The general workflow is to build the FPGA bitstream in Vivado, export the hardware definition (XSA), create a matching processor platform and application in Vitis Classic, and build and run the supplied C sources. The repository README provides the detailed tool steps.

The full-HPC design exposes the additional ADC3 channel words alongside the other ADC data. Its ILA probes provide visibility into the receiver data and calibration signals; the project-specific `pl/te0813/probes.tcl` supports inspection in Vivado Hardware Manager. This makes the Trenz example a reference for checking the complete 16-channel interface before adding application-specific acquisition and data-transfer logic.

8.6 Sundance GitHub

The sources are located here:
[SundanceMultiprocessorTechnology/SMT_FMC116: The FMC116 is a sixteen-channel ADC FMC Daughter Card which is fully compliant with the VITA 57.1-2008 standard]

Request access from your local supplier or from Sales@Sundance.com

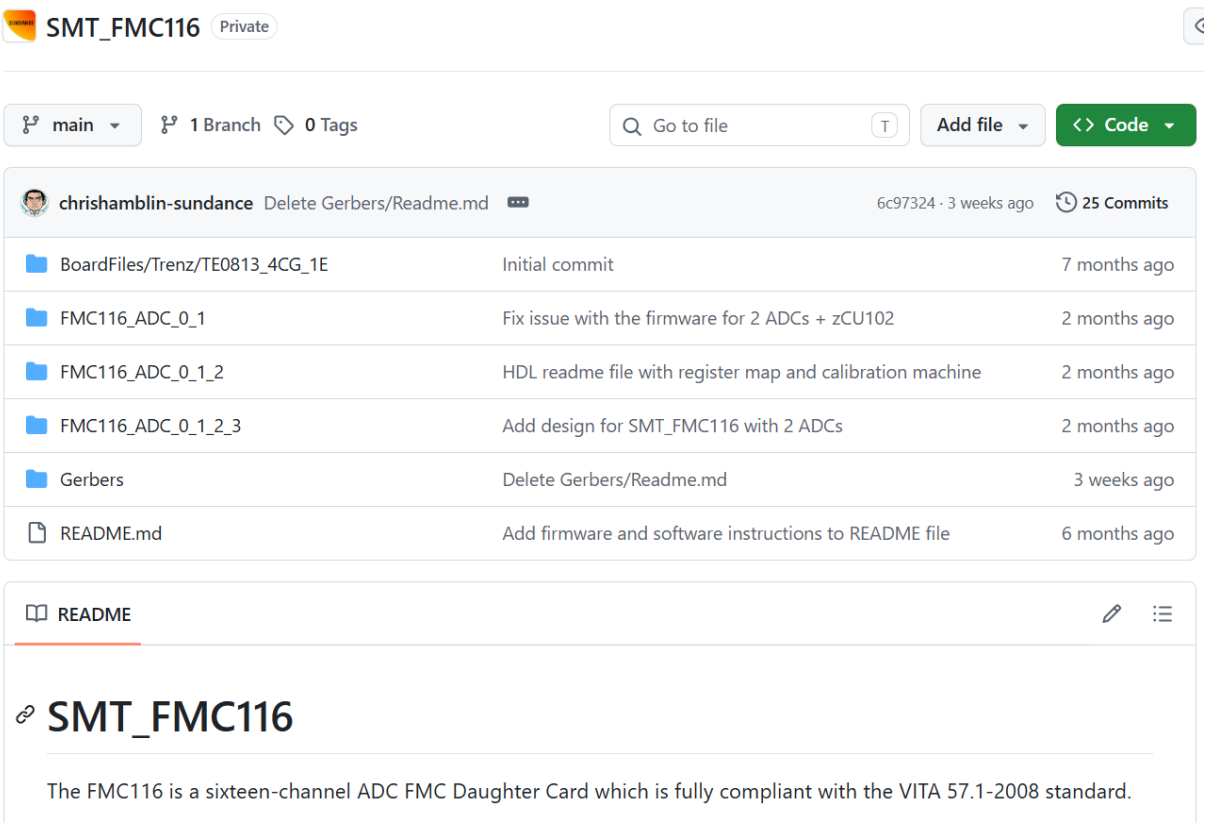


Figure 8 - Sundance GitHub for SMT-FMC116