PCIe104N

Polarfire PCIe104 Card

User Guide

REVISION HISTORY

Revision	Comments	Originator	Date
0.1	Initial Draft	RC	Dec. 1st, 2023
0.2	Fixed RGB User LED pinout	RC	Dec. 20th, 2023
0.3	Added real images of the board	NN	Feb. 6th 2025
0.4	Fixed references to eNVM	RC	Feb. 26th 2025

Sundance Digital Signal Processing Inc.
4790 Caughlin Parkway 233, Reno, NV 89519-0907, U.S.A.
Tel: +1-775-827-3103, Fax: +1-775-827-3664, email: sales@sundancedsp.com
www.sundancedsp.com

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1 INTRODUCTION

This document details the features and usage of the PCIe104N. This is a PCIe104 form factor board featuring a Polarfire FPGA (MPF500T-1FCG1152I). The board has a mezzanine connector that features 3.3 and 5V tolerant I/Os suitable for custom daughter cards. Additionally, the PCIe104N has a ruggedized connector for accessing 4 transceivers, a Samtec ASP-129637-03 which provides a stack down connection to a PCIe104 host with 4 lanes of PCIe at Gen2 speeds, and clocking options including an onboard clock generator. The PCIe104N has pushbuttons for resets and LEDS for user applications and power good indication. A MPF300 device can be installed with reduced functionality, see chapter 1.2.

1.1 Hardware features of carrier board

The hardware has the following features:

1. Main FPGA MPF500T-1FCG1152I PolarFire FPGA from Microchip
2. Option to assemble with an MPF300T-1FCG1152I device.
3. PCIe104N is in PCIe104 format with 4 lanes of PCIe interface to the host.
4. PCIe104N is designed to be connected to a stack down host.
5. On the other side of the card from the stack down connector it must be able to fit to a mezzanine card.
6. 104 IO signals are routed to the mezzanine connector (ASP-129637-02) with:
   - 63 5V IOs routed through level translators *see **Error! Reference source not found.**.
   - 20 LVDS differential pairs (41 I/O total); capable to be single ended LVCMOS33, (option to be as LVCMOS25);
7. Samtec QTE-014-01-F-D-DP-TR connector for accessing 4 additional transceivers, 1 pair of GPIO, clock capable, and reference clocks.
8. PCIe104N only boots from the internal NVM FLASH.
9. The contents of the external SPI FLASH and the internal NVM FLASH cannot be modified from the host PCIe interface. The flash content can be modified through JTAG,
10. The board features three tactile buttons, two for the user, and one reset button.
11. Four power good LEDs, Two User RGB Leds.
12. The module uses industrial grade components.
13. Two industrial grade DDR4 chips for RAM organized as 32-bit bus.
14. External SPI Flash for user data storage only.
15. Input power 5V, 3A max. 12V – for fan only and can be unused if no fan.

1.2 Board limitations and notes

The user must check the power consumptions of their FPGA designs.
Please use the Libero SmartPower analysis tool from Microchip to make the power estimation.

1. Board uses 74LVC1T45GM controllable direction level translators. User must first set Direction control signal, only after that turn on supply for that translators.

2. NOTE! PolarFire FPGAs do not support LVDS18, true LVDS outputs and inputs are available only for LVDS25. For more information about FPGA I/Os see **user guide [**2**]**

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1.3 PCIe104N Carrier Block Diagram

The following diagram shows the major blocks of PCIe104N:

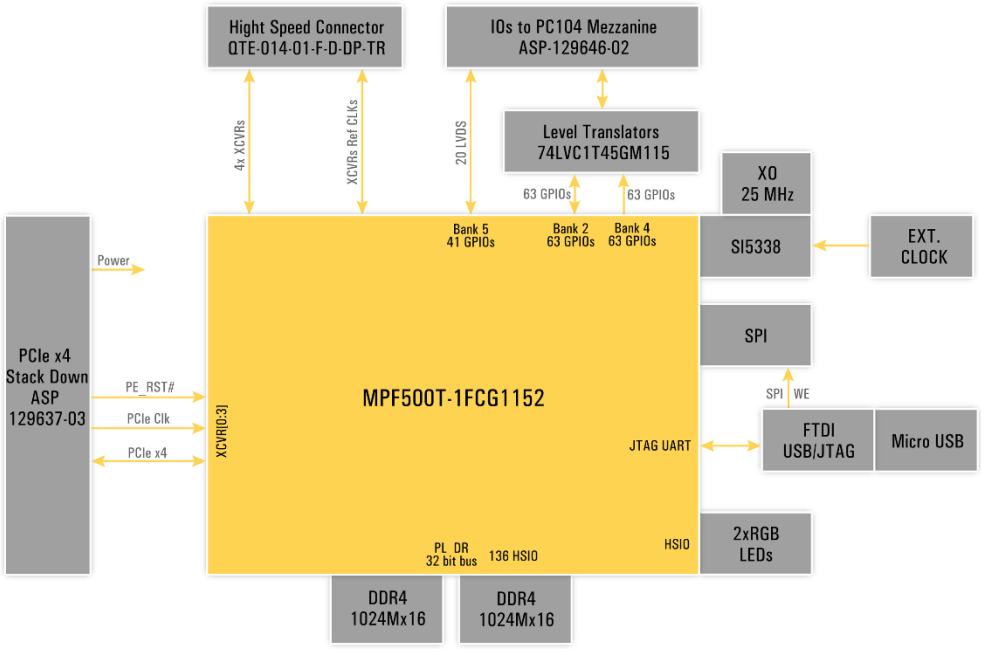

Figure 1: PCIe104N Block Diagram

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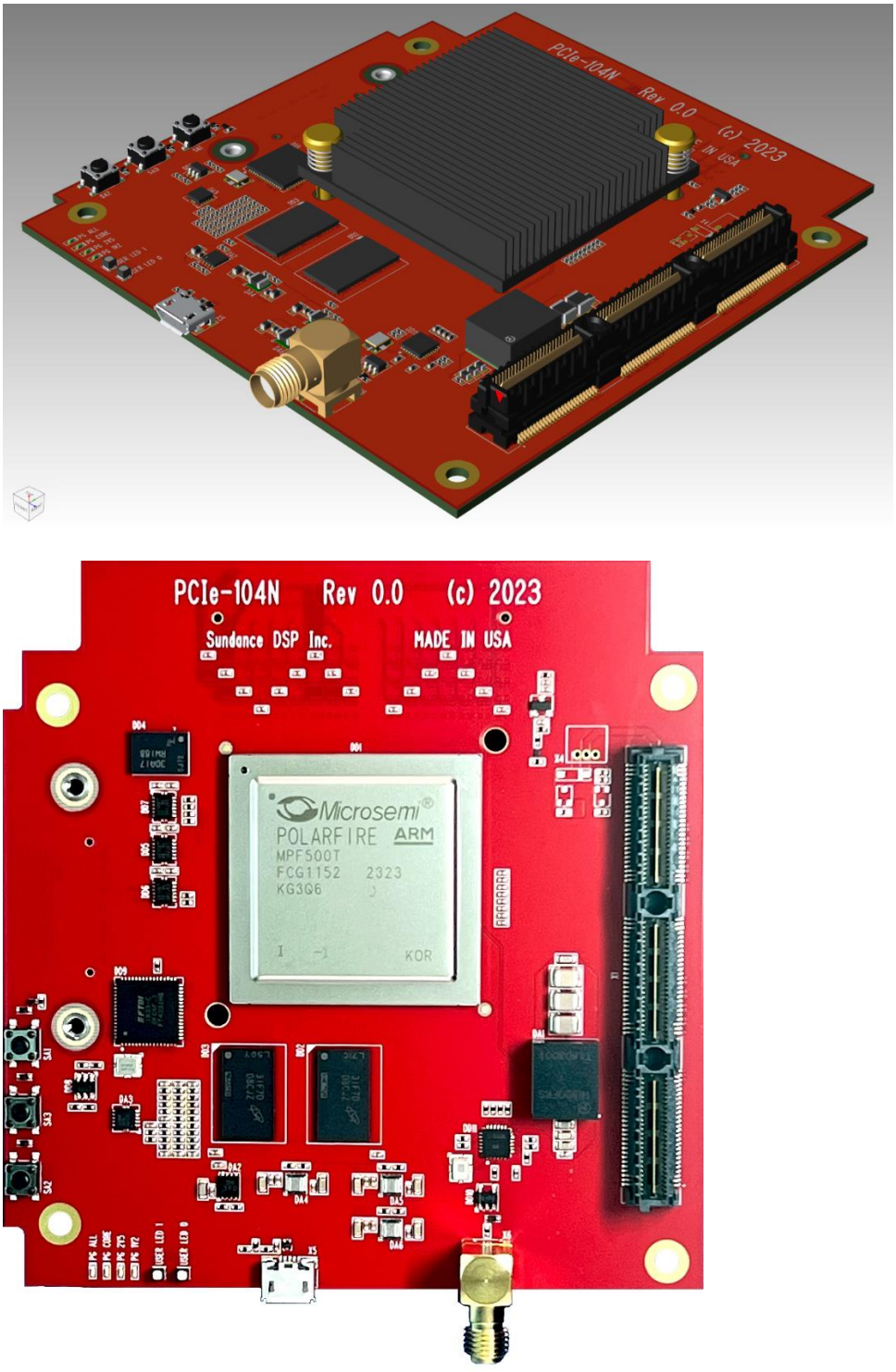

Figure 2: PCIe104N 3D view

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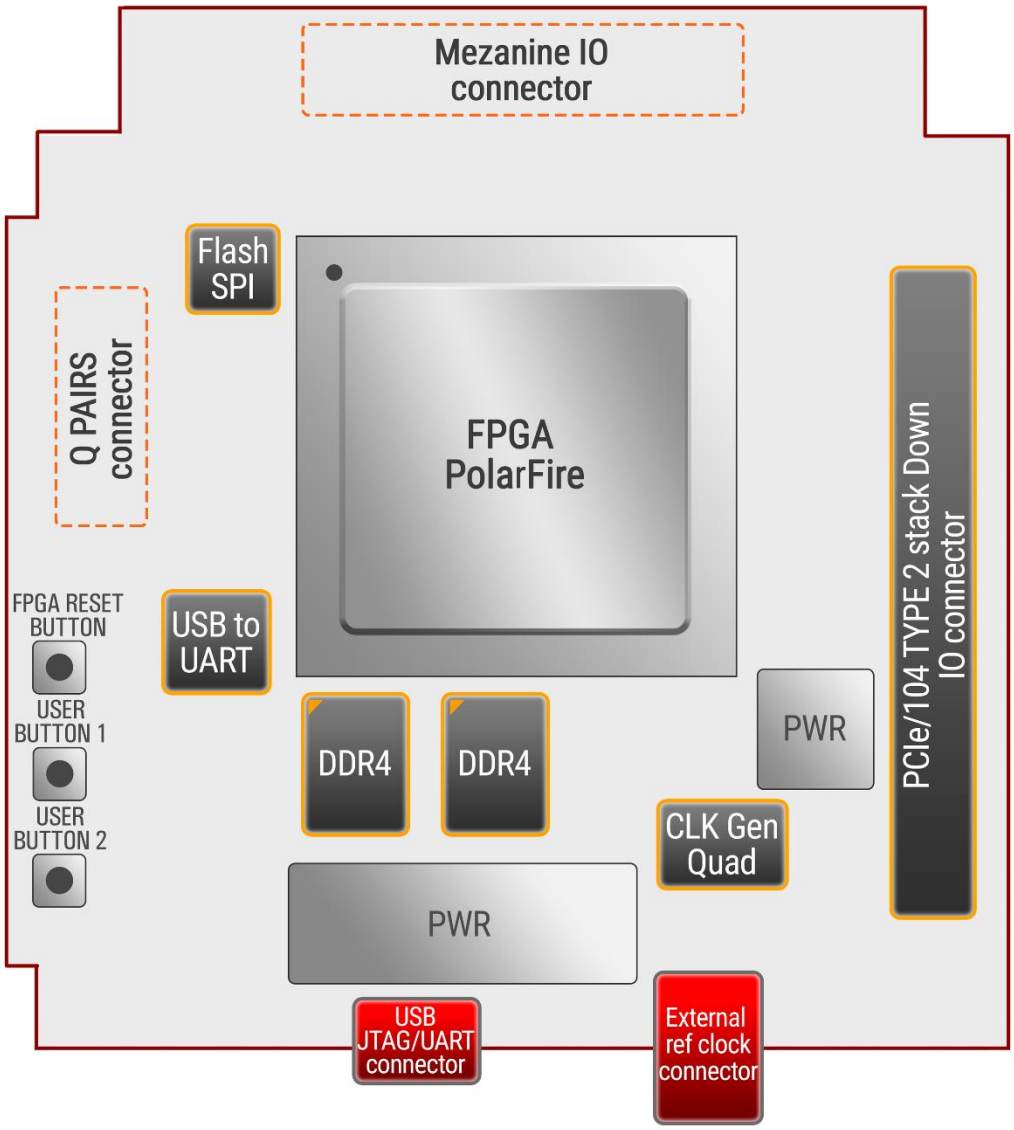

Figure 3: Component side view

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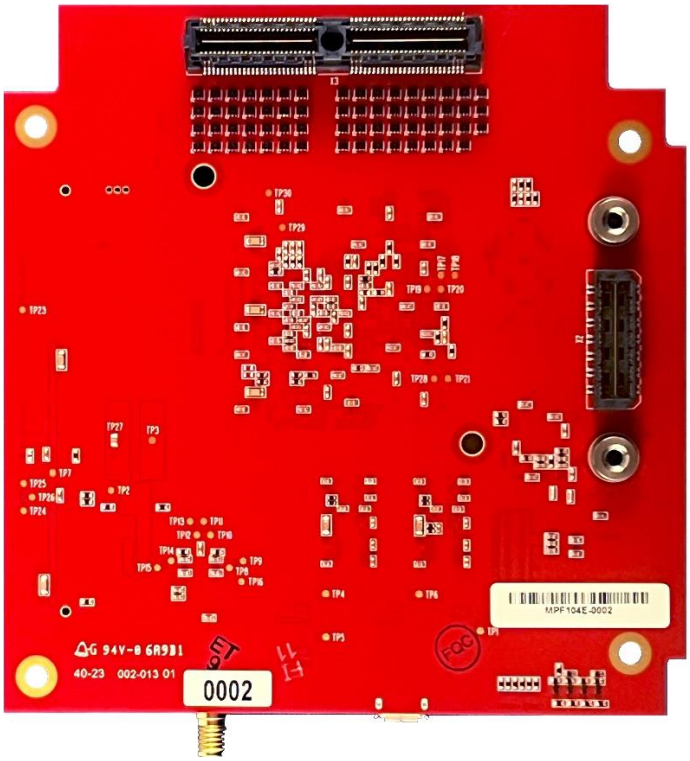

Figure 4: Solder side view

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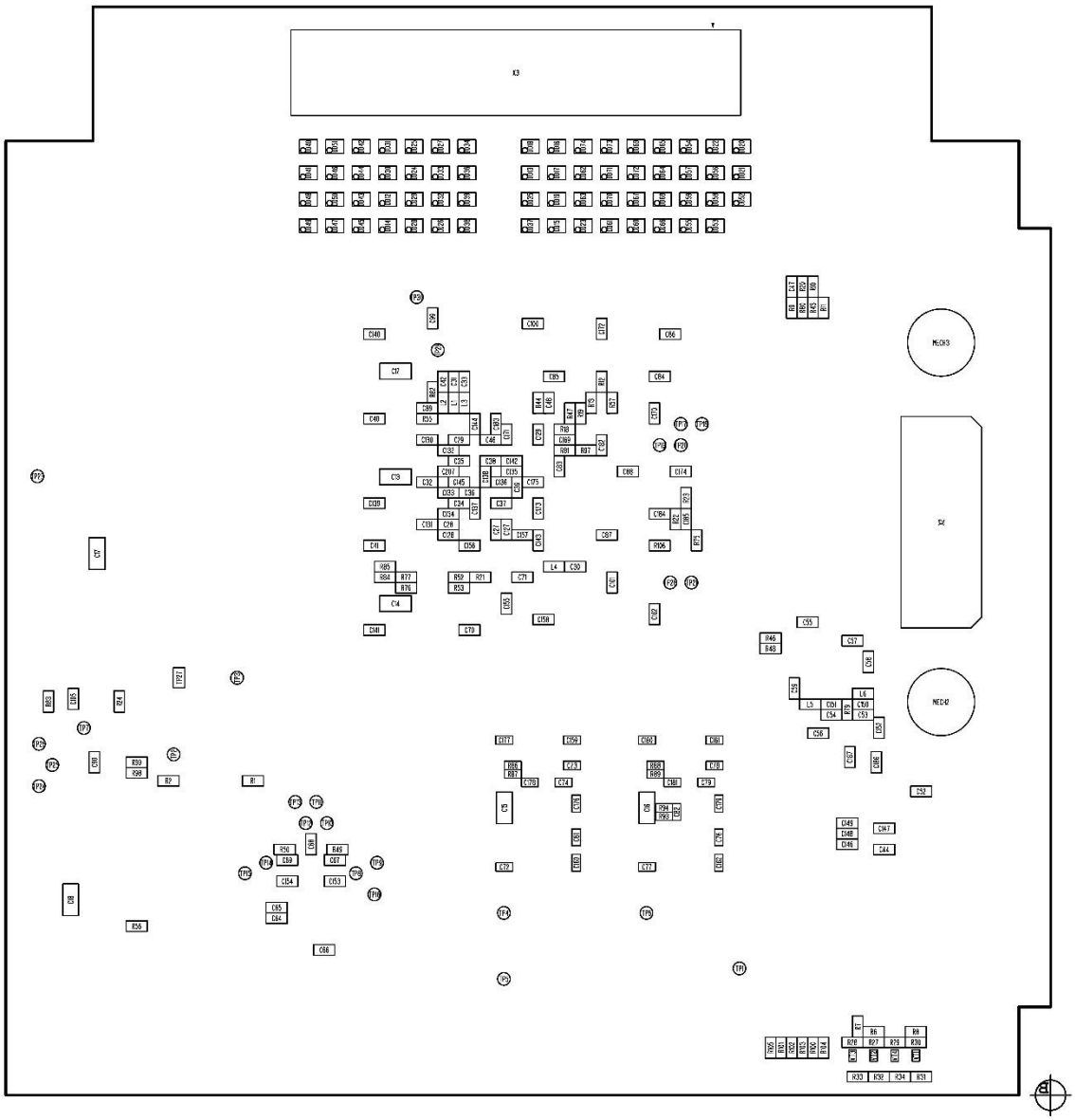

Figure 4: Solder side view

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1.4 Dimensions

The board dimension is a standard PCIe104 form factor.
Weight: 78 grams

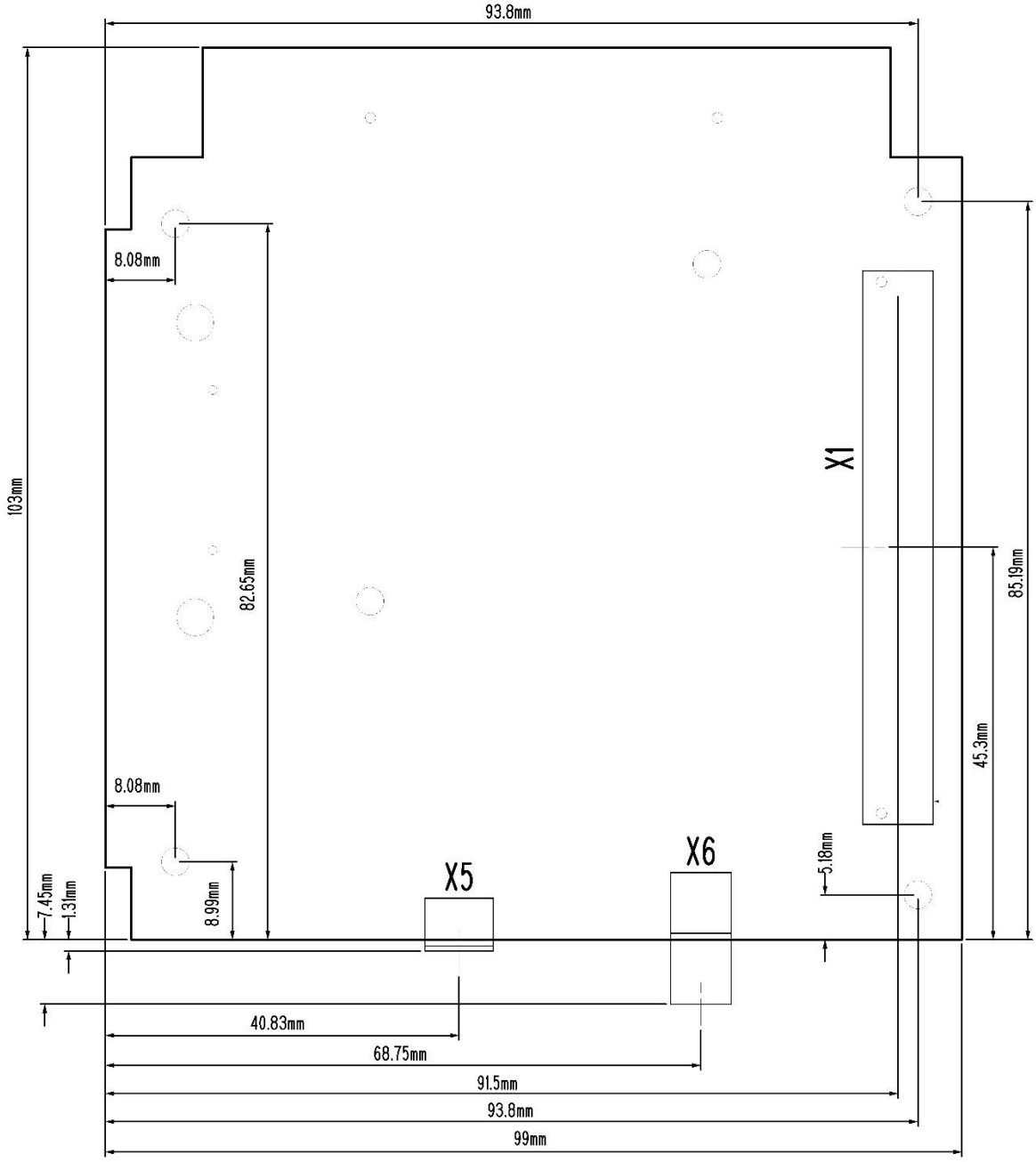

Figure 5 : Board Dimensions

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1.5 Environmental

- Operating junction temperature (Tj)
  - Extended Commercial: 0˚C to 70˚C

  Notes:

  1. A thermal solution must be designed to ensure that the board does not exceed the thermal maximum (Tj) during operation.

  2. Device functionality is not guaranteed if the board exceeds the thermal maximum (Tj) during operation.
- Storage temperature: -65˚C to +150˚C
- Humidity: 10% to 90% non-condensing

1.6 Operating Voltage

The PCIe104N has 1 power input interface.

- +5V and +12V from PCIe104 power blades.

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2 PCIE104N INTERFACES

2.1 PCIe104 Interface

The PCIe interface used is PCIe x4 gen2 EP. Provided via a PCIe104 stack down connector. The connector is the Samtec ASP-129637-03, this is the standard PCIe104 TOP connector. Voltage from the 5V blade is passed through the connector for powering the board. A 100MHz PCIe reference clock will be routed to the FPGA. The board connector is shown in the image below.

Note: See appendix section 4.3 for a detailed pinout

Table 1: PCIe connection

Signal name	FPGA pin name	Direction relative to module, Description
PCIe_TX, RX	XCVR 0	The lanes polarity and order automatically detected by IP core
PCIe_CLK	XCVR0_A_REFCLK	PCIe clock input to FPGA
PCIe_RST#	GP230PB4	PCIe reset signal input to FPGA

2.2 FPGA

The PCIe104N is populated with MPF500T-1FCG1152I device which has 480K logic cells, 24 high speed transceivers, two PCIe hard blocks and 584 IO's (324 HSIO's, 260 GPIO's)

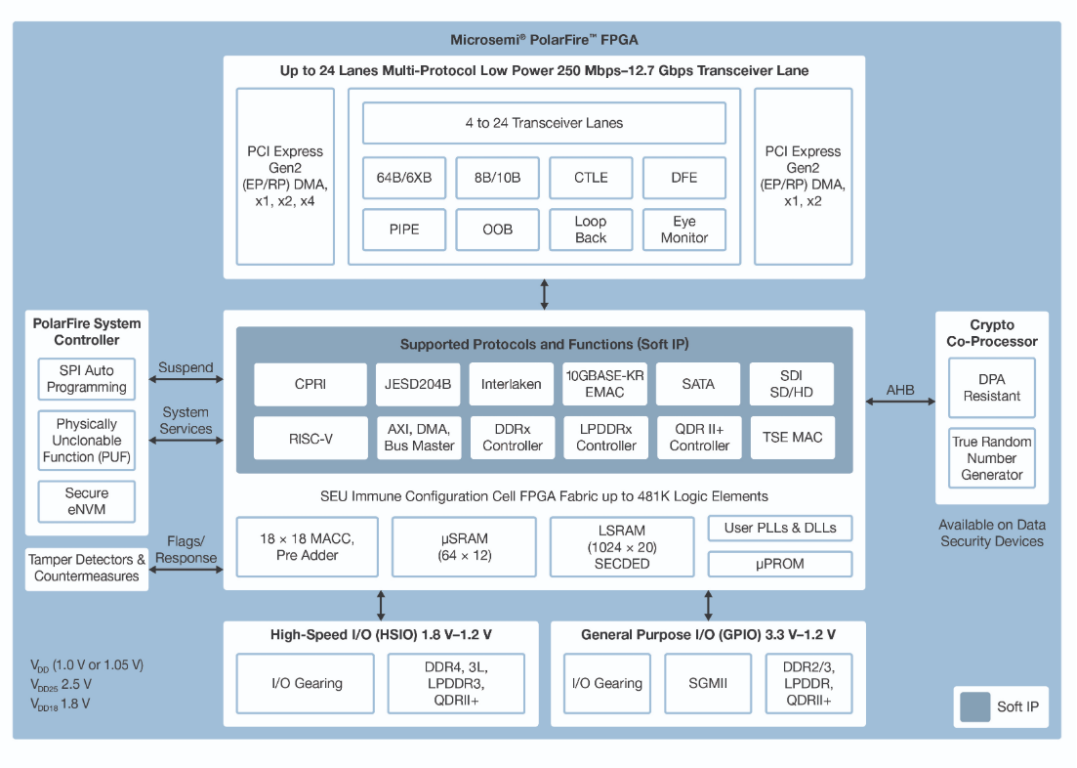

Figure 6: Microsemi Polar Fire Block Diagram

More information on the MPF devices can be found in the link below:

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https://www.microsemi.com/product-directory/fpgas/3854-polarfire-fpgas#overview

Note: The PCIe104N can alternatively be populated with MPF300T device, but this device only comes with 16 transceivers and 512 IO's (276 HSIO's, 236 GPIO's).

The FPGA can be configured from:

a. JTAG interface
b. From FPGA internal flash

For I/Os available to the FPGA:

1. 136 HSIO are utilized for the DDR4 memory.
2. The SPI interface built into the FPGA is used to control the SPI flash.
3. A few clock capable I/O pins are used for clocking.
4. 63 signals are 5V GPIOs routed to the mezzanine by using bidirectional level translators
5. 63 signals are routed to the enable the level translators
6. 41 signals are routed to the mezzanine connector as differential pairs which provide 20 LVDS signals
7. 4 transceivers routed from QUAD0 to the PCIe104 connector
8. 4 transceivers routed to the ruggedized Samtec connector

2.3 USB - JTAG - UART interface

The PCIe104N has a JTAG, UART, SPI via micro-USB connector and FT4232HQ IC.
The following table describes pinouts of FTDI. Libero software can access to JTAG and UART, SPI is not accessible directly from libero.

To access SPI interface user need custom SW;
SPI flash is write protected by default, to write you need custom SW.
During programming SPI, FPGA must be hold in reset, via FTDI

Table 2: FTDI IC connections.

FTDI IC pin name	FPGA pin name	Connection Description
UART		
CDBUS0	GP199NB4	Uart RXD, input to FPGA
CDBUS1	GP199PB4	Uart TXD, output from FPGA
JTAG		
ADBUS0	JTAG_TCK	Standard connection in Libero SW
ADBUS1	JTAG_TDI	
ADBUS2	JTAG_TDO	
ADBUS3	JTAG_TMS	
ADBUS4	JTAG_TRST#	
SPI and reset		
BDBUS0	SCK	SPI flash CLK pin
BDBUS1	SDO	SPI flash DIN(DQ0) pin

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FTDI IC pin name	FPGA pin name	Connection Description
BDBUS2	SDI	SPI flash DOUT (DQ1) pin
BDBUS3	SS	SPI flash CS# pin
BDBUS4	NC	SPI flash W# pin, set “1” – to write into SPI, “0” – default, write prohibited..
BDBUS5	SPI_EN	Enable FTDI SPI interface, and disable FPGA SPI pins. “1” – default, FTDI SPI isolated from flash and FPGA. “0” – Set to acces to SPI flash via FTDI.
BDBUS6	DEVRST_N (via invertor)	FPGA reset signal. “0” - default, normal operation. “1” – FPGA reset

2.4 PCIe104N Clocking Resources

There are 3 clock sources:

1) Clock provided by the PCIe through the connector.
2) A Silicon Labs SI clock chip (reference clock to the chip is provided by a 25 MHz crystal oscillator, the clock chip provides clocks for the FPGA, XCVRS, and DDR4).
3) External reference clock via SMA connector

The board has one multi-channel low jitter clock generation chip from Silabs. This IC can use a crystal 25MHz or external clock via SMA connector, as reference. Reference clock selection is made via registers or via software.

By default, the FPGA has internal access to the I2C interface of the Clock IC and the default address is 0x70.

The Si5338 is programmed by SDSP to ensure proper operation, and some frequencies must not be reprogrammed by the user.
The external user clock must be LVCMOS33 standard.
User reference frequency range: 5 – 200 MHz.

Table 3: Clock IC connections.

IC pin name	Connected to, comment	Freq, MHz	Pull Ups/ Pull Downs	Output/Input standard
Control GPIOs				
SDA	GP231NB4	0.4	1k to 3.3V	LVCMOS33
SCL	GP232PB4			
INTR#	GP230NB4			
Frequency inputs				
XA, XB	25MHz ±30 ppm crystal	25	N/A	
CLKIN	User reference	5-200	N/A	SE, DC coupled
Frequency outputs				
OUT0	GPI204B4/CLKIN_W_6	50	N/A	LVDS 3.3V
OUT1	XCVR_4A_REFCLK, XCVR_2B_REFCLK(Only for MPF300)	156.25		
OUT2	XCVR_2C_REFCLK	156.25		

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IC pin name	Connected to, comment	Freq, MHz	Pull Ups/ Pull Downs	Output/Input standard
OUT3	X2, 26 (for +), 28 (for -)	100	N/A	LVDS 3.3V

2.5 Mezzanine Connector

To be backward compatible, for the mezzanine connector, the Samtec ASP-129637-02 is used on the PCIe104N and the mating ASP-129646-02 on the mezzanine card. These are essentially the same connectors used for PCIe interfaces but with 2 banks.

There are a total of 104 IO signals routed to the mezzanine connector, of which 63 signals are 5V capable GPIOs using bidirectional level translators.The remaining 41 signals are routed as differential pairs which provide 20 LVDS signals. They can also operate as single-ended at a 3.3V level (or 2.5V after rework).

The bidirectional level translator that is used is the **74LVC1T45GM**.

By default, output 5V signals are powered off and the leakage at those IOs is max 1uA. User must first set DIR signal (to define desired direction of GPIO) then turn on the power to the translators.

When the Sundance DSP FC205 IP core is utilized then some of the IO signals can be used for RS232 and RS485.

Please see appendix section 4.1 Mezzanine Connector for the pinout and FPGA pin assignments.

Note: The level translator direction (GPXXX_B2X_DIR) must be set before the level translator power is enabled (EN_VCCB)

2.6 DDR4 Interface

The FPGA fabric is connected to 2 x 16Gb (total of 4GByte) of DDR4 memory as components from Micron **MT40A1G16TB-062EIT**, which provides a 32-bit wide interface. The interface is connected to the **NORTH_NE_OPT** anchor of the device; please use this option when adding constraints to the FW.

2.7 Transceiver Connector

On the PCIe104N there is an additional AUX connector with 4 transceivers and clock for development purposes. The part number of the Connector on the board is QTE-014-01-F-D-DP-A-TR. The connector can handle speeds of up to 17Gbps. For the connector pinout, please see appendix section 4.2.

All the lanes are DC coupled. AC coupling, if required, must be performed by the user.

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2.8 SPI Flash

The board has 1024Mb of platform serial flash memory from Micron (**MT25QU01GBBB8E12-0SIT**). The external flash can be used for user data storage. If the user does not require external data storage, the flash does not need to be populated.

The Polarfire FPGA also features internal flash, which is the primary storage location for the bitstream as it allows for instantaneous boot time. The Microchip tools also have the ability to encrypt the bitstream on the device and to put the device in a mode where it can no longer be programmed.

NOTE: By default the SPI flash is write-protected, to be able to write data, the user needs to create custom SW for the FTDI chip. Both a host-side application and program for handling the FTDI BDBUS GPIO programmed into the EEPROM would be required. There is also a resistor which can be populated which also allows for the flash to be wriiten to. Contact Sundance support for more information.

2.9 Fans/Cooling

By default, the fan circuit is not installed on the PCIe104N. If the user requires a fan, it must be chosen as an option. Contact SDSP support to add this option. The board uses a 12V 3 pin fan.

Table 4: FAN signal pinout and usage

FAN signal	FPGA pin name	Description
FAN_PWM	GP229PB4	PWM control
FAN_TACH#	GP231PB4	Inverted FAN tachometer input to FPGA

1 – Tacho signal from the fan, yellow wire
2 – 12V, red wire
3 – Ground, black wire

2.10 Reset buttons

The PCIe104N has 3 tactile buttons, one for resetting the entire FPGA, and 2 others for user applications.

Table 5: Button pinout

Reference	FPGA pin name	Direction relative to module, Description
SA1	DEVRST_N	Reset button
SA2	GP228PB4	User button 1, Active low
SA3	GP228PN4	User button 2, Active low

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2.11 Reset sources

There are 2 reset sources for each the board:

1. Reset from button SA1
2. Reset from FTDI IC(USB-JTAG interface)

Each reset source operates independently.

2.12 User and power good LEDS

There are 6 LEDs placed on the PCIe104N. Two RGB LEDs are connected to the FPGA for user applications, and four are power good indicators. The following table describes the functions of the LEDs.

Table 6: LED pinout and usage

Reference	FPGA pin name	Direction relative to module, Description
VD1		Power good indicator, All power supplies, are within range
VD2		2.5V rail power good indicator
VD3		1.2V rail power good indicator
VD4		FPGA core rail power good indicator
VD10	GP202NB4	RGB LED RED, Active low
	GP202PB4	RGB LED GREEN, Active low
	GP201NB4	RGB LED BLUE, Active low
VD11	GP200PB4	RGB LED RED, Active low
	GP200NB4	RGB LED GREEN, Active low
	GP201PB4	RGB LED BLUE, Active low

2.13 Power

The board requires only one voltage to operate: 5V. It will draw 12V from the PCIe104 connector if used with FAN (3.3V is not used and is generated by a DC-DC converter on the board). The other required voltages are generated on-board from the 5V rail. The power usage of the PCIe104N depends strongly on the design implemented in the FPGA and peripheral interfaces and is not specified in this document. The maximum power consumption of the module is approximatly 15 watts.

3 REFERENCES

1. **PolarFire power estimator spread sheet.**
2. **Microsemi_PolarFire_FPGA_User_IO_User_Guide_UG0686.**
3. **Microsemi_PolarFire_FPGA_Datasheet_DS0141.**
4. **Microsemi_PolarFire_FPGA_Errata.**

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4 APPENDIX/ PINOUTS

4.1 Mezzanine Connector (X3) Pinout

Note: To enable the level translators, the EN_VCCB signal must be applied from the FPGA. The FPGA enable pin is GP229NB4.

4.1.1 Even Pins

In the table below column DIR contains position of DIR signal on FPGA. To set GPIO as output from board DIR must be set to logic “1”. If GPIO must be input to FPGA, DIR must be set to logic “0”.

Logic Level/ Standard of 5V tolerant I/O: **5VDC TTL I/O Tristateable**

Note: If a Pin is 5V tolerant, an additional FPGA pin is used to enable the level translator

Table 7: Mezzanine Connector Even side pinouts

Mezzanine Pin Number	FPGA Pin	5V Tolerant	FPGA DIR Pin
J3.2	GP306PB2	YES	GP227PB4
J3.4	GP11PB2	YES	GP227NB4
J3.6	GP305NB2	YES	GP234NB4
J3.8	GP307NB2	YES	GP233PB4
J3.10	GP306NB2	YES	GP235NB4
J3.12	GP305PB2	YES	GP233NB4
J3.14	GP311PB2	YES	GP254NB4
J3.16	GP312PB2	YES	GP254PB4
J3.18	GP310PB2	YES	GP252NB4
J3.20	GP310NB2	YES	GP252PB4
J3.22	GP308PB2	YES	GP253PB4
J3.24	GP311NB2	YES	GP253NB4
J3.26	GP314PB2	YES	GP250NB4
J3.28	GP312NB2	YES	GP250PB4
J3.30	GP308NB2	YES	GP255PB4
J3.32	GP313PB2	YES	GP251PB4
J3.34	GP313NB2	YES	GP255NB4
J3.36	GP314NB2	YES	GP251NB4
J3.38	GP309PB2	YES	GP259NB4
J3.40	GP315PB2	YES	GP257PB4
J3.42	GP08NB2	YES	GP256PB4
J3.44	GP08PB2	YES	GP256NB4
J3.46	GP28NB2	YES	GP237NB4
J3.48	GP25NB2	YES	GP235PB4
J3.50	GP06NB2	YES	GP261NB4
J3.52	GP09PB2	YES	GP234PB4
J3.54	GP29PB2	YES	GP237PB4
J3.56	GP29NB2	YES	GP258PB4
J3.58	GP28PB2	YES	GP258NB4
J3.60	GP25PB2	YES	GP261PB4

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J3.62	GP27PB2	YES	GP247PB4
J3.64	GP24PB2	YES	GP248PB4
J3.66	GP24NB2	YES	GP247NB4
J3.68	GP27NB2	YES	GP248NB4
J3.70	GP20PB2	YES	GP249NB4
J3.72	GP20NB2	YES	GP249PB4
J3.74	GP26PB2	YES	GP245NB4
J3.76	GP26NB2	YES	GP245PB4
J3.78	GP07PB2	YES	GP244NB4
J3.80	GP06PB2	YES	GP236NB4
J3.82	GP21PB2	YES	GP244PB4
J3.84	GP21NB2	YES	GP236PB4
J3.86	GP32NB2	YES	GP212NB4
J3.88	GP31NB2	YES	GP211NB4
J3.90	GP32PB2	YES	GP246NB4
J3.92	GP31PB2	YES	GP246PB4
J3.94	GP33NB2	YES	GP210PB4
J3.96	GP35PB2	YES	GP211PB4
J3.98	GP33PB2	YES	GP209PB4
J3.100	GP35NB2	YES	GP212PB4
J3.102	GP30NB2	YES	GP208NB4
J3.104	GP30PB2	YES	GP209NB4

4.1.2 Odd pins

In the table below column DIR contains position of DIR signal on FPGA. To set GPIO as output from board DIR must be set to logic “1”. If GPIO must be input to FPGA, DIR must be set to logic “0”.

Logic Level/ Standard of 5V tolerant I/O: **5VDC TTL I/O Tristateable**

Logic Level/ Standard of 3.3V I/O: **3.3V LVDS or LVCMOS**

Note: If a Pin is 5V tolerant, an additional FPGA pin is used to enable the level translator

Table 8: Mezzanine Connector Odd side pinouts

Mezzanine Pin Number	FPGA Pin	5V Tolerant	FPGA DIR Pin
J3.1	GP304PB2	YES	GP232NB4
J3.3	GP10NB2	YES	GP213NB4
J3.5	GP10PB2	YES	GP213PB4
J3.7	GP304NB2	YES	GP226PB4
J3.9	GP307PB2	YES	GP226NB4
J3.11	GC_W2_GP299NB5	NO	N/A
J3.13	GC_W2_GP299PB5	NO	N/A
J3.15	GP275NB5	NO	N/A
J3.17	GP275PB5	NO	N/A
J3.19	GP272NB5	NO	N/A
J3.21	GP272PB5	NO	N/A

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J3.23	GP273NB5	NO	N/A
J3.25	GP273PB5	NO	N/A
J3.27	GP276NB5	NO	N/A
J3.29	GP276PB5	NO	N/A
J3.31	GP294NB5	NO	N/A
J3.33	GP294PB5	NO	N/A
J3.35	GP11NB2	YES	GP259PB4
J3.37	GP309NB2	YES	GP257NB4
J3.39	GP07NB2	YES	GP260PB4
J3.41	GP09NB2	YES	GP260NB4
J3.43	GP296NB5	NO	N/A
J3.45	GP296PB5	NO	N/A
J3.47	GP279NB5	NO	N/A
J3.49	GP279PB5	NO	N/A
J3.51	GP277_DQSNB5	NO	N/A
J3.53	GP277_DQSPB5	NO	N/A
J3.55	GP274NB5	NO	N/A
J3.57	GP274PB5	NO	N/A
J3.59	SW_P0_1_GP298NB5	NO	N/A
J3.61	SW_P0_1_GP298PB5	NO	N/A
J3.63	GC_W1_GP300NB5	NO	N/A
J3.65	GC_W1_GP300PB5	NO	N/A
J3.67	GC_W0_GP303NB5	NO	N/A
J3.69	GC_W0_GP303PB5	NO	N/A
J3.71	SW_P0_0_DQS_GP301NB5	NO	N/A
J3.73	SW_P0_0_DQS_GP301PB5	NO	N/A
J3.75	GP302NB5	NO	N/A
J3.77	GP302PB5	NO	N/A
J3.79	GP292NB5	NO	N/A
J3.81	GP292PB5	NO	N/A
J3.83	GP295_DQSNB5	NO	N/A
J3.85	GP295_DQSPB5	NO	N/A
J3.87	GP293NB5	NO	N/A
J3.89	GP293PB5	NO	N/A
J3.91	GP297NB5	NO	N/A
J3.93	GP297PB5	NO	N/A
J3.95	GP278NB5	NO	N/A
J3.97	GP278PB5	NO	N/A
J3.99	GP271P_B5	NO	N/A
J3.101	GP34NB2	YES	GP208PB4
J3.103	GP34PB2	YES	GP210NB4

4.2 Transceiver Connector (X2) Pinout

Table 9: Transceiver AUX connector pinout.

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FPGA pin name	QTE pin number		FPGA pin name
XCVR1_TX3+, -	1, 3	2, 4	XCVR1_RX3+, -
XCVR1_TX2+, -	5, 7	6, 8	XCVR1_RX2+, -
XCVR1_TX1+, -	9, 11	10, 12	XCVR1_RX1+, -
XCVR1_TX0+, -	13, 15	14, 16	XCVR1_RX0+, -
XCVR1_A_REFCLK+, -	17, 19	18, 20	CC_W7_GP198B4+,-
XCVR1_B_REFCLK+, -	21, 23	22, 24	VCC_5V (out from board)
XCVR1_C_REFCLK+, -	25, 27	26, 28	OUT3 from SI IC
GND	Blade		GND

4.3 PCIe104 Connector (X1) Pinout

Table 10: PCIe104 connector Pinout

PCIe signal	PCIe104 host pin	FPGA Pin/ Name	notes
PCIe_RST#	2	W2/ GPIO230PB4	
PCIe_CLK+	48	W27/ XCVR_0A_REFCLK_P	
PCIe_CLK-	50	W28/ XCVR_0A_REFCLK_P	
PCIe_TX0+	109	AB33/ XCVR_0_TX3_P	
PCIe_TX0-	111	AB34/ XCVR_0_TX3_N	
PCIe_RX0+	57	AB29/ XCVR_0_RX3_P	
PCIe_RX0-	59	AB30/ XCVR_0_RX3_N	
PCIe_TX1+	115	AA31/ XCVR_0_TX2_P	
PCIe_TX1-	117	AA32/ XCVR_0_TX2_N	
PCIe_RX1+	63	Y29/ XCVR_0_RX2_P	
PCIe_RX1-	65	Y30/XCVR_0_RX2_N	
PCIe_TX2+	121	Y33/ XCVR_0_TX1_P	
PCIe_TX2-	123	Y34/ XCVR_0_TX1_N	
PCIe_RX2+	69	W31/ XCVR_0_RX1_P	
PCIe_RX2-	71	W32/ XCVR_0_RX1_N	
PCIe_TX3+	127	V33/ XCVR_0_TX0_P	
PCIe_TX3-	129	V34/ XCVR_0_TX0_N	
PCIe_RX3+	75	V29/ XCVR_0_RX0_P	
PCIe_RX3-	77	V30/ XCVR_0_RX0_N	

5 BOARD SETUP AND CONFIGURATION

5.1 Programming Configurations

5.2 Boot Sequence

Board provides JTAG interface to the both slots and it can be configured in three ways:

1. Using JTAG

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2. Using embedded FPGA flash

All the three interfaces can be accessed by FlashPro PolarFire v2.3 and later version of the Microsemi Libero design suite.

6 BOARD SUPPORT PACKAGE

A Board support package is available for the PCIe104N which allows the user to work with the board in the Libero SoC PolarFire Design suite (version 2023.2) and select the interfaces available on board to use in block design. Please contact **Sundance DSP Inc** support for further information.

A SW part of BSP is available for Windows 10/11 and can be used to perform functional tests of the board.

Also, the FC205 and SCom cores ported to the PCIe104N are available for this board.
FC205 provides a user-selectable number of standard serial UARTs which may be connected to common external PHYs such as RS-232, RS-422 or RS-485.

Sundance DSP Communications interface (SCom). SCom is a general-purpose multi-channel data interface which is applicable in many different forms and on many different platforms.

6.1 FPGA Demo Design

This chapter describes the provided demo design that demonstrates the high-speed data transfer capability of the PolarFire FPGA using the hardened PCIe EndPoint and DDR4 controller IP. The PCIe controller with a built-in Direct Memory Access (DMA) controller performs high-speed bulk-data transfer between memory locations on a host PC and LSRAM/DDR4 memory on the board. The project also does tests of the FMC+ connector (a special FMC+ loopback module is required) and clock generators which are configured automatically whenever the board powers up.

The following tests are supported:

- PCIe test
- DDR4 test (via PCIe)
- SI5338A configuration
- LSRAM memory test
- Mezzanine connector loopback
- SPI flash test

6.2 Design Requirements

Actual software version: Microchip Libero SoC Design Suite v2023.2.
Required software license types: Platinum, Standalone.

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6.3 Deployment Flow

The project is provided as set of tcl-scripts and sources (hdl, constraints, etc.) packed in a zip archive named as **pcie104n_bsp.zip**. The last numbers in the file name are the project version and are provided here for example purposes only. The actual latest version can be different.

A structure of the project directory:

- **cfg** - Generated bitstream and other configuration files;
- **doc** - Internal documentation used during development;
- **prj** - Project files and scripts;
- **sim** - Simulation files;
- **src** - Sources (hdl, constraints, configuration, etc);
- **tmp** - Temporary files;
- CHANGELOG.md
- README.md

It's needed to unpack the project and then build it with a required version of the Libero SoC software. For that, please, select the menu "**Project -> Execute Script..**." or just press **Ctrl+U** instead. In the opened window fill the path to the script file "**build_project.tcl**" from the "**prj**" directory and click "**Run**". It'll take several minutes until the project has been created in the "**prj**" directory.

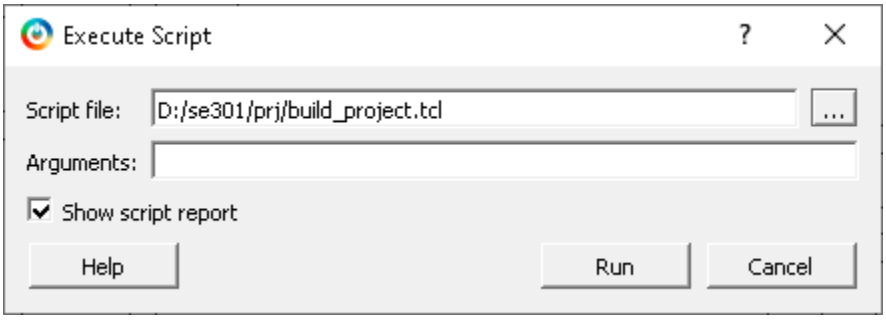

Figure 9: Libero settings for the project build.

6.4 Libero Design Flow

The Libero design flow involves the following main steps:

1. Synthesize
2. Place and route
3. Generate Bitstream
4. Program FPGA

To start any of these steps, go to the **Design Flow** window and double click the corresponding point as shown in the figure below.

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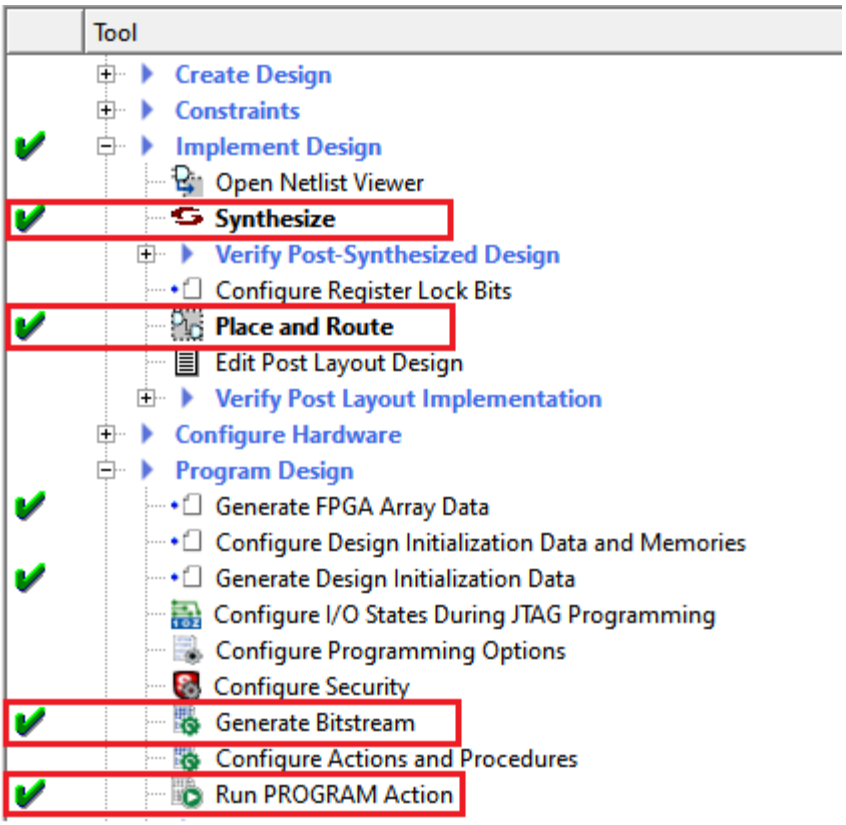

Figure 10: Libero design flow.

Alternatively, to implement the project, please, execute the script "**implement.tcl**" the same way as described above for building procedure. The implementation includes "**Synthesize**" and "**Place and Rote**" steps.

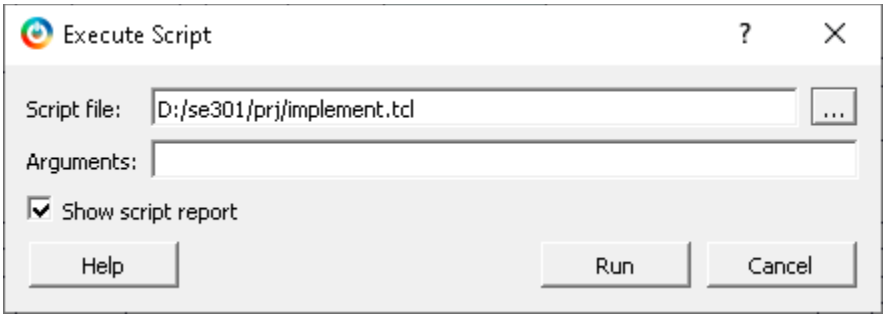

Figure 11: Libero settings for the project implementation by default.

Also, it's possible to generate the bitstream file that can be used to program FPGA.

To do this type "**bitstream**" in the field "**Arguments**" in the window "**Execute Script**" when the script "**implement.tcl**" runs.

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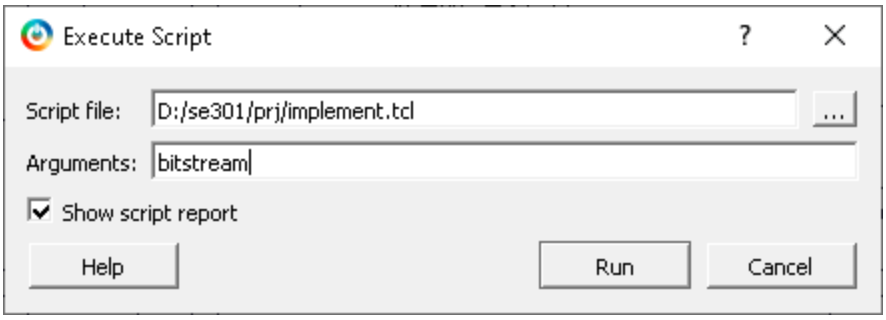

Figure 12: Libero settings for the project implementation with a bitstream generation.

In this case the bitstream generation procedure will start automatically after "**Place and Route**" finishes.

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7 SAFETY

This module presents no hazard to the user.

8 EMC

This module is designed to operate from within an enclosed host system, which is built to provide EMC shielding. Operation within EU EMC guidelines is not guaranteed unless it is installed with an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host system to lockup or reboot.

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