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User Guide for



SoM6 Ti135

Efinix Titanium Ti135 SoM

Form-factor compatible with AMD's Kria™ K24 SoM

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Revision History

Issue	Changes Made	Date	Initials
1.0	Initial draft	19/11/25	CB
1.01	Update	2/9/26	CB

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1 Introduction

1.1 Hardware Features

The SoM6 Ti135 is a compact, low-power System-on-Module (SoM) built around the Efinix Titanium Ti135 FPGA, specifically utilizing the high-density N676 FBGA package. Designed for advanced embedded applications that require performance, flexibility, and energy efficiency, the SoM6 Ti135 integrates a rich set of modern features in a form factor that emphasises modularity and interoperability.

Key Processing and Fabric Features

At the core of the SoM is the Efinix Ti135 FPGA, fabricated on a TSMC 16nm process and featuring the Quantum™ compute fabric. This fabric includes:

- Up to 129,600 logic elements using eXchangeable Logic and Routing (XLR) cells
- 960 blocks of 10-kbit SRAM (totaling ~9.83 Mbits)
- 480 DSP blocks supporting integer and BFLOAT16 computations
- A quad-core hardened RISC-V processor with full support for RV32IMACFD extensions

This makes the SoM6 Ti135 a strong candidate for edge computing, real-time control, and vision-centric workloads.

High-Speed Interfaces and Connectivity

The SoM integrates several high-speed interfaces:

- Two full-duplex transceiver banks (not fully routed on the SoM) capable of, 10G Ethernet (10GBase-KR)**,** SGMII**,** and PMA Direct operation with data rates from 1.25 Gbps to 12.5 Gbps per lane. PCIe Gen 4 is supported at x1 only.
- Dedicated SERDES routing for PCIe and 10G Ethernet
- Extended MIPI D-PHY capabilities supporting up to 2.5 Gbps per lane (TX and RX) via two 30-pin FPC connectors
- A RAW-PMA interface for implementing proprietary high-speed protocols over transceivers

All additional I/O, including power, configuration, and general-purpose signals, are routed through a 240-pin connector (Samtec ADF6–60–03.5–L–4–2–A)**.** This connector is primarily pin-compatible with the AMD Kria K24 SoM, offering a migration path or interoperability for carriers; however, full application-level compatibility cannot be guaranteed due to architectural differences between Efinix's and AMD's FPGAs.

A total of 4 full duplex Transceivers are broken out from the TI135. 1 full duplex channel from Quad Q0 and 3 full duplex channels from Quad Q1.

8-Lane MIPI TX & RX is available but requires configuration, contact Sundance Multiprocessor Ltd for more details. 8-Lane MIPI TX & RX is available but requires configuration, contact Sundance Multiprocessor Ltd for more details.

Memory Resources

The SoM integrates a block of LPDDR for use at runtime

LPDDR4

- LPDDR4 8G Configured as 256Mx32
- Connected to the Ti135 Hard DDR DRAM Interface Hard IP, see Ti135 datasheet for details.

For timing setup refer to DDR4 Test example on the SMT135-C GitHub for more details

QSPI For FPGA Persona Storage and use at Runtime

- QSPI 128Mbit FLASH memory is connected to the Ti135
- It is used to store the Ti135 persona to configure the FPGA at startup and is programmed via the edge connector for details refer to Efinity SW User Guide.

For details refer to the Carrier Hello World example on the SMT135-C GitHub for more details. This will give an example of how to program the QSPI with a persona from the SMT135-C carrier board.

Storage and Security

For onboard non-volatile memory, the SoM6 Ti135 includes:

- eMMC flash storage (soldered on-module for robustness and space efficiency)

For details refer to the eMMC example on the SMT135-C GitHub for more details.

Security is a key focus, with the module integrating the Infineon SLS32AIA010MLUSON10XTMA2 TPM (Trusted Platform Module). This hardware root-of-trust device supports:

- Secure key storage
- Cryptographic operations
- Platform integrity verification

Details of how to program and use this secure element please refer to Infineon see link below.

Clock Sources

For onboard clock sources, the SoM6 Ti135 includes:

A 100Mhz Crystal source for the SoC peripheral clock connected to ball P19 on the Ti135 (PLLIN0)

A 100Mhz Crystal source for the SoC system clock connected to ball on the Ti135 (PLLIN1)

1.2 SoM Module Limitations and Notes

Warning! Only the HVIOs on the Efinix are able to run at 3.3V. This also needs the right settings in the Efinity Interface Designer, otherwise the IO will be permanently damaged. The only FPGA banks supporting 3.3V on this SOM are Banks BL0, BL1 and BL3. To run at 3.3V also the Bank supply voltage on the 240p connector at pins B13 and B14 needs to be at 3.3V. All other Banks that are accessible via the 240p connector are 1.8V unless otherwise specified.

The SoM6 Ti135 is designed for flexible deployment, with reference clocks for the FPGA and peripherals expected to be provided by the carrier board**.** This approach allows tighter system integration and adaptation to specific timing architectures or clock domains on the carrier.

2 Related Documents

Ti135 Data Sheet:-
https://www.efinixinc.com/support/docsdl.php?s=ef&pn=DSTi135

Efinity Software (for FPGA design and programming):-
Efinity Software | Efinix, Inc.

Infineon Secure Element
OPTIGA-TRUST-M-SLS32AIA - OPTIGA™ Trust | Infineon Technologies

SMT135-C GitHub
SundanceMultiprocessorTechnology/SMT135-C

3 Acronyms, Abbreviations and Definitions

FPGA	Field Programmable Gate Array
GigE	Gigabit Ethernet
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group
Kria	Kria™ is a AMD® “System-on-Module”
LVDS	Low Voltage Differential Serial
PCB	Printed Circuit Board
SGMII	Serial Gigabit Media Independent Interface
SPI	Serial Peripheral Interface

4 Interfaces

4.1 SoM6 Ti135 Connector Overview

Table 1: SoM6 Ti135 Board Interfaces

Interface	Description
240p Samtec Connector (ADF6-60-03.5-L-4-2-A)	Intended to connect with the carrier board. This will supply power, control resets, and give access to high voltage IO and high performance IO. Additionally, access to the Ti135 transceivers is given.
30p MIPI connector (503480-2200)	Available two times, gives access to both the TX and RX of the hardened 2.5G MIPI that is available in the Ti135
JTAG Edge connect (ECV3-10-IDC)	JTAG and UART for the test of the SOM without the Carrier.
Operating voltage	5V and direct IO supply (1.2 up to 3.3V)
Total mass	100g without heatsink

4.2 SoM6 Ti135 Block Diagram

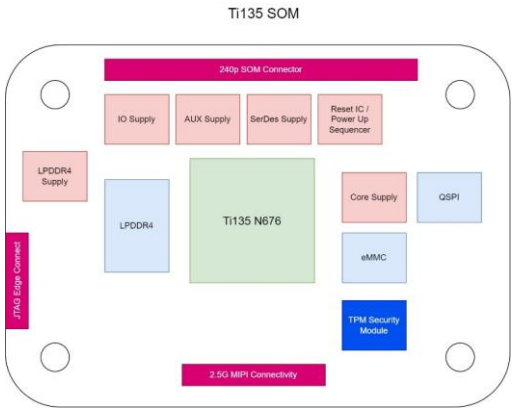
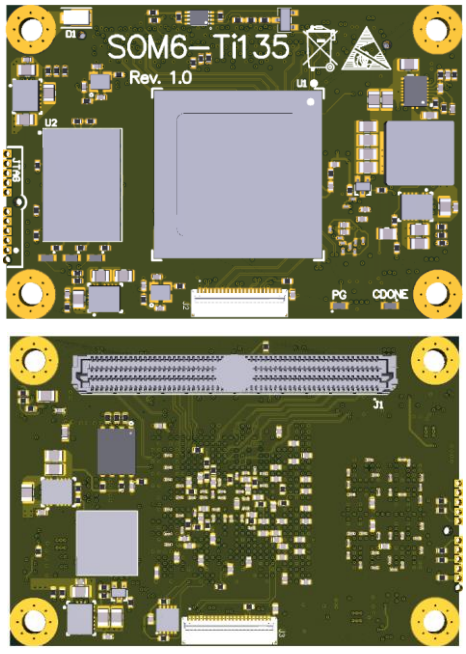


Figure 1: SoM6 Ti135 Block Diagram



4.3 240 Pin SoM Connector

The SoM uses the Samtec ADF6-60-03.5-L-4-2-A.

The connector has the following pinout on this SOM:

Table 2: ADF Pinout Row A

FPGA-Ball	ADF6 PIN	Signal Name
	A1	NC
	A2	GND
M5	A3	GPIOB_06_P
N5	A4	GPIOB_06_N
	A5	GND
N1	A6	GPIOB_00_P
P1	A7	GPIOB_00_N
	A8	GND
P4	A9	GPIOB_04_P
P3	A10	GPIOB_04_N
	A11	GND
M4	A12	GPIOB_13_N
L4	A13	GPIOB_13_P
	A14	GND
AA5	A15	GPIOL_05
W7	A16	GPIOL_02
V5	A17	GPIOL_10
	A18	GND
	A19	0V85_PG
	A20	0V85_PG
	A21	GND
J7	A22	JTAG_TMS_C2M
J8	A23	JTAG_TDO_M2C
F8	A24	JTAG_TDI_C2M
G8	A25	JTAG_TCK_C2M
	A26	GND
D1	A27	CBSEL1
C1	A28	CBSEL0
T20	A29	GPIOT_P13
P20	A30	GPIOT_P19
	A31	NC
	A32	NC
	A33	GND
U18	A34	GPIOT_N_01
R17	A35	GPIOT_N_08
U19	A36	GPIOT_P_01
	A37	GND
K18	A38	GPIOR_82
H3	A39	GPIOB_P_18
G5	A40	GPIOR_128
	A41	GND
G3	A42	GPIOB_N_18
F7	A43	GPIOR_132

F6	A44	GPIOR_131_PERST_N
	A45	GND
	A46	GND
C13	A47	Q1_TX0_P
D13	A48	Q1_TX0_N
	A49	GND
	A50	GND
E12	A51	Q0_CLK1_P
F12	A52	Q0_CLK1_N
	A53	GND
	A54	GND
A6	A55	Q0_RX0_P
B6	A56	Q0_RX0_N
	A57	GND
	A58	GND
	A59	VCC_SOM
	A60	VCC_SOM

Table 3: ADF Pinout Row B

FPGA-Ball	ADF6 PIN	Signal Name
N3	B1	GPIOB_05_N
M3	B2	GPIOB_05_P
	B3	GND
N8	B4	GPIOB_07_P
P8	B5	GPIOB_07_N
	B6	GND
K2	B7	GPIOB_11_P
K1	B8	GPIOB_11_N
	B9	GND
H1	B10	GPIOB_08_P
J1	B11	GPIOB_08_N
	B12	GND
	B13	VCCIO_HVIO
	B14	VCCIO_HVIO
	B15	GND
Y6	B16	GPIOL_03
V6	B17	GPIOL_11
U3	B18	GPIOL_17
	B19	GND
V4	B20	GPIOL_16
R1	B21	GPIOL_34_PLLIN
R2	B22	GPIOL_33
	B23	GND
	B24	NC
	B25	NC
	B26	PWROFF_C2M_L
	B27	GND
T21	B28	GPIOT_N_16
U21	B29	GPIOT_P_16
P18	B30	GPIOT_N_20
	B31	GND
P23	B32	GPIOT_N_23
	B33	NC
V21	B34	GPIOT_N_04
	B35	GND
R18	B36	GPIOT_P_07
V22	B37	GPIOT_P_06
	B38	NC
	B39	GND
K19	B40	GPIOR_84
J19	B41	GPIOR_85
	B42	GPIOR_125
	B43	GND
H6	B44	GPIOR_83
E1	B45	GPIOB_21_N
E2	B46	GPIOB_21_P
	B47	GND
	B48	GND
E16	B49	Q1_CLK0_P

F16	B50	Q1_CLK0_N
	B51	GND
	B52	GND
A16	B53	Q1_RX1_P
B16	B54	Q1_RX1_N
	B55	GND
	B56	GND
C5	B57	Q0_TX0_P
D5	B58	Q0_TX0_N
	B59	GND
	B60	VCC_SOM

Table 4: ADF Pinout Row C

FPGA-Ball	ADF6 PIN	Signal Name
	C1	GND
	C2	GND
P6	C3	GPIOB_03_P
P5	C4	GPIOB_03_N
	C5	GND
M8	C6	GPIOB_12_P
M7	C7	GPIOB_12_N
	C8	GND
G2	C9	GPIOB_14_P
H2	C10	GPIOB_14_N
	C11	GND
J4	C12	GPIOB_16_P
J3	C13	GPIOB_16_N
	C14	GND
POR IN	C15	PS_POR_L
RESET Input	C16	PS_SRST_C2M_L
	C17	GND
V7	C18	GPIOL_13
AC5W8	C19	GPIOL_08
	C20	GPIOL_12
	C21	GND
T1	C22	GPIOL_28
T5	C23	GPIOL_25_PLLIN1
R3	C24	GPIOL_32_PLLIN
	C25	GND
Y17	C26	GPIOL_65
W17	C27	GPIOL_64
W19	C28	GPIOL_63
	C29	GND
R20	C30	GPIOT_N_13
P17	C31	GPIOT_P_17
N17	C32	GPIOT_N_17
	C33	GND
T18	C34	GPIOT_N_02

W25	C35	GPIOT_P_09
V25	C36	GPIOT_N_09
	C37	GND
R23	C38	GPIOT_P_23
K21	C39	GPIOR_80
J21	C40	GPIOR_79
	C41	GND
J6	C42	GPIOB_P_28
F1	C43	GPIOB_17_N
F2	C44	GPIOB_17_P
	C45	NC
	C46	GND
E10	C47	Q0_CLK0_P
F10	C48	Q0_CLK0_N
	C49	GND
	C50	GND
C17	C51	Q1_TX2_P
D17	C52	Q1_TX2_N
	C53	GND
	C54	GND
A14	C55	Q1_RX0_P
B14	C56	Q1_RX0_N
	C57	GND
	C58	GND
	C59	VCC_SOM
	C60	VCC_SOM

Table 5: ADF Pinout Row D

FPGA-Ball	ADF6 PIN	Signal Name
	D1	VCC0_BANK4B
	D2	VCC0_BANK4B
	D3	GND
N7	D4	GPIOB_10_P
N6	D5	GPIOB_10_N
	D6	GND
L6	D7	GPIOB_09_P
L5	D8	GPIOB_09_N
	D9	GND
K4	D10	GPIOB_15_P
K3	D11	GPIOB_15_N
	D12	GND
L2	D13	GPIOB_01_P
L1	D14	GPIOB_01_N
	D15	GND
AB6	D16	GPIOL_07
AB5	D17	GPIOL_06
Y7	D18	GPIOL_04
	D19	GND
AC6	D20	GPIOL_09

W6	D21	GPIOL_00
Y5	D22	GPIOL_01
	D23	GND
	D24	VDDQX_PG
	D25	VDDQX_PG
G9	D26	CDONE
	D27	GND
V25	D28	GPIOT_N_10
U22	D29	GPIOT_N_07
T19	D30	GPIOT_P_02
	D31	GND
V21	D32	GPIOT_P_04
W22	D33	GPIOT_N_05
W23	D34	GPIOT_P_05_PLLIN
	D35	GND
N20	D36	GPIOT_N_19
R21	D37	GPIOT_N_22
W23	D38	GPIOT_P_05_PLLIN
	D39	GND
H21	D40	GPIOR_78_PLLIN
F4	D41	GPIOB_N_24
C2	D42	GPIOB_N_23
	D43	GND
B1	D44	GPIOB_P_20
A2	D45	GPIOB_N_20
	D46	NC
	D47	GND
	D48	GND
A18	D49	Q1_RX2_P
B18	D50	Q1_RX2_N
	D51	GND
	D52	GND
E12F12	D53	Q1_CLK1_P
	D54	Q1_CLK1_N
	D55	GND
	D56	GND
C15	D57	Q1_TX1_P
D17	D58	Q1_TX1_N
	D59	GND
	D60	VCC_SOM

5 Environmental

SoM6 Ti135 will require either Active cooling, which requires a heatsink and fan, or Convection cooling, which requires just a heatsink; either of these solutions will allow the SoM6 Ti135 to operate in an environment up to 60°C. The choice of active or convection cooling will dictate the specific temperature grade of the FPGA.

6 Power and Electrical

Table 6: SoM6 Ti135 Power Specifications

Parameter	Description
Supply Voltages	5V DC SoM Mounting Holes 3 and 4 Connected to GND SoM Mounting Holes 1 and2 Connected to +5V +5V Min 4.6V Max 5.6V (TBC)
Max Supply Current	2 Amps
Power consumption of SoM6	0.5W Running LPDDR4x test
Maximum power consumption of SoM6	5W
Power available on MIPI Connectors	Contact Sundance

Commented [FC1]: @Fabian KLUGE - not sure you get this as a notification, but I added a comments/question, ie.

"What power is provided on the MIPI connectors? - or did we forget