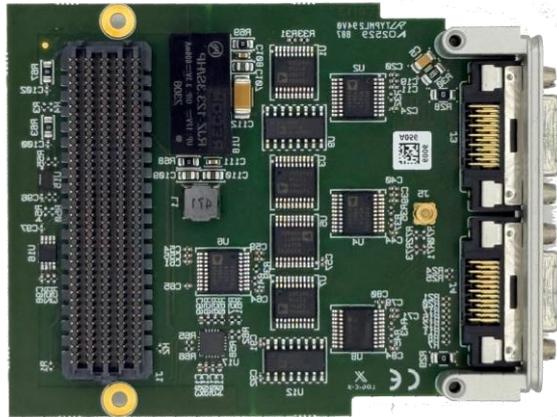


LXD40K0 - CameraLink FMC

Featuring Galvanic Isolation Between I/O and FMC Connector



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1 General Description

The LX40K0 FMC (FPGA Mezzanine Card) is designed to support Camera Link interfaces with galvanic isolation, ensuring electrical separation between the I/O and the FMC connector. The module is fully compatible with Base, Medium, and Full Camera Link standards, and can be reconfigured to support a dual Base Camera Link setup if required.

This product is part of the Logic-X stackable FMC product line, which enables flexible configurations. Two LX40K0 modules can be stacked to create a dual-Medium/Full or quad-Base Camera Link interface on a single low-pin-count FMC site.

The PCB design is divided into two isolated sections, providing isolation between the front panel and the FMC connector. This design enhances signal integrity and electromagnetic compatibility (EMC), offering a robust and reliable isolated interface for demanding Camera Link applications. Since the product incorporates standard LVDS receivers, it is not limited to Camera Link operation. Other LVDS-based signalling protocols can also be mapped onto these lanes as required.

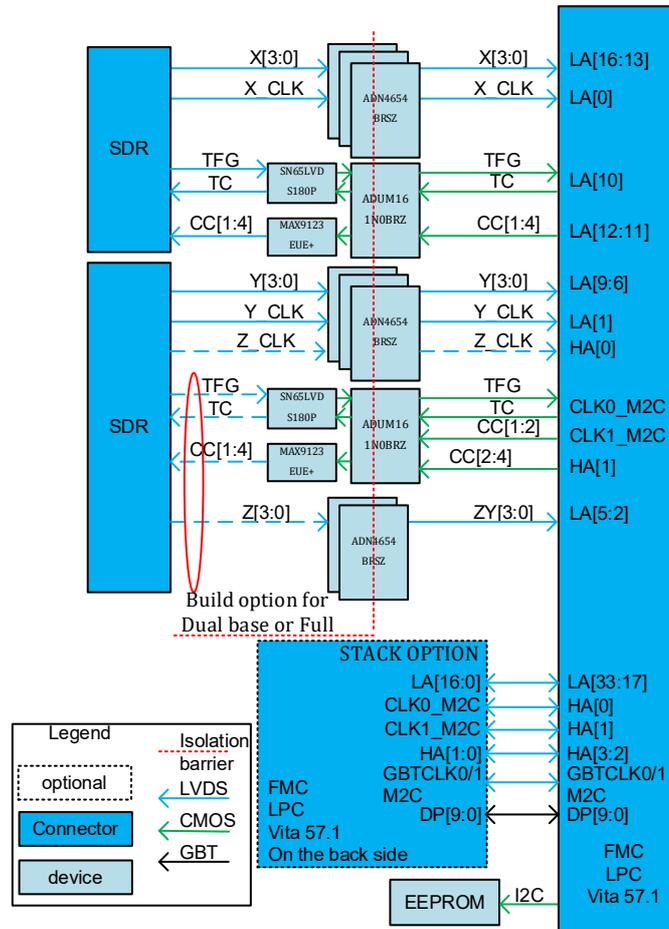


Figure 1: LX40K0 block diagram

2 Mechanical design

The board design is mechanically compliant with the VITA 57.1 (FMC) specification, with one exception: the top-side isolated power supply exceeds the specified 4.7 mm maximum height by approximately 2.8 mm.

According to the VITA 57.1 standard, the maximum component height is 1.3 mm on the bottom side and 4.7 mm on the top side of the board. This design maintains compliance with all other mechanical requirements and targets the conduction-cooled FMC format, including Region 1 for the I/O connectors.

The overall board dimensions and the component height exception are illustrated in the image below.

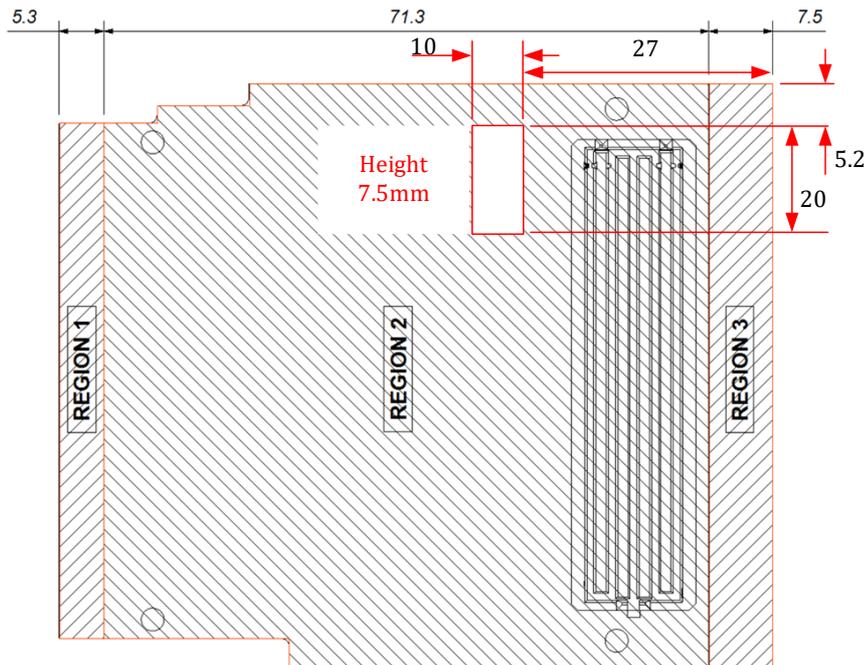


Figure 2: Board mechanical dimensions and component height violation.

2.1 Cooling

To maintain optimal operating temperatures, forced airflow is recommended for cooling.

2.2 Front panel design

The PCB's front panel provides access to two mini SDR connectors through openings in a standard FMC bezel as shown in the following figure.



Figure 3: LX40K0 bezel design

The corresponding Camera Link interface mapping is detailed in the following table.

Table 1: Front panel connectors

Connector	Cameralink cable
P1	BASE 1
P2	BASE 2 (LXD40K1) MEDIUM/FULL (LXD40K0)

3 CameraLink interface

The board supports two build options for the Camera Link interface:

1. Base/Medium/Full configuration, or
2. Dual-Base configuration.

The Camera Link interface utilizes LVDS signalling for all connections. These signals are divided into two categories:

- High-speed video data signals, which can reach data rates of up to 560 Mbps, and
- Control and serial communication signals, which typically operate at data rates of only a few Mbps.

Because of this difference, only the high-speed video data signals are buffered LVDS-to-LVDS, ensuring optimal signal integrity. The control and serial communication signals, on the other hand, are implemented as LVCMOS signals on the FMC connector side and are translated to and from LVDS via dedicated buffers.

To achieve galvanic isolation, all signals pass through isolation buffers, effectively separating the I/O from the FMC connector and enhancing electrical safety and noise immunity.

3.1 LXD40K0 base/medium/full configuration

The base build option of the LXD40K0 supports the Base, Medium, and Full Camera Link configurations. In this configuration, the Z_CLK signal is routed to the FMC HA[0] line. As a result, an LPC (Low Pin Count) FMC site cannot use the Z clock to sample the Z data directly. However, based on prior design experience, FPGAs are capable of reliably capturing data from a single Camera Link cable using a single clock source—in this case, the Y_CLK signal. The block diagram in the following image illustrates the Base/Medium/Full configuration of the LXD40K0.

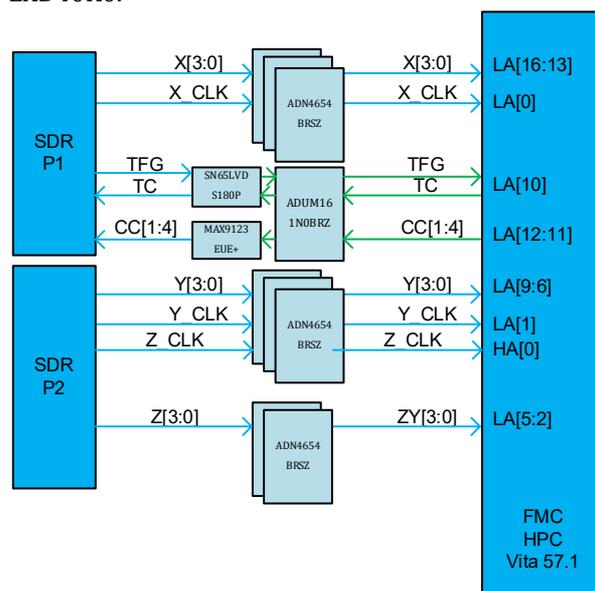


Figure 4: LXD40K0 Base/medium/full CameraLink interface build option

3.2 LXD40K1 dual base configuration

As a build option, the LXD40K0 can be configured as the LXD40K1, which provides a dual Base Camera Link interface. In this configuration:

- The TFG and TC signals are routed to the FMC CLK0_M2C line.
- The CC[1:2] signals are routed to the FMC CLK1_M2C line.

This routing ensures that these signals remain accessible on LPC-compatible carrier boards. Although the signal names CLK0/1_M2C imply mezzanine-to-carrier directionality, on most FMC carrier boards these signals connect directly to FPGA pins capable of bidirectional operation. The remaining CC[2:4] signals are routed to the FMC HA[1] line, making them available only on carriers that support this signal. However, most Camera Link cameras do not require the CC[2:4] signals for standard operation.

This signal routing provides maximum flexibility while preserving the ability to stack two FMC modules on a low-pin-count carrier. A block diagram of the dual-base configuration is shown in the following image.

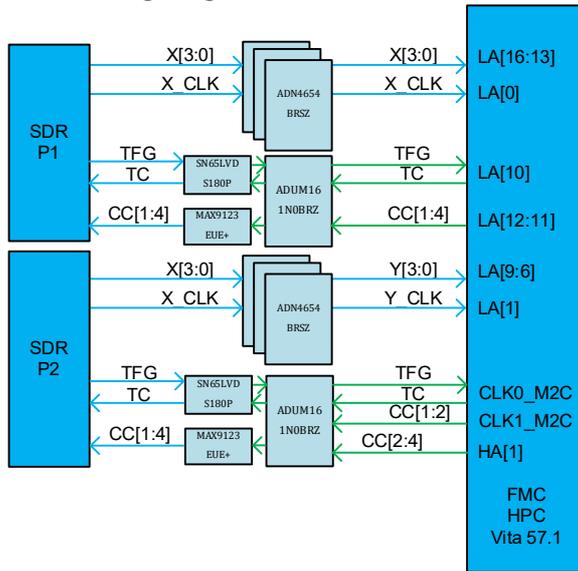


Figure 5: Dual base CameraLink interface build option

4 Stacked configuration

The LX40K0 FMC board is part of the Logic-X stackable FMC product line. These products are designed with a build option that allows an additional FMC module to be stacked on the back side of the board. This enables designers to leverage the extra I/O resources available on the carrier board, provided the system can accommodate the additional height introduced by stacking. Within the stackable product line, the following signal routing scheme is implemented between the mezzanine FMC connector and the stack FMC connector:

- LA[33:17], HA[3:2], CLK0_M2C, and CLK1_M2C on the mezzanine connector are routed to LA[16:0], HA[1:0], CLK2_BIDIR, and CLK3_BIDIR, respectively, on the stack connector.
- All high-speed gigabit transceiver lanes are directly routed from the mezzanine FMC connector to the stack FMC connector.

This architecture provides a flexible and scalable platform, allowing multiple FMC modules to operate in combination while maintaining signal integrity and carrier compatibility.

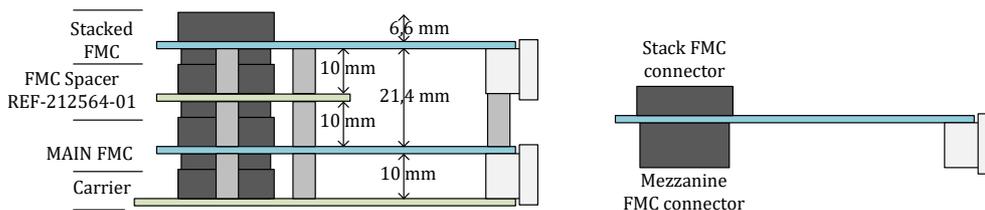


Figure 6: Logic-X stackable FMC concept

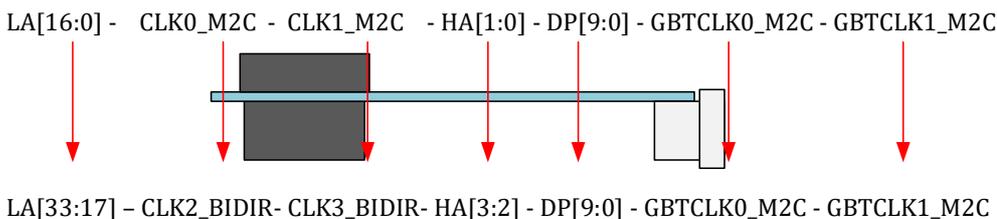


Figure 7: Stack to main signal mapping.

4.1 Stacked LX40K2 Dual base/medium/full configuration

It is possible to stack two LX40K0 modules to create a dual-Medium configuration or to provide two independent Base/Medium/Full Camera Link interfaces. This configuration is available under the dedicated part number LX40K2.

In this setup, the LX40K2 assembly consists of two LX40K0 boards that are stacked and tested together as a complete, verified unit. This approach ensures proper signal integrity, mechanical alignment, and electrical compatibility between the two modules. The resulting architecture is illustrated in the block diagram shown below.

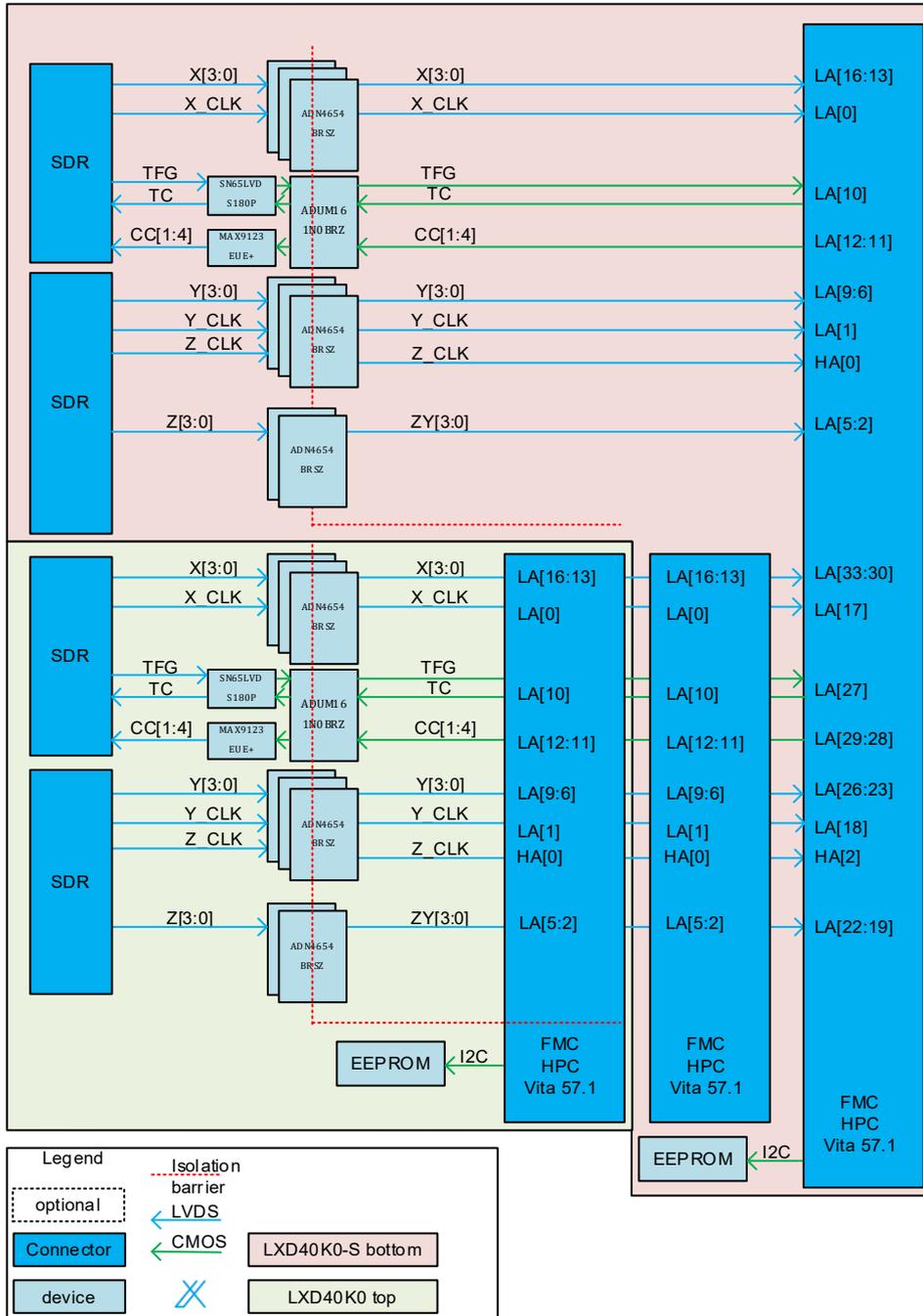


Figure 8: LX40K2 dual medium or dual base/medium full stack

4.2 LXD40K4 Quad base configuration

Similar to the LXD40K2 stack, it is also possible to stack two LXD40K1 modules to create a quad Base Camera Link interface. This configuration is offered under the dedicated part number LXD40K4.

In this setup, the LXD40K4 assembly consists of two LXD40K1 boards that are stacked and tested together as a single qualified unit. This design enables four independent Base Camera Link channels within one compact, stackable FMC assembly.

The resulting configuration is illustrated in the block diagram shown below.

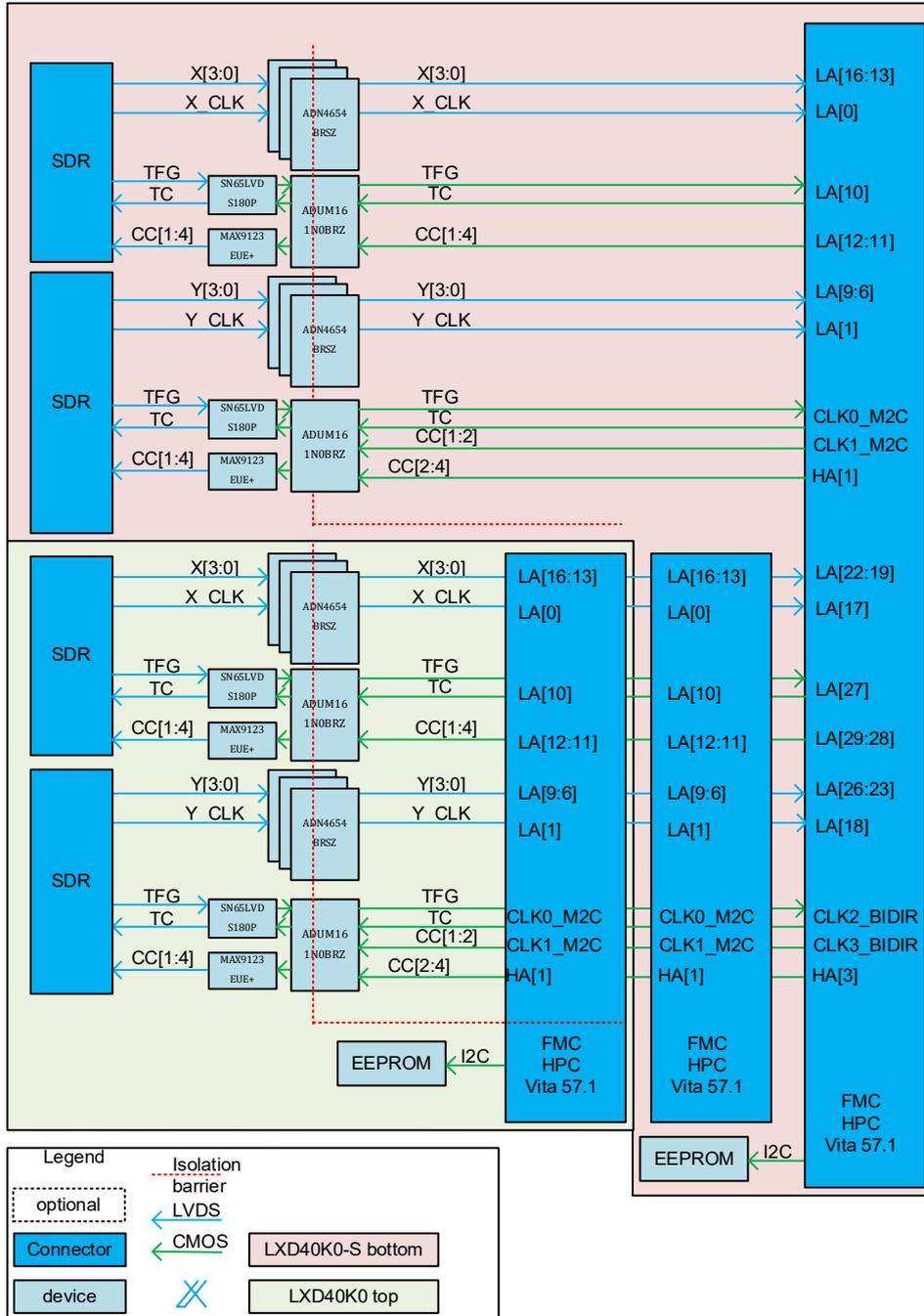


Figure 9: LXD40K4 quad base stack

4.3 Camera data interface

Within the Camera Link standard, video data is transmitted through Channel Link channels, each consisting of one LVDS clock signal and four LVDS data signals. On the LXD40K0, these Channel

Link channels are implemented using ADN4654BRSZ isolation buffers to provide the required galvanic isolation.

A total of three channels—X, Y, and Z—are implemented. All three channels share an identical design, with the exception that the Z channel’s clock signal is connected to the same isolation buffer as the Y_CLK.

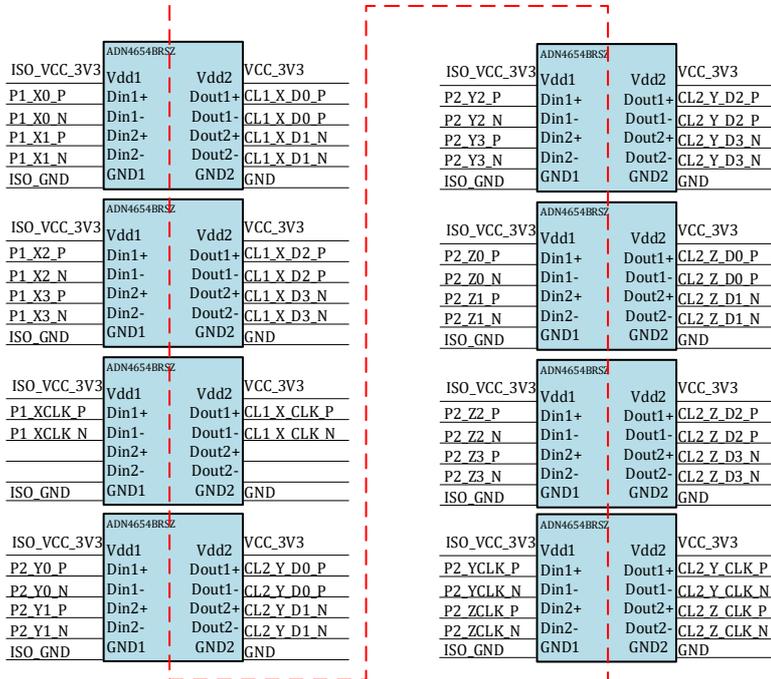


Figure 10: LX D40K0 channel link isolation design

4.4 Camera control interface

On the Base Camera Link connector, there are four control output signals (CC[3:0]) and a serial communication channel (SerTC and SerTFG). This interface is implemented using a two-stage design approach:

1. Stage 1: The LVCMOS signals are first transferred to the isolated domain.
2. Stage 2: The signals are then translated to and from LVDS, completing the galvanically isolated interface.

The diagram below illustrates the design of the control interface.

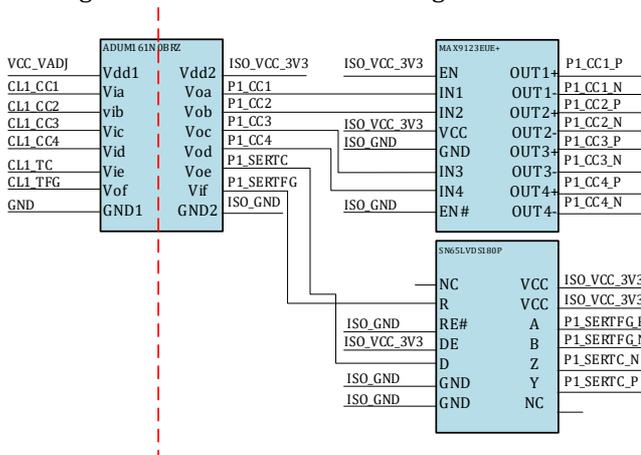


Figure 11: Camera control interface isolation design

This same interface architecture is used in the dual-Base build option. The difference is that, in this configuration, zero-ohm resistors are placed in series with the differential pairs to accommodate either the Base/Medium/Full or Dual-Base build variants.

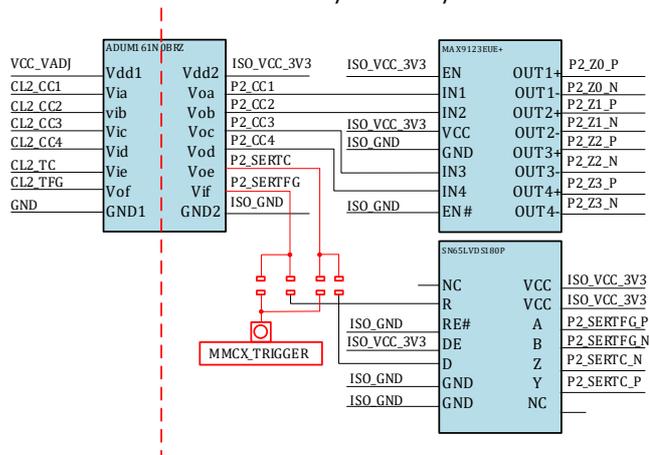


Figure 12: Camera 2 control interface isolation design.

4.4.1 MMCX GPIO

As an optional build feature, a signal from an MMCX connector (not part of the front-panel I/O) can be routed to function as either an isolated input or an isolated output. This MMCX connection is typically linked to the system I/O panel using an MMCX-to-BMC bulkhead cable, providing flexible access to isolated GPIO functionality for system integration or testing purposes. This is at the expense of the P2 SERTC/SERTFG signalling, which is not used in a medium full configuration.

4.5 CameraLink front panel connector

The LX40K0 utilizes an SDR connector for the Camera Link interface, specifically the 12226-5100-00FR model.



5 FMC interface

The LX40K0 is an FMC card designed for use with a Low Pin Count (LPC) connector.

For standard operation, the module functions as a Low Pin Count FMC, utilizing the following signals:

- LA[16:0]
- CLK0_M2C
- CLK1_M2C

For stacked configurations (two LX40K0 modules), additional signals are required:

- CLK2_BIDIR
- CLK3_BIDIR
- LA[33:17]
- with HA[1:0] being optional.

To enable stacking with a board that employs multi-gigabit transceivers, the LX40K0 also routes all DP_C2M and DP_M2C signals directly between the two FMC connectors.

This provides full high-speed signal continuity for stackable designs.

5.1 Utility connections

The following table summarizes how the utility connection signals are implemented on the LX40K0.

Table 2: FMC utility connections

Signal name	Connected to
PRSNT_M2C	Tied to GND
PG_C2M	Used to enable local power supplies
TCK	Not used
TDI	connected to TDO
TDO	connected to TDI
SCL	See chapter on I2C
SDA	See chapter on I2C
TMS	Not used
TRST_L	Not used
GA0	See chapter on I2C
GA1	See chapter on I2C
RES0	Not used
PG_M2C	Asserted when the carrier asserts PG_C2M and the local power goods are asserted

5.2 Gigabit transceiver connections

The LX40K0 routes all Gigabit transceiver connections directly to the stack connector, ensuring full high-speed signal continuity between stacked modules.

5.3 I/O Standard Support

Most signal connections to the FMC connector on the LX40K0 are differential LVDS signals. The LVCMOS control signals are passed through level translators powered by the VADJ rail on the FMC side. This ensures proper operation across a wide VADJ voltage range from 1.2 V to 3.3 V, providing compatibility with a broad range of carrier board designs.

5.4 VIO_B_M2C Support

The LX40K0 connects VIO_B_M2C directly to VADJ.

5.5 VREF Support

The VREF_A_M2C and VREF_B_M2C signals are left unconnected on the LX40K0.

6 I2C Interface

The LX40K0 includes an FMC identification EEPROM that is connected directly to the FMC I²C bus and remains active with only the 3V3_AUX supply.

The I²C schematic illustrating this implementation is shown in the following figure.

3V3_AUX

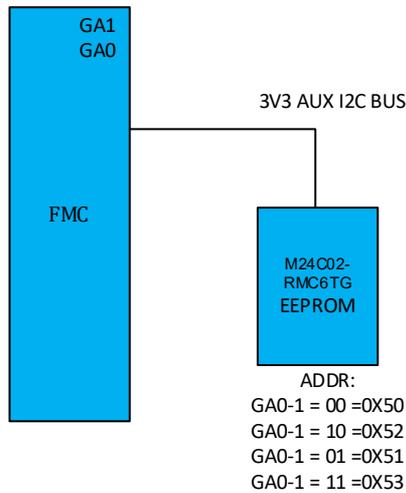


Figure 13:I2C schematic

7 JTAG

The LX40K0 does not participate in the JTAG chain. Instead, the TDI signal is looped back to the TDO signal on the board, maintaining JTAG continuity through the FMC connector.

8 Power Design

An FMC module receives multiple supply voltages from the FMC connector, namely +12 V, +3.3 V, VADJ, and +3.3 V_AUX. The LX40K0 utilizes all four supply rails to power its isolated interfaces and logic circuitry. The table below summarizes the typical power consumption and current draw of the LX40K0 for each voltage rail:

Table 3: Power consumption

Voltage Rail	Maximum Available by FMC specification(A)	Typical Current (A)	Typical Power (Watts)
VADJ	4	0.02	0,04 @ 1.8V
3P3V	3	0.4	1.32
12P0V	1	0.14	1.77
3P3VAUX (Operating)	0.020	0.010	0.033
3P3VAUX (Standby)	0.000001	0.000001	0.0000033

The power tree is depicted in the following image.

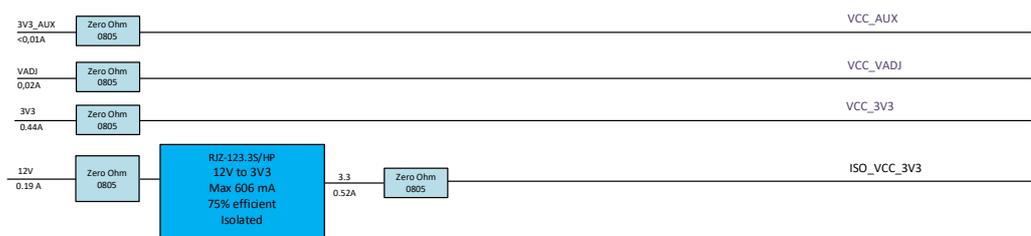


Figure 14: Power tree

9 Ordering options

Ordering code	Description	Can be used as main in FMC stack	Can be used as stacked in FMC stack
LXD40K0	Base/medium/full CameraLink interface.	NO	YES
LXD40K0-S	Base medium full CameraLink interface.	YES	YES
LXD40K1	Dual base CameraLink interface.	NO	YES
LXD40K1-S	Dual base CameraLink interface	YES	YES
LXD40K2	Stack of two LXD40K0-S forming a Dual base/medium/full CameraLink interface.	N.A.	N.A.
LXD40K4	Stack of two LXD40K1-S forming a Quad base CameraLink interface.	N.A.	N.A.

Appendix A: FMC mezzanine connector ICD

Connector vendor : Samtec

Connector part number: ASP-134488-01

AV57	Con. Pin	Net name	AV57	Con. Pin	Net name
CLK0_M2C_N	H5	CL2_TFG	DP8_M2C_P	B8	STACK_DP8_M2C_P
CLK0_M2C_P	H4	CL2_TC	DP9_C2M_N	B25	STACK_DP9_C2M_N
CLK1_M2C_N	G3	CL2_CC1	DP9_C2M_P	B24	STACK_DP9_C2M_P
CLK1_M2C_P	G2	CL2_CC2	DP9_M2C_N	B5	STACK_DP9_M2C_N
CLK2_BIDIR_N	K5	STACK_CLK0_M2C_N	DP9_M2C_P	B4	STACK_DP9_M2C_P
CLK2_BIDIR_P	K4	STACK_CLK0_M2C_P	GBTCLK0_M2C_N	D5	STACK_GBTCLK0_M2C_N
CLK3_BIDIR_N	J3	STACK_CLK1_M2C_N	GBTCLK0_M2C_P	D4	STACK_GBTCLK0_M2C_P
CLK3_BIDIR_P	J2	STACK_CLK1_M2C_P	GBTCLK1_M2C_N	B21	STACK_GBTCLK1_M2C_N
DP0_C2M_N	C3	STACK_DP0_C2M_N	GBTCLK1_M2C_P	B20	STACK_GBTCLK1_M2C_p
DP0_C2M_P	C2	STACK_DP0_C2M_P	HA00_N_CC	F5	CL2_Z_CLK_N
DP0_M2C_N	C7	STACK_DP0_M2C_N	HA00_P_CC	F4	CL2_Z_CLK_P
DP0_M2C_P	C6	STACK_DP0_M2C_P	HA01_N_CC	E3	CL2_CC3
DP1_C2M_N	A23	STACK_DP1_C2M_N	HA01_P_CC	E2	CL2_CC4
DP1_C2M_P	A22	STACK_DP1_C2M_P	HA02_N	K8	STACK_HA00_N_CC
DP1_M2C_N	A3	STACK_DP1_M2C_N	HA02_P	K7	STACK_HA00_P_CC
DP1_M2C_P	A2	STACK_DP1_M2C_P	HA03_N	J7	STACK_HA01_N_CC
DP2_C2M_N	A27	STACK_DP2_C2M_N	HA03_P	J6	STACK_HA01_P_CC
DP2_C2M_P	A26	STACK_DP2_C2M_P	HA04_N	F8	n.c.
DP2_M2C_N	A7	STACK_DP2_M2C_N	HA04_P	F7	n.c.
DP2_M2C_P	A6	STACK_DP2_M2C_P	HA05_N	E7	n.c.
DP3_C2M_N	A31	STACK_DP3_C2M_N	HA05_P	E6	n.c.
DP3_C2M_P	A30	STACK_DP3_C2M_P	HA06_N	K11	n.c.
DP3_M2C_N	A11	STACK_DP3_M2C_N	HA06_P	K10	n.c.
DP3_M2C_P	A10	STACK_DP3_M2C_P	HA07_N	J10	n.c.
DP4_C2M_N	A35	STACK_DP4_C2M_N	HA07_P	J9	n.c.
DP4_C2M_P	A34	STACK_DP4_C2M_P	HA08_N	F11	n.c.
DP4_M2C_N	A15	STACK_DP4_M2C_N	HA08_P	F10	n.c.
DP4_M2C_P	A14	STACK_DP4_M2C_P	HA09_N	E10	n.c.
DP5_C2M_N	A39	STACK_DP5_C2M_N	HA09_P	E9	n.c.
DP5_C2M_P	A38	STACK_DP5_C2M_P	HA10_N	K14	n.c.
DP5_M2C_N	A19	STACK_DP5_M2C_N	HA10_P	K13	n.c.
DP5_M2C_P	A18	STACK_DP5_M2C_P	HA11_N	J13	n.c.
DP6_C2M_N	B37	STACK_DP6_C2M_N	HA11_P	J12	n.c.
DP6_C2M_P	B36	STACK_DP6_C2M_P	HA12_N	F14	n.c.
DP6_M2C_N	B17	STACK_DP6_M2C_N	HA12_P	F13	n.c.
DP6_M2C_P	B16	STACK_DP6_M2C_P	HA13_N	E13	n.c.
DP7_C2M_N	B33	STACK_DP7_C2M_N	HA13_P	E12	n.c.
DP7_C2M_P	B32	STACK_DP7_C2M_P	HA14_N	J16	n.c.
DP7_M2C_N	B13	STACK_DP7_M2C_N	HA14_P	J15	n.c.
DP7_M2C_P	B12	STACK_DP7_M2C_P	HA15_N	F17	n.c.

DP8_C2M_N	B29	STACK_DP8_C2M_N	HA15_P	F16	n.c.
DP8_C2M_P	B28	STACK_DP8_C2M_P	HA16_N	E16	n.c.
DP8_M2C_N	B9	STACK_DP8_M2C_N	HA16_P	E15	n.c.
HA17_N_CC	K17	n.c.	HB15_N	J34	n.c.
HA17_P_CC	K16	n.c.	HB15_P	J33	n.c.
HA18_N	J19	n.c.	HB16_N	F35	n.c.
HA18_P	J18	n.c.	HB16_P	F34	n.c.
HA19_N	F20	n.c.	HB17_N_CC	K38	n.c.
HA19_P	F19	n.c.	HB17_P_CC	K37	n.c.
HA20_N	E19	n.c.	HB18_N	J37	n.c.
HA20_P	E18	n.c.	HB18_P	J36	n.c.
HA21_N	K20	n.c.	HB19_N	E34	n.c.
HA21_P	K19	n.c.	HB19_P	E33	n.c.
HA22_N	J22	n.c.	HB20_N	F38	n.c.
HA22_P	J21	n.c.	HB20_P	F37	n.c.
HA23_N	K23	n.c.	HB21_N	E37	n.c.
HA23_P	K22	n.c.	HB21_P	E36	n.c.
HB00_N_CC	K26	n.c.	LA00_N_CC	G7	CL1_X_CLK_N
HB00_P_CC	K25	n.c.	LA00_P_CC	G6	CL1_X_CLK_P
HB01_N	J25	n.c.	LA01_N_CC	D9	CL2_Y_CLK_N
HB01_P	J24	n.c.	LA01_P_CC	D8	CL2_Y_CLK_P
HB02_N	F23	n.c.	LA02_N	H8	CL2_Z_D3_N
HB02_P	F22	n.c.	LA02_P	H7	CL2_Z_D3_P
HB03_N	E22	n.c.	LA03_N	G10	CL2_Z_D2_N
HB03_P	E21	n.c.	LA03_P	G9	CL2_Z_D2_P
HB04_N	F26	n.c.	LA04_N	H11	CL2_Z_D0_N
HB04_P	F25	n.c.	LA04_P	H10	CL2_Z_D0_P
HB05_N	E25	n.c.	LA05_N	D12	CL2_Z_D1_N
HB05_P	E24	n.c.	LA05_P	D11	CL2_Z_D1_P
HB06_N_CC	K29	n.c.	LA06_N	C11	CL2_Y_D3_N
HB06_P_CC	K28	n.c.	LA06_P	C10	CL2_Y_D3_P
HB07_N	J28	n.c.	LA07_N	H14	CL2_Y_D2_N
HB07_P	J27	n.c.	LA07_P	H13	CL2_Y_D2_P
HB08_N	F29	n.c.	LA08_N	G13	CL2_Y_D1_N
HB08_P	F28	n.c.	LA08_P	G12	CL2_Y_D1_P
HB09_N	E28	n.c.	LA09_N	D15	CL2_Y_D0_N
HB09_P	E27	n.c.	LA09_P	D14	CL2_Y_D0_P
HB10_N	K32	n.c.	LA10_N	C15	CL1_TFG
HB10_P	K31	n.c.	LA10_P	C14	CL1_TC
HB11_N	J31	n.c.	LA11_N	H17	CL1_CC1
HB11_P	J30	n.c.	LA11_P	H16	CL1_CC2
HB12_N	F32	n.c.	LA12_N	G16	CL1_CC3
HB12_P	F31	n.c.	LA12_P	G15	CL1_CC4
HB13_N	E31	n.c.	LA13_N	D18	CL1_X_D2_N
HB13_P	E30	n.c.	LA13_P	D17	CL1_X_D2_P

HB14_N	K35	n.c.	LA14_N	C19	CL1_Z_D3_N
HB14_P	K34	n.c.	LA14_P	C18	CL1_X_D3_P
LA15_N	H20	CL1_X_D1_N	LA25_N	G28	STACK_LA08_N
LA15_P	H19	CL1_X_D1_P	LA25_P	G27	STACK_LA08_P
LA16_N	G19	CL1_X_D0_N	LA26_N	D27	STACK_LA09_N
LA16_P	G18	CL1_X_D0_P	LA26_P	D26	STACK_LA09_P
LA17_N_CC	D21	STACK_LA00_N_CC	LA27_N	C27	STACK_LA10_N
LA17_P_CC	D20	STACK_LA00_P_CC	LA27_P	C26	STACK_LA10_P
LA18_N_CC	C23	STACK_LA01_N_CC	LA28_N	H32	STACK_LA11_N
LA18_P_CC	C22	STACK_LA01_P_CC	LA28_P	H31	STACK_LA11_P
LA19_N	H23	STACK_LA02_N	LA29_N	G31	STACK_LA12_N
LA19_P	H22	STACK_LA02_P	LA29_P	G30	STACK_LA12_P
LA20_N	G22	STACK_LA03_N	LA30_N	H35	STACK_LA13_N
LA20_P	G21	STACK_LA03_P	LA30_P	H34	STACK_LA13_P
LA21_N	H26	STACK_LA04_N	LA31_N	G34	STACK_LA14_N
LA21_P	H25	STACK_LA04_P	LA31_P	G33	STACK_LA14_P
LA22_N	G25	STACK_LA05_N	LA32_N	H38	STACK_LA15_N
LA22_P	G24	STACK_LA05_P	LA32_P	H37	STACK_LA15_P
LA23_N	D24	STACK_LA06_N	LA33_N	G37	STACK_LA16_N
LA23_P	D23	STACK_LA06_P	LA33_P	G36	STACK_LA16_P
LA24_N	H29	STACK_LA07_N	SCL	C30	SCL
LA24_P	H28	STACK_LA07_P	SDA	C31	SDA

All net names ending with P or N are differential pairs with 100 ohm impedance and <1 mm length difference within the pair. The skew between differential pairs remains within 5 mm. The CC1-4, TC and TFG signals are LVCMOS based on the VADJ voltage level. The SCL and SDA signal are 3V3 signals.

Appendix B: FMC stack connector ICD

Connector vendor : Samtec

Connector part number: ASP-134486-01

AV57	Con. Pin	Net name	AV57	Con. Pin	Net name
CLK0_M2C_N	H5	STACK_CLK0_M2C_N	DP8_M2C_P	B8	STACK_DP8_M2C_P
CLK0_M2C_P	H4	STACK_CLK0_M2C_P	DP9_C2M_N	B25	STACK_DP9_C2M_N
CLK1_M2C_N	G3	STACK_CLK1_M2C_N	DP9_C2M_P	B24	STACK_DP9_C2M_P
CLK1_M2C_P	G2	STACK_CLK1_M2C_P	DP9_M2C_N	B5	STACK_DP9_M2C_N
CLK2_BIDIR_N	K5	n.c.	DP9_M2C_P	B4	STACK_DP9_M2C_P
CLK2_BIDIR_P	K4	n.c.	GBTCLK0_M2C_N	D5	STACK_GBTCLK0_M2C_N
CLK3_BIDIR_N	J3	n.c.	GBTCLK0_M2C_P	D4	STACK_GBTCLK0_M2C_P
CLK3_BIDIR_P	J2	n.c.	GBTCLK1_M2C_N	B21	STACK_GBTCLK1_M2C_N
DP0_C2M_N	C3	STACK_DP0_C2M_N	GBTCLK1_M2C_P	B20	STACK_GBTCLK1_M2C_p
DP0_C2M_P	C2	STACK_DP0_C2M_P	HA00_N_CC	F5	STACK_HA00_N_CC
DP0_M2C_N	C7	STACK_DP0_M2C_N	HA00_P_CC	F4	STACK_HA00_P_CC
DP0_M2C_P	C6	STACK_DP0_M2C_P	HA01_N_CC	E3	STACK_HA01_N_CC
DP1_C2M_N	A23	STACK_DP1_C2M_N	HA01_P_CC	E2	STACK_HA01_P_CC
DP1_C2M_P	A22	STACK_DP1_C2M_P	HA02_N	K8	n.c.
DP1_M2C_N	A3	STACK_DP1_M2C_N	HA02_P	K7	n.c.
DP1_M2C_P	A2	STACK_DP1_M2C_P	HA03_N	J7	n.c.
DP2_C2M_N	A27	STACK_DP2_C2M_N	HA03_P	J6	n.c.
DP2_C2M_P	A26	STACK_DP2_C2M_P	HA04_N	F8	n.c.
DP2_M2C_N	A7	STACK_DP2_M2C_N	HA04_P	F7	n.c.
DP2_M2C_P	A6	STACK_DP2_M2C_P	HA05_N	E7	n.c.
DP3_C2M_N	A31	STACK_DP3_C2M_N	HA05_P	E6	n.c.
DP3_C2M_P	A30	STACK_DP3_C2M_P	HA06_N	K11	n.c.
DP3_M2C_N	A11	STACK_DP3_M2C_N	HA06_P	K10	n.c.
DP3_M2C_P	A10	STACK_DP3_M2C_P	HA07_N	J10	n.c.
DP4_C2M_N	A35	STACK_DP4_C2M_N	HA07_P	J9	n.c.
DP4_C2M_P	A34	STACK_DP4_C2M_P	HA08_N	F11	n.c.
DP4_M2C_N	A15	STACK_DP4_M2C_N	HA08_P	F10	n.c.
DP4_M2C_P	A14	STACK_DP4_M2C_P	HA09_N	E10	n.c.
DP5_C2M_N	A39	STACK_DP5_C2M_N	HA09_P	E9	n.c.
DP5_C2M_P	A38	STACK_DP5_C2M_P	HA10_N	K14	n.c.
DP5_M2C_N	A19	STACK_DP5_M2C_N	HA10_P	K13	n.c.
DP5_M2C_P	A18	STACK_DP5_M2C_P	HA11_N	J13	n.c.
DP6_C2M_N	B37	STACK_DP6_C2M_N	HA11_P	J12	n.c.
DP6_C2M_P	B36	STACK_DP6_C2M_P	HA12_N	F14	n.c.
DP6_M2C_N	B17	STACK_DP6_M2C_N	HA12_P	F13	n.c.
DP6_M2C_P	B16	STACK_DP6_M2C_P	HA13_N	E13	n.c.
DP7_C2M_N	B33	STACK_DP7_C2M_N	HA13_P	E12	n.c.
DP7_C2M_P	B32	STACK_DP7_C2M_P	HA14_N	J16	n.c.
DP7_M2C_N	B13	STACK_DP7_M2C_N	HA14_P	J15	n.c.

DP7_M2C_P	B12	STACK_DP7_M2C_P	HA15_N	F17	n.c.
DP8_C2M_N	B29	STACK_DP8_C2M_N	HA15_P	F16	n.c.
DP8_C2M_P	B28	STACK_DP8_C2M_P	HA16_N	E16	n.c.
DP8_M2C_N	B9	STACK_DP8_M2C_N	HA16_P	E15	n.c.
HA17_N_CC	K17	n.c.	HB15_N	J34	n.c.
HA17_P_CC	K16	n.c.	HB15_P	J33	n.c.
HA18_N	J19	n.c.	HB16_N	F35	n.c.
HA18_P	J18	n.c.	HB16_P	F34	n.c.
HA19_N	F20	n.c.	HB17_N_CC	K38	n.c.
HA19_P	F19	n.c.	HB17_P_CC	K37	n.c.
HA20_N	E19	n.c.	HB18_N	J37	n.c.
HA20_P	E18	n.c.	HB18_P	J36	n.c.
HA21_N	K20	n.c.	HB19_N	E34	n.c.
HA21_P	K19	n.c.	HB19_P	E33	n.c.
HA22_N	J22	n.c.	HB20_N	F38	n.c.
HA22_P	J21	n.c.	HB20_P	F37	n.c.
HA23_N	K23	n.c.	HB21_N	E37	n.c.
HA23_P	K22	n.c.	HB21_P	E36	n.c.
HB00_N_CC	K26	n.c.	LA00_N_CC	G7	STACK_LA00_N_CC
HB00_P_CC	K25	n.c.	LA00_P_CC	G6	STACK_LA00_P_CC
HB01_N	J25	n.c.	LA01_N_CC	D9	STACK_LA01_N_CC
HB01_P	J24	n.c.	LA01_P_CC	D8	STACK_LA01_P_CC
HB02_N	F23	n.c.	LA02_N	H8	STACK_LA02_N
HB02_P	F22	n.c.	LA02_P	H7	STACK_LA02_P
HB03_N	E22	n.c.	LA03_N	G10	STACK_LA03_N
HB03_P	E21	n.c.	LA03_P	G9	STACK_LA03_P
HB04_N	F26	n.c.	LA04_N	H11	STACK_LA04_N
HB04_P	F25	n.c.	LA04_P	H10	STACK_LA04_P
HB05_N	E25	n.c.	LA05_N	D12	STACK_LA05_N
HB05_P	E24	n.c.	LA05_P	D11	STACK_LA05_P
HB06_N_CC	K29	n.c.	LA06_N	C11	STACK_LA06_N
HB06_P_CC	K28	n.c.	LA06_P	C10	STACK_LA06_P
HB07_N	J28	n.c.	LA07_N	H14	STACK_LA07_N
HB07_P	J27	n.c.	LA07_P	H13	STACK_LA07_P
HB08_N	F29	n.c.	LA08_N	G13	STACK_LA08_N
HB08_P	F28	n.c.	LA08_P	G12	STACK_LA08_P
HB09_N	E28	n.c.	LA09_N	D15	STACK_LA09_N
HB09_P	E27	n.c.	LA09_P	D14	STACK_LA09_P
HB10_N	K32	n.c.	LA10_N	C15	STACK_LA10_N
HB10_P	K31	n.c.	LA10_P	C14	STACK_LA10_P
HB11_N	J31	n.c.	LA11_N	H17	STACK_LA11_N
HB11_P	J30	n.c.	LA11_P	H16	STACK_LA11_P
HB12_N	F32	n.c.	LA12_N	G16	STACK_LA12_N
HB12_P	F31	n.c.	LA12_P	G15	STACK_LA12_P
HB13_N	E31	n.c.	LA13_N	D18	STACK_LA13_N

HB13_P	E30	n.c.	LA13_P	D17	STACK_LA13_P
HB14_N	K35	n.c.	LA14_N	C19	STACK_LA14_N
HB14_P	K34	n.c.	LA14_P	C18	STACK_LA14_P
LA15_N	H20	STACK_LA15_N	LA25_N	G28	n.c.
LA15_P	H19	STACK_LA15_P	LA25_P	G27	n.c.
LA16_N	G19	STACK_LA16_N	LA26_N	D27	n.c.
LA16_P	G18	STACK_LA16_P	LA26_P	D26	n.c.
LA17_N_CC	D21	n.c.	LA27_N	C27	n.c.
LA17_P_CC	D20	n.c.	LA27_P	C26	n.c.
LA18_N_CC	C23	n.c.	LA28_N	H32	n.c.
LA18_P_CC	C22	n.c.	LA28_P	H31	n.c.
LA19_N	H23	n.c.	LA29_N	G31	n.c.
LA19_P	H22	n.c.	LA29_P	G30	n.c.
LA20_N	G22	n.c.	LA30_N	H35	n.c.
LA20_P	G21	n.c.	LA30_P	H34	n.c.
LA21_N	H26	n.c.	LA31_N	G34	n.c.
LA21_P	H25	n.c.	LA31_P	G33	n.c.
LA22_N	G25	n.c.	LA32_N	H38	n.c.
LA22_P	G24	n.c.	LA32_P	H37	n.c.
LA23_N	D24	n.c.	LA33_N	G37	n.c.
LA23_P	D23	n.c.	LA33_P	G36	n.c.
LA24_N	H29	n.c.	SCL	C30	STACK_SCL
LA24_P	H28	n.c.	SDA	C31	STACK_SDA

All net names ending with P or N are differential pairs with 100 ohm impedance and <1 mm length difference within the pair. The skew between differential pairs remains within 5 mm. The CC1-4, TC and TFG signals are LVCMOS based on the VADJ voltage level. The SCL and SDA signal are 3V3 signals.

Appendix C: SDR ICD for base/medium/full

This is the Cameralink ICD in case the board is configured as base/medium/full (LXD40K0)

Connector supplier: 3M

Connector part number: 12226-5100-00FR

QTY 2 Jack screws part number: 12600-S-10

Connector P1 and P2

cable name P1	Base (P1 connector pin)	Net name P1	Direction P1	Cable Name P2	Medium/Full/ (P2 connector pin)	Net name P2	Direcion P2
Inner Shield	1	P1_SHIELD	n.a.	Inner Shield	1	P2_SHIELD	n.a.
Inner Shield	14	P1_SHIELD	n.a.	Inner Shield	14	P2_SHIELD	n.a.
PAIR1-	25	P1_X0_N	out	PAIR1-	25	P2_Y0_N	out
PAIR1+	12	P1_X0_P	out	PAIR1+	12	P2_Y0_P	out
PAIR2-	24	P1_X1_N	out	PAIR2-	24	P2_Y1_N	out
PAIR2+	11	P1_X1_P	out	PAIR2+	11	P2_Y1_P	out
PAIR3-	23	P1_X2_N	out	PAIR3-	23	P2_Y2_N	out
PAIR3+	10	P1_X2_P	out	PAIR3+	10	P2_Y2_P	out
PAIR4-	22	P1_XCLK_N	out	PAIR4-	22	P2_YCLK_N	out
PAIR4+	9	P1_XCLK_P	out	PAIR4+	9	P2_YCLK_P	out
PAIR5-	21	P1_X3_N	out	PAIR5-	21	P2_Y3_N	out
PAIR5+	8	P1_X3_P	out	PAIR5+	8	P2_Y3_P	out
PAIR6+	20	P1_SERTC_P	out	PAIR6+	20	100 Ω	n.a.
PAIR6-	7	P1_SERTC_N	out	PAIR6-	7	terminated	n.a.
PAIR7-	19	P1_SERTFG_N	in	PAIR7-	19	P2_Z0_N	out
PAIR7+	6	P1_SERTFG_P	in	PAIR7+	6	P2_Z0_P	out
PAIR8-	18	P1_CC1_N	out	PAIR8-	18	P2_Z1_N	out
PAIR8+	5	P1_CC1_P	out	PAIR8+	5	P2_Z1_P	out
PAIR9+	17	P1_CC2_P	out	PAIR9+	17	P2_Z2_N	out
PAIR9-	4	P1_CC2_N	out	PAIR9-	4	P2_Z2_P	out
PAIR10-	16	P1_CC3_N	out	PAIR10-	16	P2_ZCLK_N	out
PAIR10+	3	P1_CC3_P	out	PAIR10+	3	P2_ZCLK_P	out
PAIR11+	15	P1_CC4_P	out	PAIR11+	15	P2_Z3_N	out
PAIR11-	2	P1_CC4_N	out	PAIR11-	2	P2_Z3_P	out
Inner Shield	13	P1_SHIELD	n.a.	Inner Shield	13	P2_SHIELD	n.a.
Inner Shield	26	P1_SHIELD	n.a.	Inner Shield	26	P2_SHIELD	n.a.

All net names ending with P or N are LVDS signals and are routed as differential pairs with 100 ohm impedance and <1 mm length difference within the pair. The skew between differential pairs should remains within 5 mm

P1_SHIELD connects to ISO_GND through a capacitor in parallel with a 10M-ohm resistor

P2_SHIELD connects to ISO_GND through a capacitor in parallel with a 10M-ohm resistor

Inner Shield connects to ISO_GND through a 0 ohm resistor.

Appendix D: SDR ICD for dual base

This is the CameraLink ICD in case the board is configured as dual base (LXD40K1)

Connector supplier: 3M

Connector part number: 12226-5100-00FR

QTY 2 Jack screws part number: 12600-S-10

Connector P1 and P2

cable name P1	Base (P1 connector pin)	Net name P1	Direction P1	Cable Name P2	Medium/Full/ (P2 connector pin)	Net name P2	Direction P2
Inner Shield	1	P1_SHIELD	n.a.	Inner Shield	1	P2_SHIELD	n.a.
Inner Shield	14	P1_SHIELD	n.a.	Inner Shield	14	P2_SHIELD	n.a.
PAIR1-	25	P1_X0_N	out	PAIR1-	25	P2_X0_N	out
PAIR1+	12	P1_X0_P	out	PAIR1+	12	P2_X0_P	out
PAIR2-	24	P1_X1_N	out	PAIR2-	24	P2_X1_N	out
PAIR2+	11	P1_X1_P	out	PAIR2+	11	P2_X1_P	out
PAIR3-	23	P1_X2_N	out	PAIR3-	23	P2_X2_N	out
PAIR3+	10	P1_X2_P	out	PAIR3+	10	P2_X2_P	out
PAIR4-	22	P1_XCLK_N	out	PAIR4-	22	P2_XCLK_N	out
PAIR4+	9	P1_XCLK_P	out	PAIR4+	9	P2_XCLK_P	out
PAIR5-	21	P1_X3_N	out	PAIR5-	21	P2_X3_N	out
PAIR5+	8	P1_X3_P	out	PAIR5+	8	P2_X3_P	out
PAIR6+	20	P1_SERTC_P	out	PAIR6+	20	P2_SERTC_P	out
PAIR6-	7	P1_SERTC_N	Out	PAIR6-	7	P2_SERTC_N	out
PAIR7-	19	P1_SERTFG_N	In	PAIR7-	19	P2_SERTFG_N	In
PAIR7+	6	P1_SERTFG_P	In	PAIR7+	6	P2_SERTFG_P	In
PAIR8-	18	P1_CC1_N	out	PAIR8-	18	P2_CC1_N	out
PAIR8+	5	P1_CC1_P	out	PAIR8+	5	P2_CC1_P	out
PAIR9+	17	P1_CC2_P	out	PAIR9+	17	P2_CC2_P	out
PAIR9-	4	P1_CC2_N	out	PAIR9-	4	P2_CC2_N	out
PAIR10-	16	P1_CC3_N	out	PAIR10-	16	P2_CC3_N	out
PAIR10+	3	P1_CC3_P	out	PAIR10+	3	P2_CC3_P	out
PAIR11+	15	P1_CC4_P	out	PAIR11+	15	P2_CC4_P	out
PAIR11-	2	P1_CC4_N	out	PAIR11-	2	P2_CC4_N	out
Inner Shield	13	P1_SHIELD	n.a.	Inner Shield	13	P2_SHIELD	n.a.
Inner Shield	26	P1_SHIELD	n.a.	Inner Shield	26	P2_SHIELD	n.a.

All net names ending with P or N are LVDS signals and are routed as differential pairs with 100 ohm impedance and <1 mm length difference within the pair. The skew between differential pairs should remain within 5 mm

P1_SHIELD connects to ISO_GND through a capacitor in parallel with a 10M-ohm resistor

P2_SHIELD connects to ISO_GND through a capacitor in parallel with a 10M-ohm resistor

Inner Shield connects to ISO_GND through a 0 ohm resistor.

APPENDIX E: FMC carrier board compatibility chart

Table 4: LXF90K0 FMC compatibility

FMC Connector /site	LX40K0 Base/medium/Full	LXD40K1 Dual Base	LXD40K2 Dual medium Dual Base/Medium/Full	LXD40K4 Quad Base
FMC	Compatible	Compatible	Compatible	Compatible

Table 5: KCU105 FMC compatibility

FMC Connector /site	LX40K0 Base/medium/Full	LXD40K1 Dual Base	LXD40K2 Dual medium Dual Base/Medium/Full	LXD40K4 Quad Base
FMC LPC	Compatible No Z_CLK	Compatible No CC[3:4] on the stack	Compatible No Z_CLK on both main and stack	Partially Tripple Base only
FMC HPC	Compatible	Compatible	Compatible	Compatible

Table 6: TEB0911 FMC compatibility

FMC Connector /site	LX40K0 Base/medium/Full	LXD40K1 Dual Base	LXD40K2 Dual medium Dual Base/Medium/Full	LXD40K4 Quad Base
J4 / FMC B	Not supported	Not supported	Not supported	Not supported
J8 / FMC C	Not supported	Not supported	Not supported	Not supported
J7 / FMC D	Compatible No Z_CLK	Compatible No CC[3:4]	Compatible No Z_CLK on both main and stack	Partially Tripple Base only
J6 / FMC E	Compatible No Z_CLK	Compatible No CC[3:4]	Compatible No Z_CLK on both main and stack	Partially Tripple Base only
J10 / FMC A	Not supported	Not supported	Not supported	Not supported
J21 / FMC F	Not supported	Not supported	Not supported	Not supported

Appendix F: LXD40K0 to/from LXD40K1 conversion

To convert from LXD40K0 to LXD40K1 make the following modifications:

- 1) Remove: R7, R8, R11, R12, R15, R17, R20, R21, R24, R25, R16
- 2) PLACE: R5, R6, R9, R10, R13, R14, R18, R19, R22, R23, R26, R27

To convert from LXD40K1 to LXD40K0 make the following modifications:

- 1) Remove: R5, R6, R9, R10, R13, R14, R18, R19, R22, R23, R26, R27
- 2) PLACE: R7, R8, R11, R12, R15, R17, R20, R21, R24, R25, R16

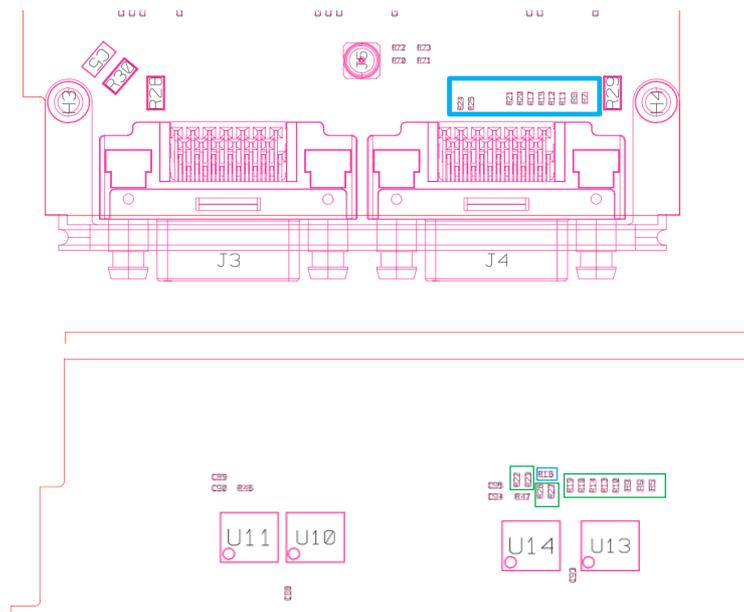


Figure 15: LXD40K0 to/from LXD40K1 conversion resistor locations

Appendix G: MMCX IO build options

There is a build option for an isolated MMCX input or output at the cost of reduced CameraLink functionality. For the input you will either lose SERTFG on the second CameraLink port (LXD40K1) or the Z channel (LXD40K0). For the output option you will lose the SERTC on the second CameraLink port (LXD40K1), for the LXD40K0 build there is no impact.

Table 7: MMCX IO build options

MMCX IO option	R70	R71	R72	R73
NO IO (default)	Do not place	Place	Do not place	Place
INPUT	Place	Do not place	Do not place	Place
OUTPUT	Do not place	Place	Place	Do not place

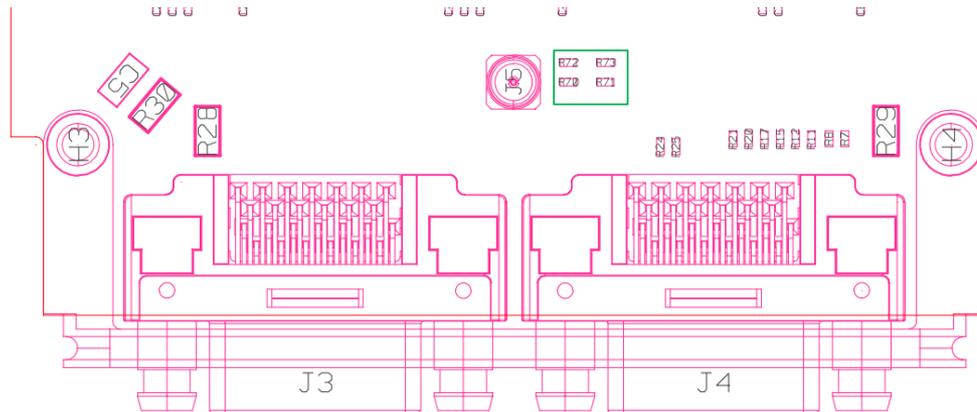


Figure 16: MMCX IO resistor locations.

Appendix H: LXD40K2/LXD40K4 assembly instructions

It is possible to directly stack the two FMC boards together if you remove the bezels. For a more modular solution we offer the LXD40K2 and LXD40K4. The LXD40K2/LXD40K4 assembly is a stack of two LXD40K0/LXD40K1 boards respectively. To provide proper clearance at the front panel we use a VITA 57.1 FMC EXTENDER CARD. The following image shows the assembly drawing and required components to create the stack. If an order is placed at Logic-X for the LXD40K2 or LXD40K4 you will receive a pre-assembled stack.

The assembly steps are (Perform steps on both sides of the stack):

- 1) Attach A to the MAIN FMC using B. Apply a small drop of thread locker in A before assembly
- 2) Attach D to MAIN FMC using B. Apply a small drop of thread locker in A before assembly
- 3) Attach C to MAIN FMC. Apply a small drop of thread locker in A before assembly
- 4) Attach STACKED FMC to D using F and G. Apply a small drop of thread locker in A before assembly

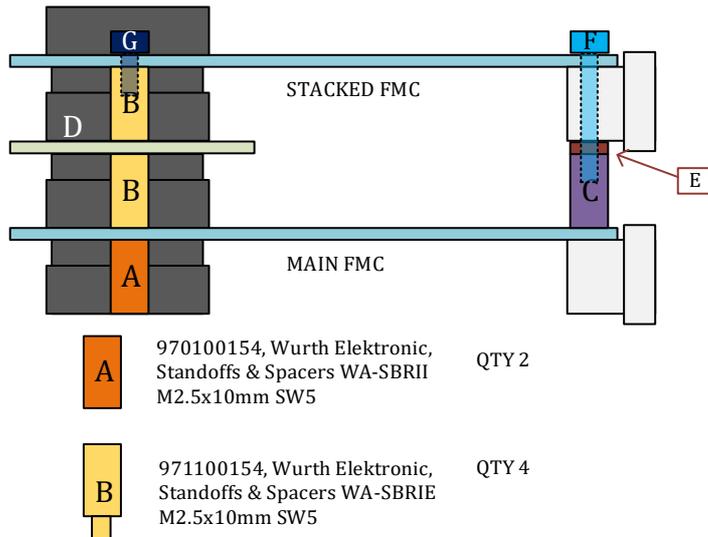


Figure 17: LXD40K2/LXD40K4 assembly drawing.

Appendix I: Revision history

Document Revision	Changes			Quality Approval	Date
R1.0	First release			EBA	October 7, 2025
R1.1	Added appendices with rework and assembly instructions			EBA	October 17, 2025
R1.2	Updated the MMCX option description and updated some block diagrams to match the final layout			EBA	February 25, 2026