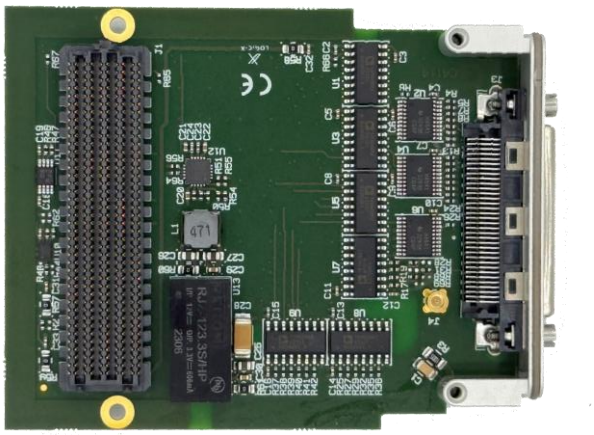
LXD41K0 - LVCMOS IO

Featuring Galvanic Isolation Between I/O and FMC Connector



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LOGIC-X

THE POWER OF LOGIC

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1 General Description

The LXD41K0 FMC (FPGA Mezzanine Card) is designed to support 16-bit input and 16-bit output digital interface, a clock output and a trigger input and output channel with galvanic isolation, ensuring electrical separation between the I/O and the FMC connector. This provides the user with a total of 18 digital outputs and 17 digital inputs via an industry standard VHDCI 68-pin Connector. The IO standard is 3V3 LVCMOS.

This product is part of the Logic-X stackable FMC product line, which enables flexible configurations. An optional FMC stack connector at the bottom of the board enables versatile configurations. Specifically, the lower LA[16:0] signals from the stack connector are routed to the LA[33:17] signals of the FMC connector at the top of the board, allowing two LXD41K0 modules to stack, creating two digital input /output ports on one LPC site. Alternatively, you can also mix other FMC boards that only require the LA[16:0] signals. As a built option it is possible to add a total of 16 additional input signals.

The PCB design is divided into two isolated sections, providing isolation between the front panel and the FMC connector. This design enhances signal integrity and electromagnetic compatibility (EMC), offering a robust and reliable isolated interface for demanding digital IO.

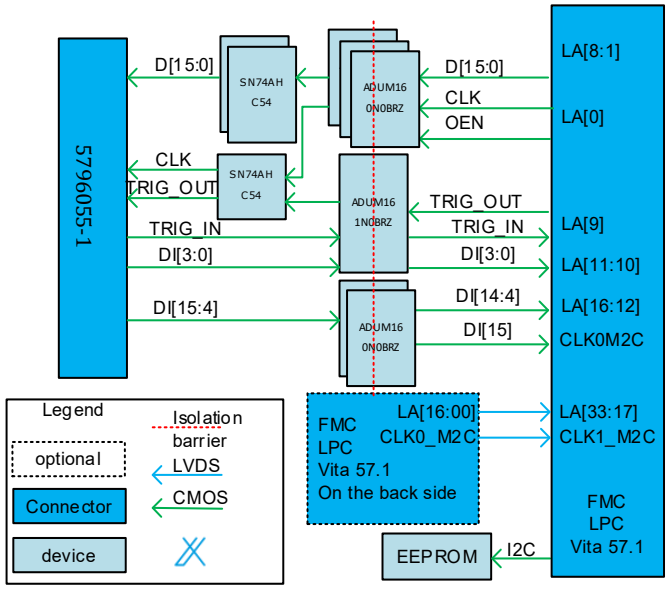

Figure 1: LXD41K0 block diagram

2 Mechanical design

The board design is mechanically compliant with the VITA 57.1 (FMC) specification, with one exception: the top-side isolated power supply exceeds the specified 4.7 mm maximum height by approximately 2.8 mm.
According to the VITA 57.1 standard, the maximum component height is 1.3 mm on the bottom side and 4.7 mm on the top side of the board. This design maintains compliance with all other mechanical requirements and targets the conduction-cooled FMC format, including Region 1 for the I/O connectors.
The overall board dimensions and the component height exception are illustrated in the image below.

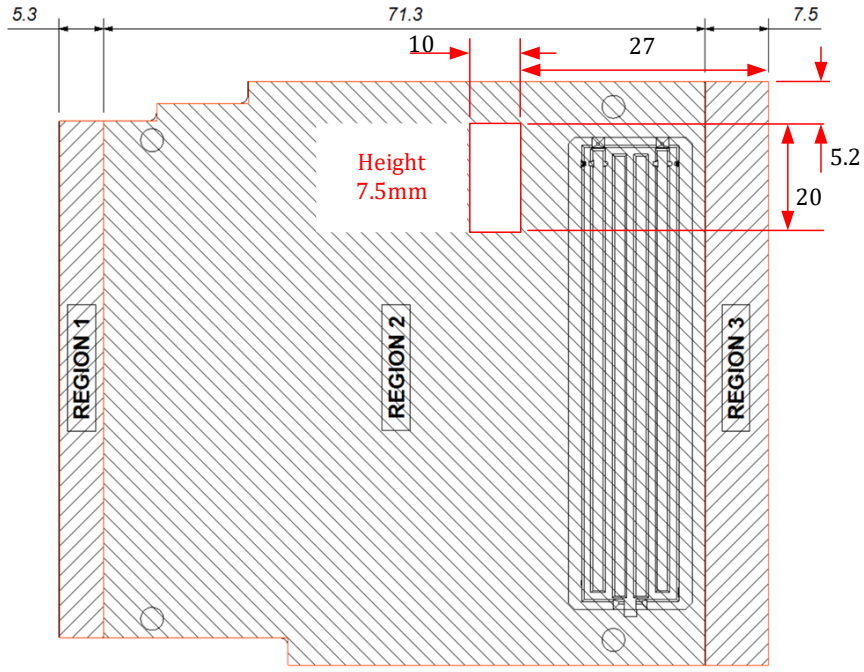

Figure 2:Board mechanical dimensions and component height violation.

2.1 Cooling

To maintain optimal operating temperatures, forced airflow is recommended for cooling.

2.2 Front panel design

The PCB's front panel provides access to the VHDCI 68-pin connector through an opening in a standard FMC bezel as shown in the following figure.

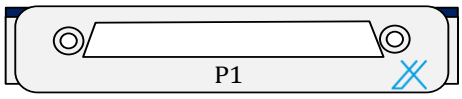

Figure 3: LXD41K0 bezel design

3 Digital IO interface

The product offers a total of 18 digital output signals and 17 digital input signal. All IO signals are galvanically isolated from the FMC connector side. The input signal is 5V TTL compatible and the outputs are 3.3V TTL compatible. There is a build option to swap the TRIGGER_IN and TRIGGER_OUT. The default build option will not swap the signals. The following image shows the design of the digital IO interface. The design includes zero-ohm resistors on all inputs and 33 Ohms resistors on all output signals.

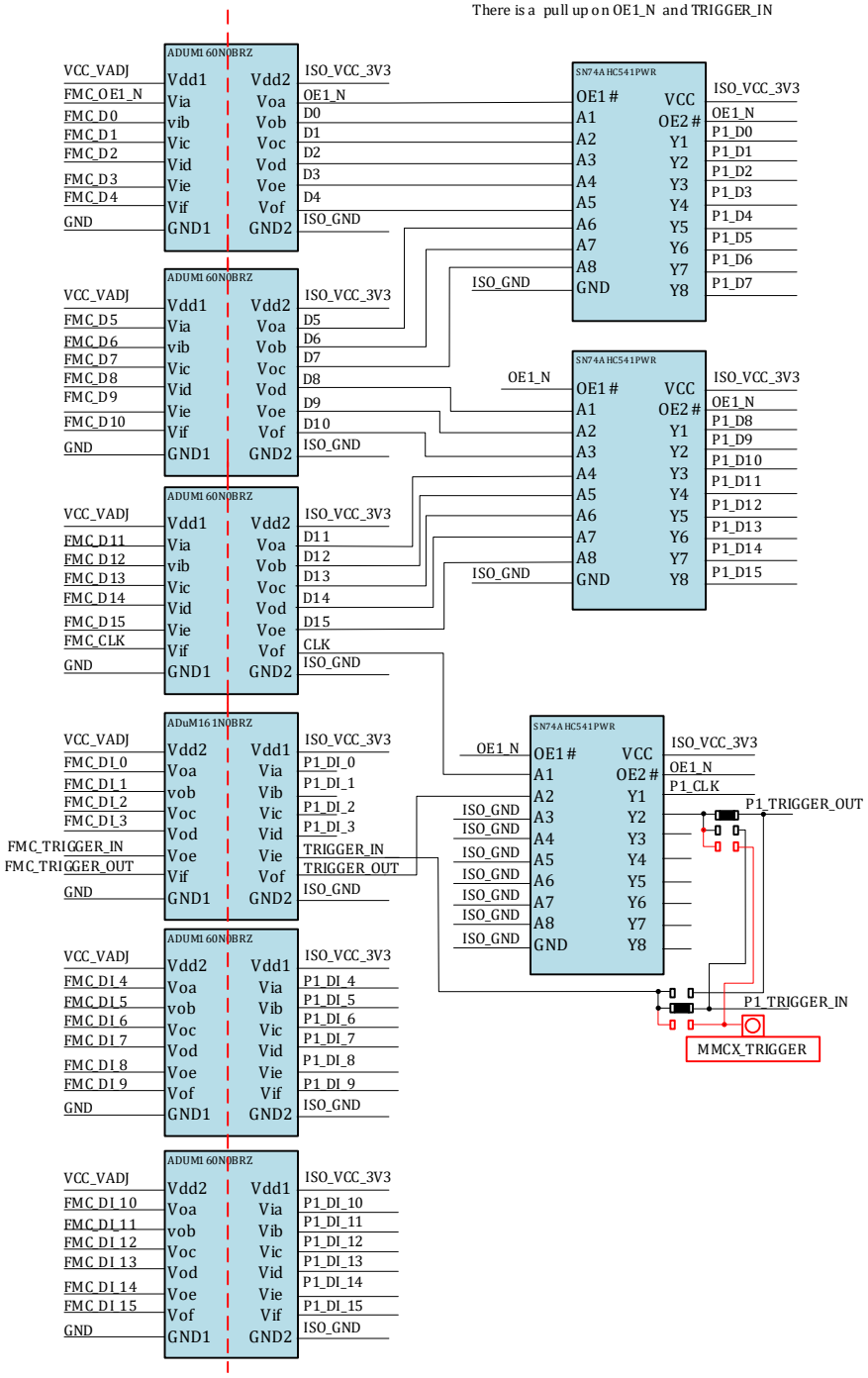

Figure 4: Digital IO interface isolation design

3.1 Digital IO interface front panel connector

The external IO interface is built with the receptacle 5796055-1 from TE Connectivity. It is a through hole component that offers ample of mechanical strength. The 30 µin (microinches) flash gold offers good reliability, and wear resistance. For best EMI performance the connector is attached to the front panel using the 787004-3 jack sockets.

Figure 5: Front panel IO connector 5796055-1

4 Stacked configuration

The LXD41K0 FMC board is part of the Logic-X stackable FMC product line. These products are designed with a build option that allows an additional FMC module to be stacked on the back side of the board. This enables designers to leverage the extra I/O resources available on the carrier board, provided the system can accommodate the additional height introduced by stacking. Within the stackable product line, the following signal routing scheme is implemented between the mezzanine FMC connector and the stack FMC connector:

- LA[33:17], CLK1_M2C on the mezzanine connector are routed to LA[16:0] and CLK0_M2C respectively, on the stack connector.
- All high-speed gigabit transceiver lanes are directly routed from the mezzanine FMC connector to the stack FMC connector.

This architecture provides a flexible and scalable platform, allowing multiple FMC modules to operate in combination while maintaining signal integrity and carrier compatibility.

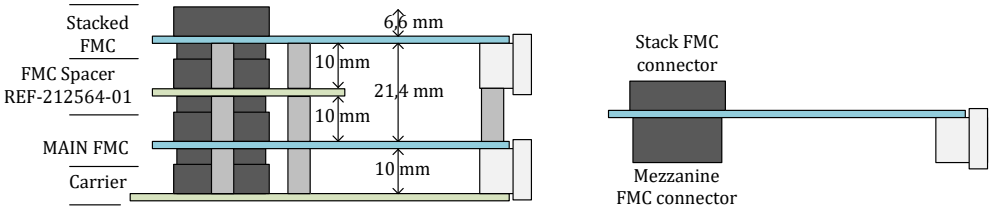

Figure 6: Logic-X stackable FMC concept

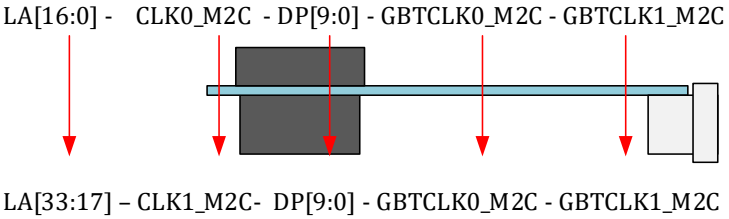

Figure 7: Stack to main signal mapping.

5 MMCX GPIO

As an optional build feature, a signal from an MMCX connector (not part of the front-panel I/O) can be routed to function as either an isolated input or an isolated output.

This MMCX connection is typically linked to the system I/O panel using an MMCX-to-BMC bulkhead cable, providing flexible access to isolated GPIO functionality for system integration or testing purposes.
The build option can route either the TRIGGER_IN or the TRIGGER_OUT to the onboard MMCX header. The respective connection to the front panel connector will be removed to prevent conflicts. The connection from FMC_TRIGGER_IN/OUT to either P1_TRIGGER_IN/OUT or MMCX_TRGGER is done using the resistors, R28, R30, R31, R33, R68 and R69.
The following image shows the locations of these resistors.

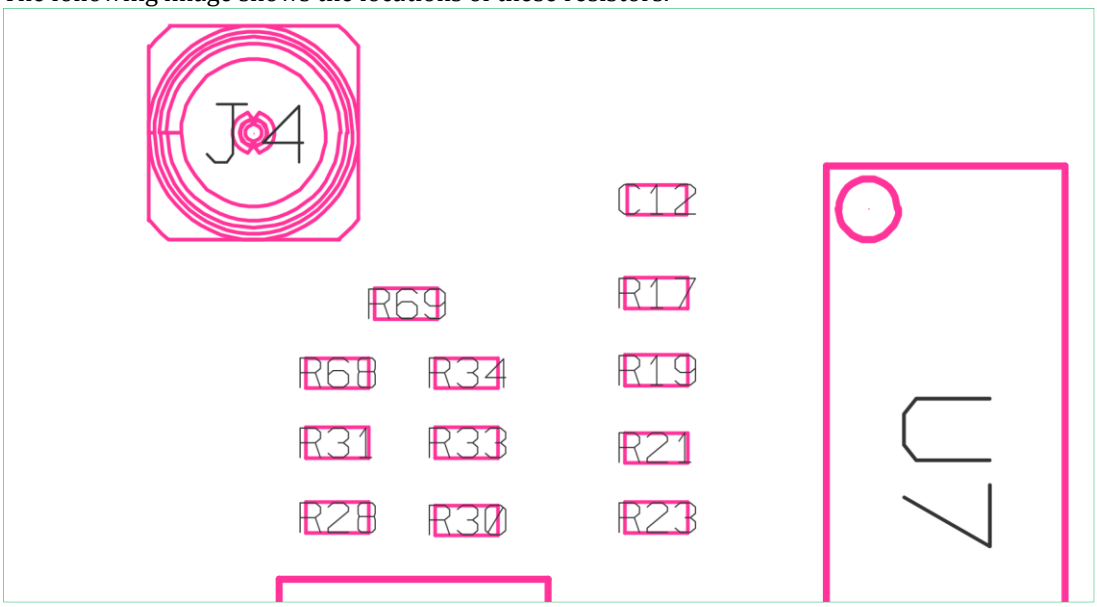

Figure 8: Trigger connection resistors locations.

Table 1: Trigger resistor build options

Option	FMC_TRIGGER_IN	FMC_TRIGGER_OUT	R28	R30	R31	R33	R68	R69
P1_0 (Default)	P1_TRIGGER_OUT	P1_TRIGGER_IN	DNP	Place	Place	DNP	DNP	DNP
P1_1	P1_TRIGGER_IN	P1_TRIGGER_OUT	Place	DNP	DNP	Place	DNP	DNP
MMCX_IN_0	MMCX_TRIGGER	P1_TRIGGER_IN	DNP	Place	DNP	DNP	DNP	Place
MMCX_IN_1	MMCX_TRIGGER	P1_TRIGGER_OUT	Place	DNP	DNP	DNP	DNP	Place
MMCX_OUT_0	P1_TRIGGER_OUT	MMCX_TRIGGER	DNP	DNP	Place	DNP	Place	DNP
MMCX_OUT_1	P1_TRIGGER_IN	MMCX_TRIGGER	DNP	DNP	DNP	Place	Place	DNP

6 FMC interface

The LXD41K0 is an FMC card designed for use with a Low Pin Count (LPC) connector.
For standard operation, the module functions as a Low Pin Count FMC, utilizing the following signals:

- LA[16:0]
- CLK0_M2C

For stacked configurations (two LXD41K0 modules or another FMC module on the stack), additional signals are required:

- CLK1_M2C
- LA[33:17]

To enable stacking with a board that employs multi-gigabit transceivers, the LXD41K0 also routes all DP_C2M and DP_M2C signals directly between the two FMC connectors.
This provides full high-speed signal continuity for stackable designs.

6.1 Utility connections

The following table summarizes how the utility connection signals are implemented on the LXD41K0.

Table 2: FMC utility connections

Signal name	Connected to
PRSNT_M2C	Tied to GND
PG_C2M	Used to enable local power supplies
TCK	Not used
TDI	connected to TDO
TDO	connected to TDI
SCL	See chapter on I2C
SDA	See chapter on I2C
TMS	Not used
TRST_L	Not used
GA0	See chapter on I2C
GA1	See chapter on I2C
RES0	Not used
PG_M2C	Asserted when the carrier asserts PG_C2M and the local power goods are asserted

6.2 Gigabit transceiver connections

The LXD41K0 routes all Gigabit transceiver connections directly to the stack connector, ensuring full high-speed signal continuity between stacked modules.

6.3 I/O Standard Support

Most signal connections to the FMC connector on the LXD41K0 are differential LVDS signals. The LVCMOS control signals are passed through level translators powered by the VADJ rail on the FMC side. This ensures proper operation across a wide VADJ voltage range from 1.2 V to 3.3 V, providing compatibility with a broad range of carrier board designs.

6.4 VIO_B_M2C Support

The LXD41K0 connects VIO_B_M2C directly to VADJ.

6.5 VREF Support

The VREF_A_M2C and VREF_B_M2C signals are left unconnected on the LXD41K0.

7 I2C Interface

The LXD41K0 includes an FMC identification EEPROM that is connected directly to the FMC I^2C bus and remains active with only the 3V3_AUX supply.

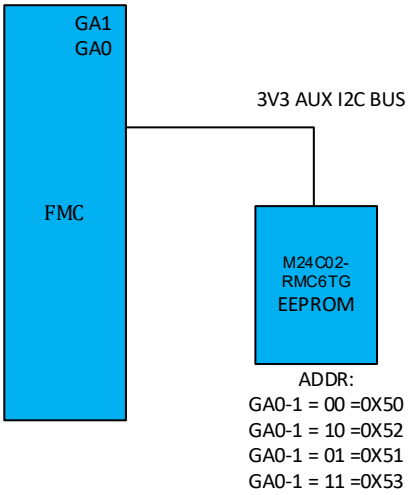

Figure 9:I2C schematic

8 JTAG

The LXD41K0 does not participate in the JTAG chain. Instead, the TDI signal is looped back to the TDO signal on the board, maintaining JTAG continuity through the FMC connector.

9 Power Design

An FMC module receives multiple supply voltages from the FMC connector, namely +12 V, +3.3 V, VADJ, and +3.3 V_AUX. The LXD41K0 utilizes all four supply rails to power its isolated interfaces and logic circuitry. The table below summarizes the typical power consumption and current draw of the LXD41K0 for each voltage rail:

Table 3: Power consumption

Voltage Rail	Maximum Available by FMC specification(A)	Typical Current (A)	Typical Power (Watts)
VADJ	4	0.02	0,04 @ 1.8V
3P3V	3	0.4	1.32
12P0V	1	0.14	1.77
3P3VAUX (Operating) 3P3VAUX (Standby)	0.020 0.000001	0.010 0.000001	0.033 0.0000033

The power tree is depicted in the following image.

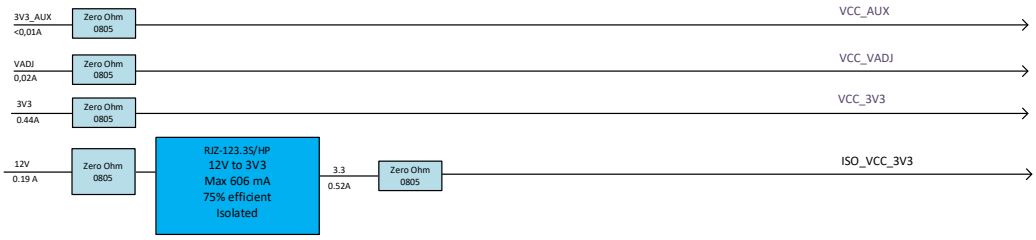

Figure 10: Power tree

10 Ordering options

Ordering code	Description	Can be used as main in FMC stack	Can be used as stacked in FMC stack
LXD41K0	LVCMOS IO.	NO	YES
LXD41K0-S	LVCMOS IO with stack connector.	YES	YES

Appendix A: FMC mezzanine connector ICD

Connector vendor : Samtec
Connector part number: ASP-134488-01

AV57	Con. Pin	Net name	AV57	Con. Pin	Net name
CLK0_M2C_N	H5	FMC_DI_14	DP8_M2C_P	B8	STACK_DP8_M2C_P
CLK0_M2C_P	H4	FMC_DI_15	DP9_C2M_N	B25	STACK_DP9_C2M_N
CLK1_M2C_N	G3	STACK_CLK0_M2C_N	DP9_C2M_P	B24	STACK_DP9_C2M_P
CLK1_M2C_P	G2	STACK_CLK0_M2C_P	DP9_M2C_N	B5	STACK_DP9_M2C_N
CLK2_BIDIR_N	K5	n.c.	DP9_M2C_P	B4	STACK_DP9_M2C_P
CLK2_BIDIR_P	K4	n.c.	GBTCLK0_M2C_N	D5	STACK_GBTCLK0_M2C_N
CLK3_BIDIR_N	J3	n.c.	GBTCLK0_M2C_P	D4	STACK_GBTCLK0_M2C_P
CLK3_BIDIR_P	J2	n.c.	GBTCLK1_M2C_N	B21	STACK_GBTCLK1_M2C_N
DP0_C2M_N	C3	STACK_DP0_C2M_N	GBTCLK1_M2C_P	B20	STACK_GBTCLK1_M2C_p
DP0_C2M_P	C2	STACK_DP0_C2M_P	HA00_N_CC	F5	n.c.
DP0_M2C_N	C7	STACK_DP0_M2C_N	HA00_P_CC	F4	n.c.
DP0_M2C_P	C6	STACK_DP0_M2C_P	HA01_N_CC	E3	n.c.
DP1_C2M_N	A23	STACK_DP1_C2M_N	HA01_P_CC	E2	n.c.
DP1_C2M_P	A22	STACK_DP1_C2M_P	HA02_N	K8	n.c.
DP1_M2C_N	A3	STACK_DP1_M2C_N	HA02_P	K7	n.c.
DP1_M2C_P	A2	STACK_DP1_M2C_P	HA03_N	J7	n.c.
DP2_C2M_N	A27	STACK_DP2_C2M_N	HA03_P	J6	n.c.
DP2_C2M_P	A26	STACK_DP2_C2M_P	HA04_N	F8	n.c.
DP2_M2C_N	A7	STACK_DP2_M2C_N	HA04_P	F7	n.c.
DP2_M2C_P	A6	STACK_DP2_M2C_P	HA05_N	E7	n.c.
DP3_C2M_N	A31	STACK_DP3_C2M_N	HA05_P	E6	n.c.
DP3_C2M_P	A30	STACK_DP3_C2M_P	HA06_N	K11	n.c.
DP3_M2C_N	A11	STACK_DP3_M2C_N	HA06_P	K10	n.c.
DP3_M2C_P	A10	STACK_DP3_M2C_P	HA07_N	J10	n.c.
DP4_C2M_N	A35	STACK_DP4_C2M_N	HA07_P	J9	n.c.
DP4_C2M_P	A34	STACK_DP4_C2M_P	HA08_N	F11	n.c.
DP4_M2C_N	A15	STACK_DP4_M2C_N	HA08_P	F10	n.c.
DP4_M2C_P	A14	STACK_DP4_M2C_P	HA09_N	E10	n.c.
DP5_C2M_N	A39	STACK_DP5_C2M_N	HA09_P	E9	n.c.
DP5_C2M_P	A38	STACK_DP5_C2M_P	HA10_N	K14	n.c.
DP5_M2C_N	A19	STACK_DP5_M2C_N	HA10_P	K13	n.c.
DP5_M2C_P	A18	STACK_DP5_M2C_P	HA11_N	J13	n.c.
DP6_C2M_N	B37	STACK_DP6_C2M_N	HA11_P	J12	n.c.
DP6_C2M_P	B36	STACK_DP6_C2M_P	HA12_N	F14	n.c.
DP6_M2C_N	B17	STACK_DP6_M2C_N	HA12_P	F13	n.c.
DP6_M2C_P	B16	STACK_DP6_M2C_P	HA13_N	E13	n.c.
DP7_C2M_N	B33	STACK_DP7_C2M_N	HA13_P	E12	n.c.
DP7_C2M_P	B32	STACK_DP7_C2M_P	HA14_N	J16	n.c.
DP7_M2C_N	B13	STACK_DP7_M2C_N	HA14_P	J15	n.c.
DP7_M2C_P	B12	STACK_DP7_M2C_P	HA15_N	F17	n.c.

DP8_C2M_N	B29	STACK_DP8_C2M_N	HA15_P	F16	n.c.
DP8_C2M_P	B28	STACK_DP8_C2M_P	HA16_N	E16	n.c.
DP8_M2C_N	B9	STACK_DP8_M2C_N	HA16_P	E15	n.c.
HA17_N_CC	K17	n.c.	HB15_N	J34	n.c.
HA17_P_CC	K16	n.c.	HB15_P	J33	n.c.
HA18_N	J19	n.c.	HB16_N	F35	n.c.
HA18_P	J18	n.c.	HB16_P	F34	n.c.
HA19_N	F20	n.c.	HB17_N_CC	K38	n.c.
HA19_P	F19	n.c.	HB17_P_CC	K37	n.c.
HA20_N	E19	n.c.	HB18_N	J37	n.c.
HA20_P	E18	n.c.	HB18_P	J36	n.c.
HA21_N	K20	n.c.	HB19_N	E34	n.c.
HA21_P	K19	n.c.	HB19_P	E33	n.c.
HA22_N	J22	n.c.	HB20_N	F38	n.c.
HA22_P	J21	n.c.	HB20_P	F37	n.c.
HA23_N	K23	n.c.	HB21_N	E37	n.c.
HA23_P	K22	n.c.	HB21_P	E36	n.c.
HB00_N_CC	K26	n.c.	LA00_N_CC	G7	FMC_CLK
HB00_P_CC	K25	n.c.	LA00_P_CC	G6	FMC_OE1_N
HB01_N	J25	n.c.	LA01_N_CC	D9	FMC_D0
HB01_P	J24	n.c.	LA01_P_CC	D8	FMC_D1
HB02_N	F23	n.c.	LA02_N	H8	FMC_D2
HB02_P	F22	n.c.	LA02_P	H7	FMC_D3
HB03_N	E22	n.c.	LA03_N	G10	FMC_D4
HB03_P	E21	n.c.	LA03_P	G9	FMC_D5
HB04_N	F26	n.c.	LA04_N	H11	FMC_D6
HB04_P	F25	n.c.	LA04_P	H10	FMC_D7
HB05_N	E25	n.c.	LA05_N	D12	FMC_D8
HB05_P	E24	n.c.	LA05_P	D11	FMC_D9
HB06_N_CC	K29	n.c.	LA06_N	C11	FMC_D10
HB06_P_CC	K28	n.c.	LA06_P	C10	FMC_D11
HB07_N	J28	n.c.	LA07_N	H14	FMC_D12
HB07_P	J27	n.c.	LA07_P	H13	FMC_D13
HB08_N	F29	n.c.	LA08_N	G13	FMC_D14
HB08_P	F28	n.c.	LA08_P	G12	FMC_D15
HB09_N	E28	n.c.	LA09_N	D15	FMC_TRIGGER_IN
HB09_P	E27	n.c.	LA09_P	D14	FMC_TRIGGER_OUT
HB10_N	K32	n.c.	LA10_N	C15	FMC_DI_0
HB10_P	K31	n.c.	LA10_P	C14	FMC_DI_1
HB11_N	J31	n.c.	LA11_N	H17	FMC_DI_2
HB11_P	J30	n.c.	LA11_P	H16	FMC_DI_3
HB12_N	F32	n.c.	LA12_N	G16	FMC_DI_4
HB12_P	F31	n.c.	LA12_P	G15	FMC_DI_5
HB13_N	E31	n.c.	LA13_N	D18	FMC_DI_6
HB13_P	E30	n.c.	LA13_P	D17	FMC_DI_7

HB14_N	K35	n.c.	LA14_N	C19	FMC_DI_8
HB14_P	K34	n.c.	LA14_P	C18	FMC_DI_9
LA15_N	H20	FMC_DI_10	LA25_N	G28	STACK_LA08_N
LA15_P	H19	FMC_DI_11	LA25_P	G27	STACK_LA08_P
LA16_N	G19	FMC_DI_12	LA26_N	D27	STACK_LA09_N
LA16_P	G18	FMC_DI_13	LA26_P	D26	STACK_LA09_P
LA17_N_CC	D21	STACK_LA00_N_CC	LA27_N	C27	STACK_LA10_N
LA17_P_CC	D20	STACK_LA00_P_CC	LA27_P	C26	STACK_LA10_P
LA18_N_CC	C23	STACK_LA01_N_CC	LA28_N	H32	STACK_LA11_N
LA18_P_CC	C22	STACK_LA01_P_CC	LA28_P	H31	STACK_LA11_P
LA19_N	H23	STACK_LA02_N	LA29_N	G31	STACK_LA12_N
LA19_P	H22	STACK_LA02_P	LA29_P	G30	STACK_LA12_P
LA20_N	G22	STACK_LA03_N	LA30_N	H35	STACK_LA13_N
LA20_P	G21	STACK_LA03_P	LA30_P	H34	STACK_LA13_P
LA21_N	H26	STACK_LA04_N	LA31_N	G34	STACK_LA14_N
LA21_P	H25	STACK_LA04_P	LA31_P	G33	STACK_LA14_P
LA22_N	G25	STACK_LA05_N	LA32_N	H38	STACK_LA15_N
LA22_P	G24	STACK_LA05_P	LA32_P	H37	STACK_LA15_P
LA23_N	D24	STACK_LA06_N	LA33_N	G37	STACK_LA16_N
LA23_P	D23	STACK_LA06_P	LA33_P	G36	STACK_LA16_P
LA24_N	H29	STACK_LA07_N	SCL	C30	SCL
LA24_P	H28	STACK_LA07_P	SDA	C31	SDA

All stack signals are routed as differential pair with 100 ohm impedance and <1 mm length difference within the pair and < 5 mm between the pairs.
The SCL and SDA signal are 3V3 signals.

Appendix B: FMC stack connector ICD

Connector vendor : Samtec
Connector part number: ASP-134486-01

AV57	Con. Pin	Net name	AV57	Con. Pin	Net name
CLK0_M2C_N	H5	STACK_CLK0_M2C_N	DP8_M2C_P	B8	STACK_DP8_M2C_P
CLK0_M2C_P	H4	STACK_CLK0_M2C_N	DP9_C2M_N	B25	STACK_DP9_C2M_N
CLK1_M2C_N	G3	n.c.	DP9_C2M_P	B24	STACK_DP9_C2M_P
CLK1_M2C_P	G2	n.c.	DP9_M2C_N	B5	STACK_DP9_M2C_N
CLK2_BIDIR_N	K5	n.c.	DP9_M2C_P	B4	STACK_DP9_M2C_P
CLK2_BIDIR_P	K4	n.c.	GBTCLK0_M2C_N	D5	STACK_GBTCLK0_M2C_N
CLK3_BIDIR_N	J3	n.c.	GBTCLK0_M2C_P	D4	STACK_GBTCLK0_M2C_P
CLK3_BIDIR_P	J2	n.c.	GBTCLK1_M2C_N	B21	STACK_GBTCLK1_M2C_N
DP0_C2M_N	C3	STACK_DP0_C2M_N	GBTCLK1_M2C_P	B20	STACK_GBTCLK1_M2C_p
DP0_C2M_P	C2	STACK_DP0_C2M_P	HA00_N_CC	F5	n.c.
DP0_M2C_N	C7	STACK_DP0_M2C_N	HA00_P_CC	F4	n.c.
DP0_M2C_P	C6	STACK_DP0_M2C_P	HA01_N_CC	E3	n.c.
DP1_C2M_N	A23	STACK_DP1_C2M_N	HA01_P_CC	E2	n.c.
DP1_C2M_P	A22	STACK_DP1_C2M_P	HA02_N	K8	n.c.
DP1_M2C_N	A3	STACK_DP1_M2C_N	HA02_P	K7	n.c.
DP1_M2C_P	A2	STACK_DP1_M2C_P	HA03_N	J7	n.c.
DP2_C2M_N	A27	STACK_DP2_C2M_N	HA03_P	J6	n.c.
DP2_C2M_P	A26	STACK_DP2_C2M_P	HA04_N	F8	n.c.
DP2_M2C_N	A7	STACK_DP2_M2C_N	HA04_P	F7	n.c.
DP2_M2C_P	A6	STACK_DP2_M2C_P	HA05_N	E7	n.c.
DP3_C2M_N	A31	STACK_DP3_C2M_N	HA05_P	E6	n.c.
DP3_C2M_P	A30	STACK_DP3_C2M_P	HA06_N	K11	n.c.
DP3_M2C_N	A11	STACK_DP3_M2C_N	HA06_P	K10	n.c.
DP3_M2C_P	A10	STACK_DP3_M2C_P	HA07_N	J10	n.c.
DP4_C2M_N	A35	STACK_DP4_C2M_N	HA07_P	J9	n.c.
DP4_C2M_P	A34	STACK_DP4_C2M_P	HA08_N	F11	n.c.
DP4_M2C_N	A15	STACK_DP4_M2C_N	HA08_P	F10	n.c.
DP4_M2C_P	A14	STACK_DP4_M2C_P	HA09_N	E10	n.c.
DP5_C2M_N	A39	STACK_DP5_C2M_N	HA09_P	E9	n.c.
DP5_C2M_P	A38	STACK_DP5_C2M_P	HA10_N	K14	n.c.
DP5_M2C_N	A19	STACK_DP5_M2C_N	HA10_P	K13	n.c.
DP5_M2C_P	A18	STACK_DP5_M2C_P	HA11_N	J13	n.c.
DP6_C2M_N	B37	STACK_DP6_C2M_N	HA11_P	J12	n.c.
DP6_C2M_P	B36	STACK_DP6_C2M_P	HA12_N	F14	n.c.
DP6_M2C_N	B17	STACK_DP6_M2C_N	HA12_P	F13	n.c.
DP6_M2C_P	B16	STACK_DP6_M2C_P	HA13_N	E13	n.c.
DP7_C2M_N	B33	STACK_DP7_C2M_N	HA13_P	E12	n.c.
DP7_C2M_P	B32	STACK_DP7_C2M_P	HA14_N	J16	n.c.
DP7_M2C_N	B13	STACK_DP7_M2C_N	HA14_P	J15	n.c.

DP7_M2C_P	B12	STACK_DP7_M2C_P	HA15_N	F17	n.c.
DP8_C2M_N	B29	STACK_DP8_C2M_N	HA15_P	F16	n.c.
DP8_C2M_P	B28	STACK_DP8_C2M_P	HA16_N	E16	n.c.
DP8_M2C_N	B9	STACK_DP8_M2C_N	HA16_P	E15	n.c.
HA17_N_CC	K17	n.c.	HB15_N	J34	n.c.
HA17_P_CC	K16	n.c.	HB15_P	J33	n.c.
HA18_N	J19	n.c.	HB16_N	F35	n.c.
HA18_P	J18	n.c.	HB16_P	F34	n.c.
HA19_N	F20	n.c.	HB17_N_CC	K38	n.c.
HA19_P	F19	n.c.	HB17_P_CC	K37	n.c.
HA20_N	E19	n.c.	HB18_N	J37	n.c.
HA20_P	E18	n.c.	HB18_P	J36	n.c.
HA21_N	K20	n.c.	HB19_N	E34	n.c.
HA21_P	K19	n.c.	HB19_P	E33	n.c.
HA22_N	J22	n.c.	HB20_N	F38	n.c.
HA22_P	J21	n.c.	HB20_P	F37	n.c.
HA23_N	K23	n.c.	HB21_N	E37	n.c.
HA23_P	K22	n.c.	HB21_P	E36	n.c.
HB00_N_CC	K26	n.c.	LA00_N_CC	G7	STACK_LA00_N_CC
HB00_P_CC	K25	n.c.	LA00_P_CC	G6	STACK_LA00_P_CC
HB01_N	J25	n.c.	LA01_N_CC	D9	STACK_LA01_N_CC
HB01_P	J24	n.c.	LA01_P_CC	D8	STACK_LA01_P_CC
HB02_N	F23	n.c.	LA02_N	H8	STACK_LA02_N
HB02_P	F22	n.c.	LA02_P	H7	STACK_LA02_P
HB03_N	E22	n.c.	LA03_N	G10	STACK_LA03_N
HB03_P	E21	n.c.	LA03_P	G9	STACK_LA03_P
HB04_N	F26	n.c.	LA04_N	H11	STACK_LA04_N
HB04_P	F25	n.c.	LA04_P	H10	STACK_LA04_P
HB05_N	E25	n.c.	LA05_N	D12	STACK_LA05_N
HB05_P	E24	n.c.	LA05_P	D11	STACK_LA05_P
HB06_N_CC	K29	n.c.	LA06_N	C11	STACK_LA06_N
HB06_P_CC	K28	n.c.	LA06_P	C10	STACK_LA06_P
HB07_N	J28	n.c.	LA07_N	H14	STACK_LA07_N
HB07_P	J27	n.c.	LA07_P	H13	STACK_LA07_P
HB08_N	F29	n.c.	LA08_N	G13	STACK_LA08_N
HB08_P	F28	n.c.	LA08_P	G12	STACK_LA08_P
HB09_N	E28	n.c.	LA09_N	D15	STACK_LA09_N
HB09_P	E27	n.c.	LA09_P	D14	STACK_LA09_P
HB10_N	K32	n.c.	LA10_N	C15	STACK_LA10_N
HB10_P	K31	n.c.	LA10_P	C14	STACK_LA10_P
HB11_N	J31	n.c.	LA11_N	H17	STACK_LA11_N
HB11_P	J30	n.c.	LA11_P	H16	STACK_LA11_P
HB12_N	F32	n.c.	LA12_N	G16	STACK_LA12_N
HB12_P	F31	n.c.	LA12_P	G15	STACK_LA12_P
HB13_N	E31	n.c.	LA13_N	D18	STACK_LA13_N

HB13_P	E30	n.c.	LA13_P	D17	STACK_LA13_P
HB14_N	K35	n.c.	LA14_N	C19	STACK_LA14_N
HB14_P	K34	n.c.	LA14_P	C18	STACK_LA14_P
LA15_N	H20	STACK_LA15_N	LA25_N	G28	n.c.
LA15_P	H19	STACK_LA15_P	LA25_P	G27	n.c.
LA16_N	G19	STACK_LA16_N	LA26_N	D27	n.c.
LA16_P	G18	STACK_LA16_P	LA26_P	D26	n.c.
LA17_N_CC	D21	n.c.	LA27_N	C27	n.c.
LA17_P_CC	D20	n.c.	LA27_P	C26	n.c.
LA18_N_CC	C23	n.c.	LA28_N	H32	n.c.
LA18_P_CC	C22	n.c.	LA28_P	H31	n.c.
LA19_N	H23	n.c.	LA29_N	G31	n.c.
LA19_P	H22	n.c.	LA29_P	G30	n.c.
LA20_N	G22	n.c.	LA30_N	H35	n.c.
LA20_P	G21	n.c.	LA30_P	H34	n.c.
LA21_N	H26	n.c.	LA31_N	G34	n.c.
LA21_P	H25	n.c.	LA31_P	G33	n.c.
LA22_N	G25	n.c.	LA32_N	H38	n.c.
LA22_P	G24	n.c.	LA32_P	H37	n.c.
LA23_N	D24	n.c.	LA33_N	G37	n.c.
LA23_P	D23	n.c.	LA33_P	G36	n.c.
LA24_N	H29	n.c.	SCL	C30	STACK_SCL
LA24_P	H28	n.c.	SDA	C31	STACK_SDA

All stack signals are routed as differential pair with 100 ohm impedance and <1 mm length difference within the pair and < 5 mm between the pairs.
The SCL and SDA signal are 3V3 signals

Appendix C: ICD for Digital IO connector

Connector supplier: TE Connectivity
Connector part number: 5796055-1
QTY 2 Jack screws part number: 787004-3

P1 connector pin	Net name	Direction		P1 connector pin	Net name	Direction
1	ISO_GND			35	ISO_GND	
2	P1_D0	out		36	P1_D1	out
3	ISO_GND			37	ISO_GND	
4	P1_D2	out		38	P1_D3	out
5	ISO_GND			39	ISO_GND	
6	P1_D4	out		40	P1_D5	out
7	ISO_GND			41	ISO_GND	
8	P1_D6	out		42	P1_D7	out
9	GND ISO_GND			43	ISO_GND	
10	P1_D8	out		44	P1_D9	out
11	ISO_GND			45	ISO_GND	
12	P1_D10	out		46	P1_D11	out
13	ISO_GND			47	ISO_GND	
14	P1_D12	out		48	P1_D13	out
15	ISO_GND			49	ISO_GND	
16	P1_D14	out		50	P1_D15	out
17	ISO_GND			51	ISO_GND	
18	P1_DI_0	In		52	P1_DI_1	In
19	P1_DI_2	In		53	P1_DI_3	In
20	P1_DI_4	In		54	P1_DI_5	In
21	ISO_GND			55	ISO_GND	
22	P1_DI_6	In		56	P1_DI_7	In
23	P1_DI_8	In		57	P1_DI_9	In
24	P1_DI_10	In		58	P1_DI_11	In
25	ISO_GND			59	ISO_GND	
26	P1_DI_12	In		60	P1_DI_13	In
27	ISO_GND			61	ISO_GND	
28	P1_TRIGGER_OUT[1]	out		62	P1_DI_14	In
29	ISO_GND			63	ISO_GND	
30	CLK	out		64	n.c.	
31	ISO_GND			65	ISO_GND	
32	P1_TRIGGER_IN[1]	in		66	P1_DI_15	In
33	ISO_GND			67	ISO_GND	
34	n.c.			68	n.c.	

P1_SHIELD connects to ISO_GND through a capacitor in parallel with a 0-ohm resistor

The FMC_TRIGGER_IN and FMC_TRIGGER_OUT connection to P1_TRIGGER_IN and P1_TRIGGER_OUT can be changed using a resistor build option. See chapter 5 for more details.

APPENDIX E: FMC carrier board compatibility chart

Table 4: LXF90K0 FMC compatibility

FMC Connector /site	LX41K0	LXD41K0-S + LXD41K0
FMC	Compatible	Compatible

Table 5: KCU105 FMC compatibility

FMC Connector /site	LX41K0	LXD41K0-S + LXD41K0
FMC LPC	Compatible	Compatible
FMC HPC	Compatible	Compatible

Table 6: TEB0911 FMC compatibility

TEC0911 FMC Connector /site	LX41K0	LXD41K0-S + LXD41K0
J4 / FMC B	Compatible	Compatible
J6 / FMC E	Compatible	Compatible
J7 / FMC D	Compatible	Compatible
J8 / FMC C	Compatible	Compatible
J10 / FMC A	Not supported	Not supported
J21 / FMC F	Not supported	Not supported

Appendix E: Revision history

Document Revision	Changes			Quality Approval	Date
R1.0	First release			EBA	November 28, 2025