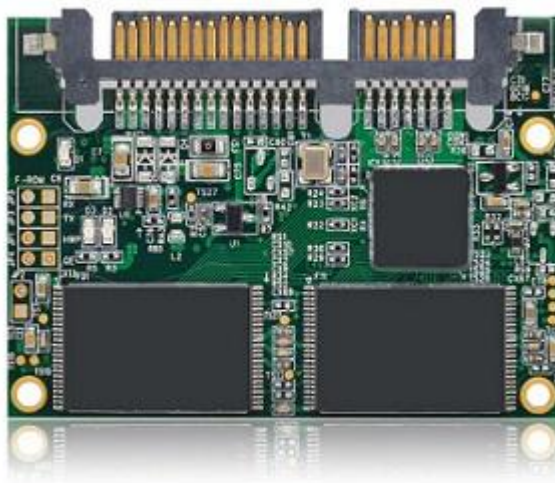


ShenZhen Renice Technology Co., Ltd

# X5A Half-slim SATAIII SSD

Datasheet



V1.1

2017-8-20



# CATALOGUE

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# 1. Introduction

## 1.1 Product Overview

The Renice X5A Halfslim SATAIII SSD is a high capacity SSD solution delivers extremely high performance up to 520MB/S read and 440MB/S write through the SATAIII 6.0Gbps interface. The X5A is ideal for a variety of applications, including enterprise solutions where data throughput needs to be high, as well as industrial and military installations where the potential for high shock and vibration conditions exist. fully compliant with JEDEC MO-297 industrial standard.

X5A Halfslim SSD carries up to 512MB DDR3 Cache which gains high performance. With adopting SLC/ MLC NAND flash technology, and utilizing a unique firmware architecture, the X5A maximizes the bandwidth limitations of SATA III providing up to 75,000 input/output operations per second (IOPS).

## 1.2 Feature

- **Standard Serial ATA:** SATA III, 6.0Gbps (Backward compatible with SATA 1.5 and 3.0Gbps)
- **Form factor:** (54.0mm x 39.0mm x 4.0mm) L×W×H
- **Connector:** 7+15pin SATAIII 6.0Gb/s
- **Performance:**
  - Max Sequential Data Read/Write: 520MB/440MB/s
  - 4Kb Random Read/Write IOPS: 70,000 / 75,000
  - Access Time: <0.1ms
- **Capacities:** 64GB, 128GB, 256GB, 512GB (MLC)  
32GB, 64GB, 128GB, 256GB (SLC)
- **Power Management:**
  - Input voltage: 5V (±5%)
  - Support Hot Plug/Removal Function
- **Temperature ranges:**
  - Operation: -40°C to +85°C
  - Storage: -50°C to +95°C
- **Intelligent features:**
  - Flash management algorithm: static and dynamic wear-leveling, bad block management algorithm
  - Supports dynamic power management and SMART (Self-Monitoring, Analysis and Reporting Technology)
  - Supports BCH ECC 66bits in 1KBytes
  - Support Power Failure Protection
  - Support over Voltage Protection
  - Support AES 256bit Encryption (Optional)
  - Support Secure Erase (Optional)

- Support TRIM
- Support NCQ
- **MTBF:** >3,000,000 Hours @25C

## 2. Functional Block Diagram

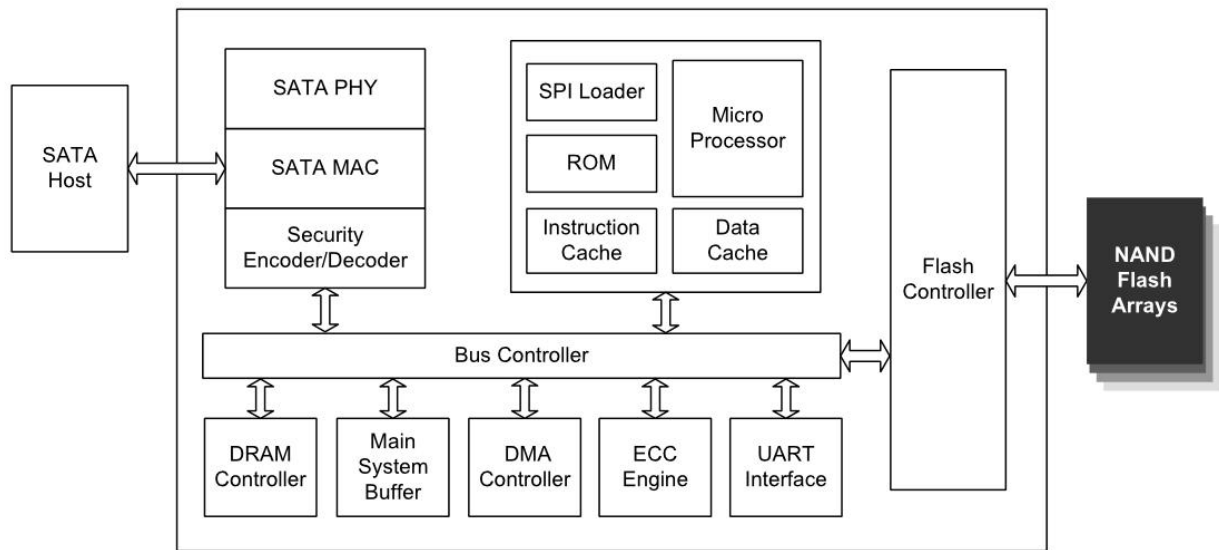


Figure 1: Renice X5A Half-Slim SATAIII SSD Block Diagram



## 3. Product Specifications

### 3.1 Physical Specifications

Table 1: Physical Specifications

|                    |                   |                    |
|--------------------|-------------------|--------------------|
| <b>Form Factor</b> | Half-slim         |                    |
| <b>Dimensions</b>  | Length            | 54.0mm $\pm$ 0.2mm |
|                    | Width             | 39.0mm $\pm$ 0.2mm |
|                    | Height            | 4mm $\pm$ 0.2mm    |
| <b>Weight</b>      | <30g              |                    |
| <b>Connector</b>   | SATA III 7+15 pin |                    |

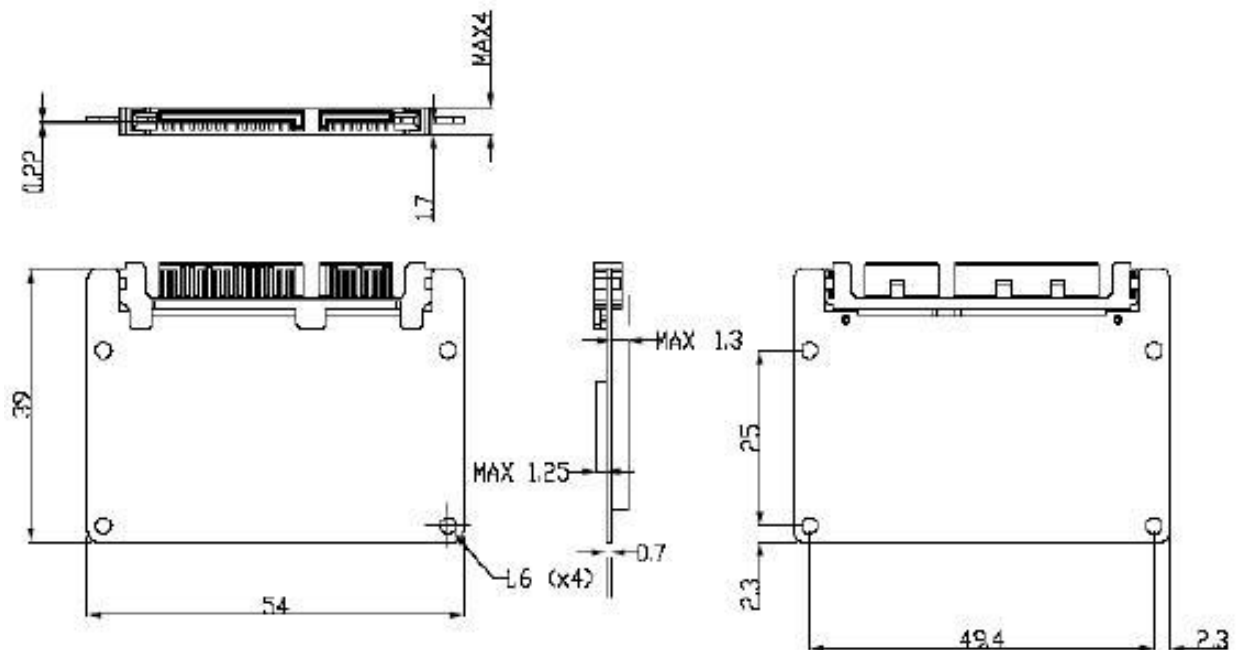


Figure 2: Renice X5A Half-slim SATAIII SSD mechanical dimensions

### 3.2 Host Interface

Industrial Standard SATA Revision 3.1 compliant

Industrial Standard ATA/ATAPI-8 ACS-2 command compliant

Supports SATA interface rate of 6Gb/s(backward compatible to 1.5Gb/s and 3Gb/s)

Native Command Queuing (NCQ): up to 32 commands

S.M.A.R.T. command transport (SCT) technology

SATA Device Sleep( Dev Sleep)

Data Set Management command (TRIM)

Supports 28bit and 48bit LBA mode commands



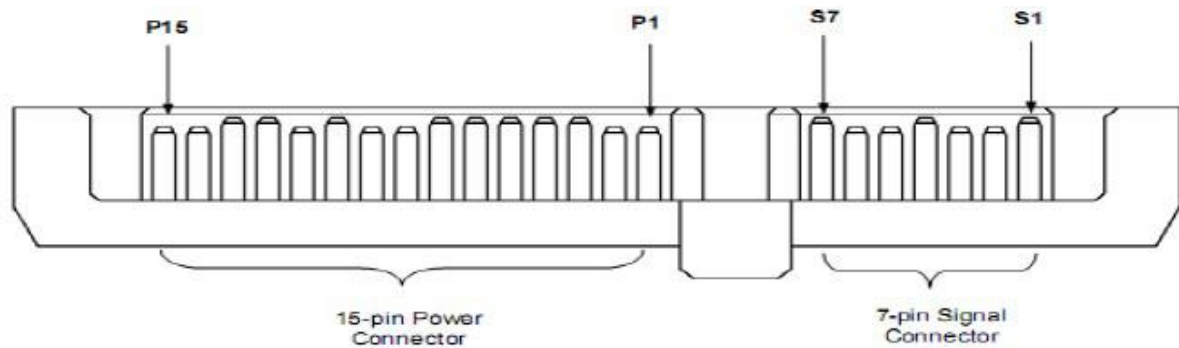
## 3.3 Capacity

**Table 2: Capacity Specification**

| Parameter. | LBA Counts(512Byte) | Over-provision (%) |
|------------|---------------------|--------------------|
| 32GB       | 61,865,984          | 6.25               |
| 64GB       | 123,731,968         | 6.25               |
| 128GB      | 247,463,936         | 6.25               |
| 256GB      | 494,927,872         | 6.25               |
| 512GB      | 989,855,744         | 6.25               |

## 4. Interface Description

### 4.1 Pin Assignment



**Figure 3: Pin Assignments**



## 4.2 Pin Description

**Table 3: Signal and Power segment**

| Pin No. | Pin Name                           | Pin No. | Pin Name    |
|---------|------------------------------------|---------|-------------|
| S1      | GND (2 <sup>nd</sup> mate)         | P1      | Not Connect |
| S2      | SATA Differential RX+ based on SSD | P2      | Not Connect |
| S3      | SATA Differential RX- based on SSD | P3      | CDI/DEVSLP  |
| S4      | GND(2 <sup>nd</sup> mate)          | P4      | GND         |
| S5      | SATA Differential TX- based on SSD | P5      | GND         |
| S6      | SATA Differential TX+ based on SSD | P6      | GND         |
| S7      | GND(2 <sup>nd</sup> mate)          | P7      | +5V         |
|         |                                    | P8      | +5V         |
|         |                                    | P9      | +5V         |
|         |                                    | P10     | GND         |
|         |                                    | P11     | DAS         |
|         |                                    | P12     | GND         |
|         |                                    | P13     | Not Connect |
|         |                                    | P14     | SE IN       |
|         |                                    | P15     | SE LED      |

## 5. Power Specifications

### 5.1 Operating Voltage

Operating voltage: 5V ( $\pm 5\%$ )

### 5.2 Power Supply Voltage

1.2V for Core, 3.3V for NAND and IO

### 5.3 Power Consumption (typical)

Operation (Read/Write) –1.1W/ 6W

Idle – 0.6W

Standby - 0.45W



## 6. Reliability Specification

### 6.1 Environment

**Table 4: Environmental Specifications**

| Item        | Features                                                                                                                                                                              |                       |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| Temperature | Operation                                                                                                                                                                             | Industrial: -40~+85°C |
| Humidity    | 5-95%                                                                                                                                                                                 |                       |
| Vibration   | 10Hz-2000Hz, 16.4 G (X, Y, Z axis, 1 hour /axis)                                                                                                                                      |                       |
| Shock       | Peak Acceleration: 1,500 G, 0.5ms(Half-sine wave, $\pm X, \pm Y, \pm Z$ axis, 1 time/axis)<br>Peak Acceleration: 50 G, 11ms(Half-sine wave, $\pm X, \pm Y, \pm Z$ axis, 3 times/axis) |                       |

### 6.2 Wear-leveling

Renice X5A Half-slim SATAIII SSD support both static and dynamic wear-leveling, these two algorithms guarantee all type of flash memory at same level of erase cycles to improve lifetime limitation of NAND based storage.

### 6.3 H/W ECC and EDC for NAND Flash

BCH ECC 66 bits in 1024 bytes.

### 6.4 Power Failure Protection

Renice X5A Half-slim SATAIII SSD adopts Voltage Detector Circuit to detect current voltage status, when current voltage is detected abnormal, the controller will block the NAND WP(write protect) pin to stop the data to be written into NAND, and ensure the existed data integrity upon sudden power loss.

### 6.5 Endurance

Write endurance: >25 years @ 100GB write/ day (512GB MLC)

Read endurance: unlimited



## 6.6 MTBF

MTBF (Mean Time between Failures) of Renice X5A Halfslim SATAIII SSD: >3,000,000 Hours  
@25C

## 7. Security Function (Optional)

Renice X5A Half-slim SSD reserves GPIO for emergency data erase. External wires connected to reserve Pinout (P14) to GND for above 3 seconds to trigger Secure Erase. The process of erase will not stop until finished when power loss occurs, it will continue when power is on again.

No matter Renice X5A Half-slim SSD is acting as master drive or slave drive, once the Secure Erase function is triggered, SE will be carried out immediately whether the SSD is in idle mode (no read/ write) or work (read/ write) mode.

### 7.1 Technical Concept

The SE command is transmitted to controller chip from the GPIO of the IO expanding chip, SE could be triggered by pulling GPIO down for 3 seconds whether through HW (i.e. external switch or button) or SW, the controller will then send Delete Command to NAND Flash to start SE.

**a. Trigger Time: 0~3 seconds**

Controller will take it as spurious triggering and no SE command will be sent.

**b. Trigger Time: 3~10 seconds**

All data on board will be deleted and data of 00 pattern will be written in.



## 8. Supported ATA Command Lists

Table 5: Support ATA Command Lists

| Command                             | Code       | Protocol                  |
|-------------------------------------|------------|---------------------------|
| <b>General Feature Set</b>          |            |                           |
| Execute Device Diagnostic           | 90h        | Execute device diagnostic |
| Flush Cache                         | E7h        | Non-data                  |
| Identify Device                     | ECh        | PIO data-in               |
| Initialize Drive Parameters         | 91h        | Non-data                  |
| Read DMA                            | C8h        | DMA                       |
| Read Log Ext                        | 2Fh        | PIO data-in               |
| Read Multiple                       | C4h        | PIO data-in               |
| Read Sector(s)                      | 20h        | PIO data-in               |
| Read Verify Sector(s)               | 40h or 41h | Non-data                  |
| Set Feature                         | EFh        | Non-data                  |
| Set Multiple Mode                   | C6h        | Non-data                  |
| Write DMA                           | CAh        | DMA                       |
| Write Multiple                      | C5h        | PIO data-out              |
| Write Sector(s)                     | 30h        | PIO data-out              |
| NOP                                 | 00h        | Non-data                  |
| Read Buffer                         | E4h        | PIO data-in               |
| Write Buffer                        | E8h        | PIO data-out              |
| <b>Power Management Feature Set</b> |            |                           |
| Check Power Mode                    | E5h or 98h | Non-data                  |
| Idle                                | E3h or 97h | Non-data                  |
| Idle Immediate                      | E1h or 95h | Non-data                  |
| Sleep                               | E6h or 99h | Non-data                  |
| Standby                             | E2h or 96h | Non-data                  |
| Standby Immediate                   | E0h or 94h | Non-data                  |
| <b>Security Mode Feature Set</b>    |            |                           |
| Security Set Password               | F1h        | PIO data-out              |
| Security Unlock                     | F2h        | PIO data-out              |
| Security Erase Prepare              | F3h        | Non-data                  |
| Security Erase Unit                 | F4h        | PIO data-out              |
| Security Freeze Lock                | F5h        | Non-data                  |
| Security Disable Password           | F6h        | PIO data-out              |



|                                        |     |              |
|----------------------------------------|-----|--------------|
| SMART Disable Operations               | B0h | Non-data     |
| SMART Enable/Disable Autosave          | B0h | Non-data     |
| SMART Enable Operations                | B0h | Non-data     |
| SMART Execute OFF-LINE Immediate       | B0h | Non-data     |
| SMART Read Log                         | B0h | PIO data-in  |
| SMART Read Data                        | B0h | PIO data-in  |
| SMART Read Threshold                   | B0h | PIO data-in  |
| SMART Return Status                    | B0h | Non-data     |
| SMART Save Attribute Values            | B0h | Non-data     |
| SMART Write Log                        | B0h | PIO data-out |
| <b>Host Protected Area Feature Set</b> |     |              |
| Read Native Max Address                | F8h | Non-data     |
| Set Max Address                        | F9h | Non-data     |
| Set Max Set Password                   | F9h | PIO data-out |
| Set Max Lock                           | F9h | Non-data     |
| Set Max Freeze Lock                    | F9h | Non-data     |
| Set Max Unlock                         | F9h | PIO data-out |
| <b>48-bit Address Feature Set</b>      |     |              |
| Flush Cache Ext                        | EAh | Non-data     |
| Read Sector(s) Ext                     | 24h | PIO data-in  |
| Read DMA Ext                           | 25h | DMA          |
| Read Multiple Ext                      | 29h | PIO data-in  |
| Read Native Max Address Ext            | 27h | Non-data     |
| Read Verify Sector(s) Ext              | 42h | Non-data     |
| Set Max Address Ext                    | 37h | Non-data     |
| Write DMA Ext                          | 35h | DMA          |
| Write Multiple Ext                     | 39h | PIO data-out |
| Write Sector(s) Ext                    | 34h | PIO data-out |
| <b>NCQ Feature Set</b>                 |     |              |
| Read FPDMA Queued                      | 60h | DMA Queued   |
| Write FPDMA Queued                     | 61h | DMA Queued   |
| <b>Others</b>                          |     |              |
| Data Set Management                    | 06h | DMA          |
| Seek                                   | 70h | Non-data     |



## 9. SMART Feature Set

The Renice X5A Halfslim SATAIII SSD supports the SMART command set and defines some vendor-specific data to report spare/bad block numbers in each memory management unit.

Table 6: SMART Feature Register Values

| Command Name                            | Command Code |
|-----------------------------------------|--------------|
| SMART READ DATA                         | D0h          |
| SMART Read Attribute Threshold          | D1h          |
| SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE | D2h          |
| SMART SAVE ATTRIBUTE VALUES             | D3h          |
| SMART EXECUTE OFF-LINE IMMEDIATE        | D4h          |
| SMART READ LOG                          | D5h          |
| SMART WRITE LOG                         | D6h          |
| SMART ENABLE OPERATIONS                 | D8h          |
| SMART DISABLE OPERATIONS                | D9h          |
| SMART RETURN STATUS                     | DAh          |



## 9.1 SMART Data Structure

The following 512bytes make up the device SMART data structure. Users can obtain the data using the “Read Data” command (D0h).

**Table 7: SMART Data Structure**

| Byte      | F / V | Description                                                                          |
|-----------|-------|--------------------------------------------------------------------------------------|
| 0 - 1     | X     | Revision code                                                                        |
| 2 - 361   | X     | Vendor specific (see 4.3.2)                                                          |
| 362       | V     | Off-line data collection status                                                      |
| 363       | X     | Self-test execution status byte                                                      |
| 364 - 365 | V     | Total time in seconds to complete off-line data collection activity                  |
| 366       | X     | Vendor specific                                                                      |
| 367       | F     | Off-line data collection capability                                                  |
| 368 - 369 | F     | SMART capability                                                                     |
| 370       | F     | Error logging capability<br>• 7-1 Reserved<br>• 0 1 = Device error logging supported |
| 371       | X     | Vendor specific                                                                      |
| 372       | F     | Short self-test routine recommended polling time (in minutes)                        |
| 373       | F     | Extended self-test routine recommended polling time (in minutes)                     |
| 374       | F     | Conveyance self-test routine recommended polling time (in minutes)                   |
| 375 - 385 | R     | Reserved                                                                             |
| 386 - 395 | F     | Firmware version/date code                                                           |
| 396 - 399 | F     | Reserved                                                                             |
| 400 - 405 | F     | 'SM2246'                                                                             |
| 406 - 510 | X     | Vendor specific                                                                      |
| 511       | V     | Data structure checksum                                                              |

**Notes:**

1. F = content (byte) is fixed and does not change.
2. V = content (byte) is variable and may change depending on the state of the device or the commands executed by the device.
3. X = content (byte) is vendor specific and may be fixed or variable.
4. R = content (byte) is reserved and shall be zero.



## 9.2 SMART Attributes

The following table defines the vendor specific data in byte 2 to 361 of the 512byte SMART data.

**Table 8: SMART Data Vendor-specific Attributes**

| Attribute ID (hex) | Raw Attribute Value |     |    |     |    |    |     | Attribute Name                              |
|--------------------|---------------------|-----|----|-----|----|----|-----|---------------------------------------------|
| 01                 | MSB                 | 00  | 00 | 00  | 00 | 00 | 00  | Read error rate                             |
| 05                 | LSB                 | MSB | 00 | 00  | 00 | 00 | 00  | Reallocated sectors count                   |
| 09                 | LSB                 |     |    | MSB | 00 | 00 | 00  | Power-on hours                              |
| 0C                 | LSB                 |     |    | MSB | 00 | 00 | 00  | Power cycle count                           |
| A0                 | LSB                 |     |    | MSB | 00 | 00 | 00  | Uncorrectable sector count when read/write  |
| A1                 | LSB                 | MSB | 00 | 00  | 00 | 00 | 00  | Number of valid spare block                 |
| A3                 | LSB                 | MSB | 00 | 00  | 00 | 00 | 00  | Number of initial invalid block             |
| A4                 | LSB                 |     |    | MSB | 00 | 00 | 00  | Total erase count                           |
| A5                 | LSB                 |     |    | MSB | 00 | 00 | 00  | Maximum erase count                         |
| A6                 | LSB                 |     |    | MSB | 00 | 00 | 00  | Minimum erase count                         |
| A7                 | LSB                 |     |    | MSB | 00 | 00 | 00  | Average erase count                         |
| A8                 | LSB                 |     |    | MSB | 00 | 00 | 00  | Max erase count of spec                     |
| A9                 | LSB                 |     |    | MSB | 00 | 00 | 00  | Remain Life (percentage)                    |
| AF                 | LSB                 |     |    | MSB | 00 | 00 | 00  | Program fail count in worst die             |
| B0                 | LSB                 | MSB | 00 | 00  | 00 | 00 | 00  | Erase fail count in worst die               |
| B1                 | LSB                 |     |    | MSB | 00 | 00 | 00  | Total wearlevel count                       |
| B2                 | LSB                 | MSB | 00 | 00  | 00 | 00 | 00  | Runtime invalid block count                 |
| B5                 | LSB                 |     |    | MSB | 00 | 00 | 00  | Total program fail count                    |
| B6                 | LSB                 | MSB | 00 | 00  | 00 | 00 | 00  | Total erase fail count                      |
| BB                 | LSB                 |     |    | MSB | 00 | 00 | 00  | Uncorrectable error count                   |
| C0                 | LSB                 | MSB | 00 | 00  | 00 | 00 | 00  | Power-off retract count                     |
| C2                 | MSB                 | 00  | 00 | 00  | 00 | 00 | 00  | Controlled temperature                      |
| C3                 | LSB                 |     |    | MSB | 00 | 00 | 00  | Hardware ECC recovered                      |
| C4                 | LSB                 |     |    | MSB | 00 | 00 | 00  | Reallocation event count                    |
| C6                 | LSB                 |     |    | MSB | 00 | 00 | 00  | Uncorrectable error count off-line          |
| C7                 | LSB                 | MSB | 00 | 00  | 00 | 00 | 00  | UltraDMA CRC error count                    |
| E1                 | LSB                 |     |    |     |    |    | MSB | Total LBAs written (each write unit = 32MB) |
| E8                 | LSB                 | MSB | 00 | 00  | 00 | 00 | 00  | Available reserved space                    |
| F1                 | LSB                 |     |    |     |    |    | MSB | Total LBAs written (each write unit = 32MB) |
| F2                 | LSB                 |     |    |     |    |    | MSB | Total LBAs read (each read unit = 32MB)     |



## 10. Ordering Information

**Table 9: Valid Combinations**

| Capacities/Flash type | Industrial Temp | Part Number  |
|-----------------------|-----------------|--------------|
| 64GB/MLC              | -40°C to +85°C  | RIM064-SX5AH |
| 128GB/MLC             | -40°C to +85°C  | RIM128-SX5AH |
| 256GB/MLC             | -40°C to +85°C  | RIM256-SX5AH |
| 512GB/MLC             | -40°C to +85°C  | RIM512-SX5AH |
| 32GB/SLC              | -40°C to +85°C  | RIS032-SX5AH |
| 64GB/SLC              | -40°C to +85°C  | RIS064-SX5AH |
| 128GB/SLC             | -40°C to +85°C  | RIS128-SX5AH |
| 256GB/SLC             | -40°C to +85°C  | RIS256-SX5AH |



## 11. Part Number Naming Rule

