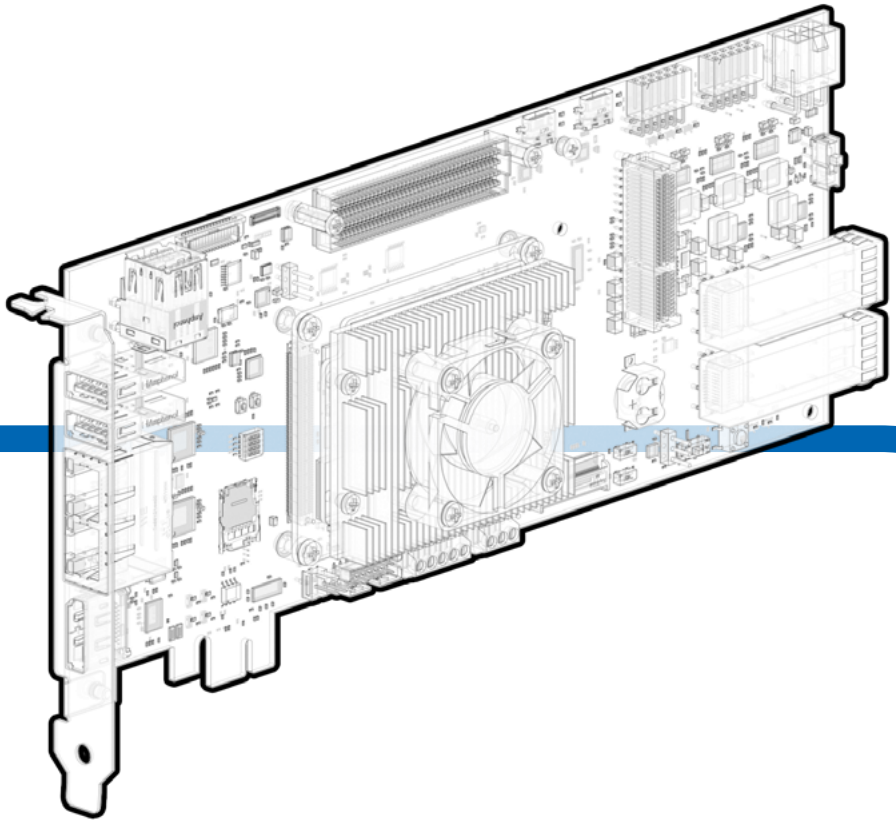
Datasheet



DE160100

AMD Kria SoM PCIe

Development Kit

DEICO

www.deico.com.tr

Contents

1. Description

DE160100 AMD Kria SoM PCIe Development Kit is a feature-rich, high-performance carrier board carefully designed to unlock the full potential of the AMD Kria™ K26 System-on-Module (SoM). While the K26 SoM itself integrates a powerful AMD Zynq™ UltraScale+™ MPSoC, memory, boot, and security module into a compact form factor, the AMD Kria SoM PCIe Development Kit dramatically expands its connectivity and application capabilities.

This carrier card provides an extensive array of industry-standard interfaces, facilitating prototyping and deployment for complex embedded systems. Key interfacing options include versatile high-speed data ports such as 4-port USB 3.0, DisplayPort 1.2a, dual SFP+ cages for flexible optical networking, and comprehensive PCIe connectivity with both x1 PCIe Gen3 Endpoint and x2 PCIe Gen3 Root Complex capabilities. Storage solutions are robust, featuring an M.2 SATA slot, a uSD Card interface, and an 8 kbit EEPROM for non-volatile configuration data.

Networking is well-supported with both 1G PS Ethernet and 1G PL Ethernet ports. For imaging and vision applications, the card incorporates an RPi Camera CSI-2 interface and a generic IAS (Image Sensor) Interface. Development and debugging are streamlined with onboard JTAG, dual PMOD connectors for extendibility, an LPC FMC connector for further expansion, and dual UART to USB converters for easy console access. Industrial connectivity is also a core focus, with integrated CAN bus and dual RS-485 transceivers.

1.1. Key Features

- PCIe Gen3 x2 Root Complex
- PCIe Gen3 x1 Endpoint
- 4-Port USB 3.0 Hub
- DisplayPort 1.2a
- 1G PS ethernet (RJ45)
- 1G PL ethernet (RJ45)
- Dual SFP+ Cages
- M.2 SATA connector (M-Key)
- MicroSD card slot
- LPC FMC connector
- Dual PMOD connectors
- Raspberry Pi camera interface (CSI-2)
- Generic IAS (image sensor) interface
- Dual RS-485 transceivers
- CAN bus transceiver
- Dual UART-to-USB bridges
- System health monitor IC
- Hardware watchdog timer
- 8 kbit I²C EEPROM

2. Hardware Overview

2.1. Circuitry

DE160100 AMD Kria SoM PCIe Development Kit is a feature-rich, high-performance carrier card meticulously designed to unlock the full potential of the AMD Kria™ K26 System-on-Module (SoM). It bridges the gap between the compact, powerful K26 SoM and the demands of real-world applications by providing an extensive array of industry-standard interfaces for connectivity, storage, and expansion.

This board is engineered to accelerate development cycles for complex embedded systems. Its core capabilities include versatile high-speed connectivity with dual PCIe Gen3 interfaces (Root Complex and Endpoint), a quad-port USB 3.0 hub, and a DisplayPort 1.2a output. Networking is exceptionally flexible, featuring both PS and PL-based Gigabit Ethernet ports alongside dual SFP+ cages for fibre optic or other high-speed links.

For industrial and vision applications, the board is equipped with dual RS-485 transceivers, a CAN bus interface, a Raspberry Pi camera connector, and a generic IAS interface. Robust storage options are provided through an M.2 SATA slot and a MicroSD card interface. With integrated development essentials like an LPC FMC connector, dual PMODs, and on-board JTAG and UART-to-USB debugging, the AMD Kria SoM PCIe Development Kit serves as a complete and powerful platform for prototyping and deployment in fields such as machine vision, industrial automation, networking, and edge AI.

Block diagram of the AMD Kria SoM PCIe Development Kit is shown in Figure 1.

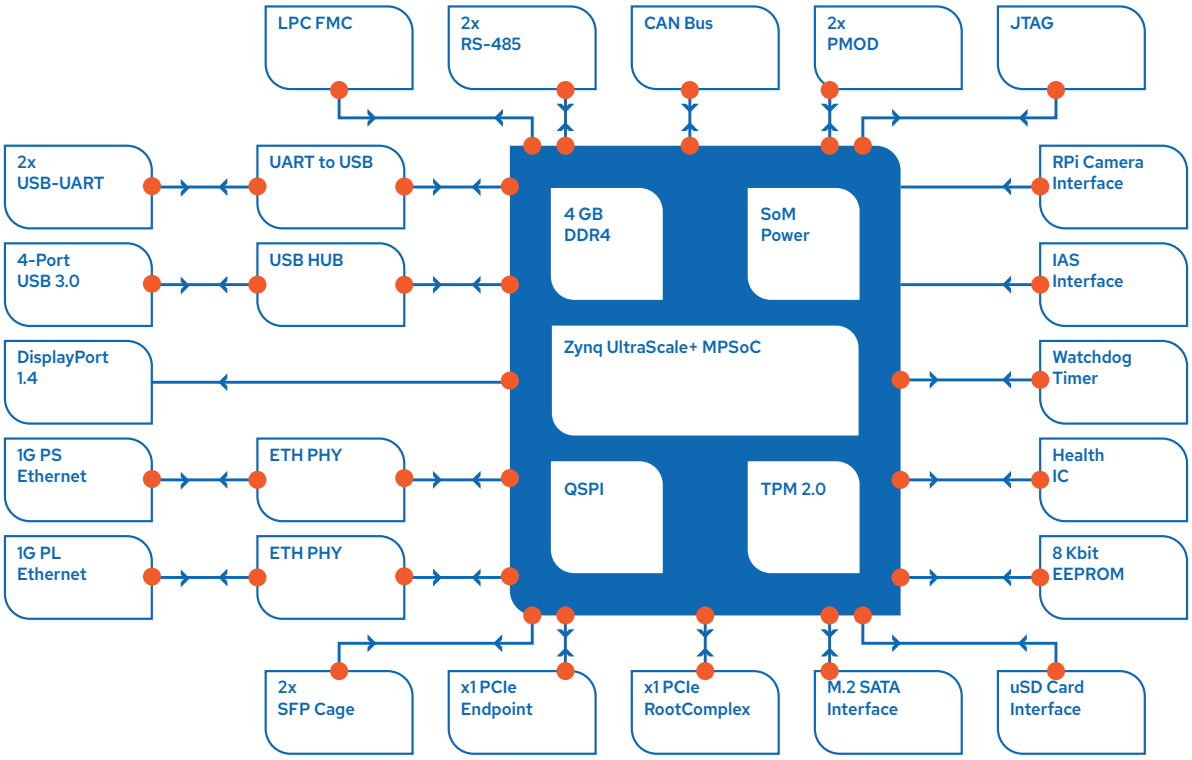


Figure 1: Block Diagram of the Carrier Board

2.2. Hardware Specifications

2.2.1. 1G PS Ethernet

The carrier board includes a Gigabit Ethernet port directly connected to the Processing System (PS) of the Kria K26 SoM. This interface leverages the Zynq UltraScale+ MPSoC's hardened Gigabit Ethernet MAC (GEM) controller, providing a high-performance, low-latency network connection ideal for the primary operating system, management access, and data-intensive applications. Block diagram of 1G PS ethernet is shown in Figure 2. Detailed pinout for the 1G PS ethernet is provided in Table 1.

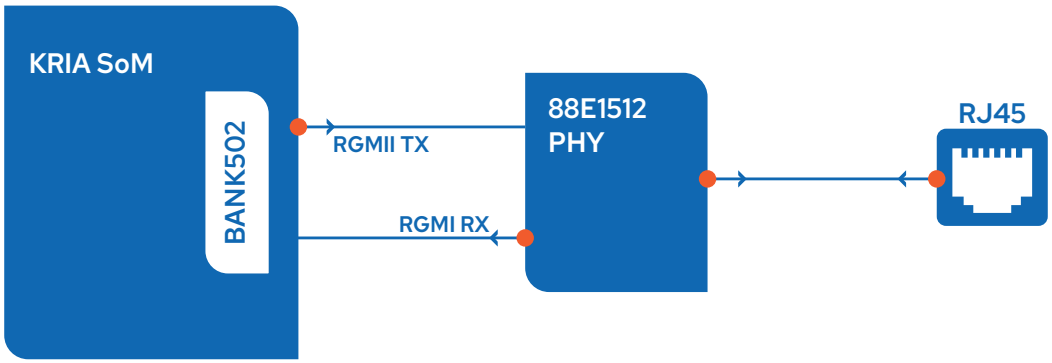


Figure 2: Block Diagram of PS Ethernet

Table 1: Pinout of PS Ethernet

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
MIO64	J1-D40	E19	ETH_PS_TX_CLK	PS Ethernet RGMII Transmit Clock
MIO65	J1-D41	A18	ETH_PS_TXD0	PS Ethernet Transmit Data 0
MIO66	J1-D42	G19	ETH_PS_TXD1	PS Ethernet Transmit Data 1
MIO67	J1-C42	B18	ETH_PS_TXD2	PS Ethernet Transmit Data 2
MIO68	J1-C43	C18	ETH_PS_TXD3	PS Ethernet Transmit Data 3
MIO69	J1-C44	D19	ETH_PS_TX_CTRL	PS Ethernet RGMII Transmit Enable
MIO70	J1-B44	C19	ETH_PS_RX_CLK	PS Ethernet RGMII Receive Clock
MIO71	J1-B45	B19	ETH_PS_RXD0	PS Ethernet Receive Data 0
MIO72	J1-B46	G20	ETH_PS_RXD1	PS Ethernet Receive Data 1
MIO73	J1-A42	G21	ETH_PS_RXD2	PS Ethernet Receive Data 2
MIO74	J1-A43	D20	ETH_PS_RXD3	PS Ethernet Receive Data 3
MIO75	J1-A44	A19	ETH_PS_RX_CTRL	PS Ethernet RGMII Receive Enable
MIO76	J1-D44	B20	ETH_PS_MDC	PS Ethernet MDIO Clock
MIO77	J1-D45	F20	ETH_PS_MDIO	PS Ethernet MDIO Data
MIO38	J1-B32	H18	ETH_PS_RSTn	PS Ethernet Reset (Active Low)

2.2.1.1. PS Ethernet Implementation and Key Specifications

- The port interfaces with the K26 SoM's dedicated GEM controller via a standard RGMII (Reduced Gigabit Media-Independent Interface).
- The physical layer is implemented using a Marvell Alaska 88E1512 Gigabit Ethernet PHY. This industry-standard IC handles the 10/100/1000 Mb/s auto-negotiation and translates the RGMII signals to the standard ethernet electrical signals required for the physical connection.
- A standard RJ45 connector with integrated magnetics and status LEDs is used.
- The port supports auto-negotiation for 10/100/1000 Mb/s data rates, full-duplex and half-duplex.
- The integrated LEDs provide at-a-glance feedback on link status, network activity, and connection speed.
- 88E1512 Gigabit Ethernet PHY Address is 0x01.

2.2.2. 1G PL Ethernet

In addition to the PS-based ethernet port, the carrier board provides a second, independent Gigabit Ethernet interface connected directly to the Programmable Logic (PL) fabric of the Kria K26 SoM. This architecture allows for the implementation of a user-defined ethernet MAC (e.g., the Xilinx AXI 1G/2.5G Ethernet Subsystem IP) within the FPGA.

This PL-based port is ideal for applications requiring a dedicated, low-latency network for FPGA-centric tasks—such as real-time video streaming, industrial control, or network packet processing—completely independent of the main processing system's network traffic. Block diagram of 1G PL Ethernet is shown in Figure 3. Detailed pinout for the 1G PL Ethernet is provided in Table 2.

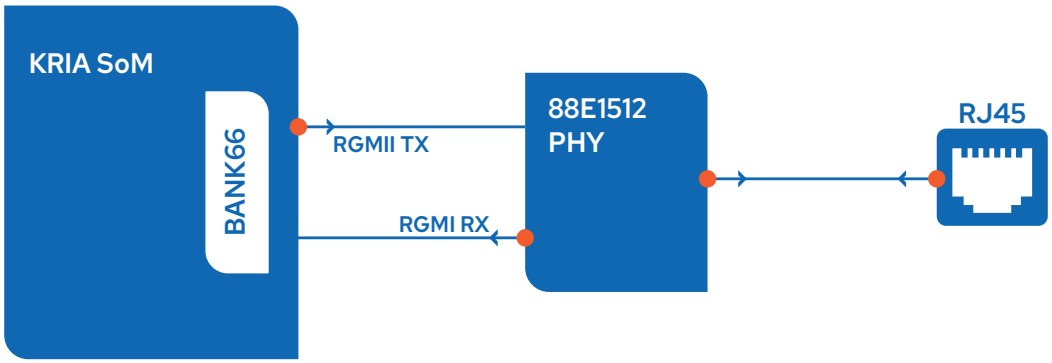


Figure 3: Block Diagram of PL Ethernet

Table 2: Pinout of PL Ethernet

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
HPA03_P	J1-C6	G3	ETH_PL_TX_CLK	PL Ethernet RGMII Transmit Clock
HPA02_N	J1-D5	E2	ETH_PL_TXD0	PL Ethernet Transmit Data 0
HPA02_P	J1-D4	F2	ETH_PL_TXD1	PL Ethernet Transmit Data 1
HPA01_N	J1-D8	D1	ETH_PL_TXD2	PL Ethernet Transmit Data 2
HPA01_P	J1-D7	E1	ETH_PL_TXD3	PL Ethernet Transmit Data 3
HPA03_N	J1-C7	F3	ETH_PL_TX_CTRL	PL Ethernet RGMII Transmit Enable
HPA_CLK0_P	J1-A6	C3	ETH_PL_RX_CLK	PL Ethernet RGMII Receive Clock
HPA13_N	J1-A13	F7	ETH_PL_RXD0	PL Ethernet Receive Data 0
HPA13_P	J1-A12	G8	ETH_PL_RXD1	PL Ethernet Receive Data 1
HPA04_N	J1-B5	E3	ETH_PL_RXD2	PL Ethernet Receive Data 2
HPA04_P	J1-B4	E4	ETH_PL_RXD3	PL Ethernet Receive Data 3
HPA_CLK0_N	J1-A7	C2	ETH_PL_RX_CTRL	PL Ethernet RGMII Receive Enable
HPA14_P	J1-D13	F8	ETH_PL_MDC	PL Ethernet MDIO Clock
HPA14_N	J1-D14	E8	ETH_PL_MDIO	PL Ethernet MDIO Data
HPA00_CC_P	J1-C3	G1	ETH_PL_RST	PL Ethernet Reset (Active Low)

2.2.2.1. PL Ethernet Implementation and Key Specifications

- The interface connects to standard I/O pins on the Kria SoM's PL side via RGMII. This requires a soft MAC IP core to be instantiated in the FPGA design.
- The physical layer is implemented using a Marvell Alaska 88E1512 Gigabit Ethernet PHY. This industry-standard IC handles the 10/100/1000 Mb/s auto-negotiation and translates the RGMII signals to the standard ethernet electrical signals.
- A standard RJ45 connector with integrated magnetics and status LEDs is used for the physical connection.
- The port supports auto-negotiation for 10/100/1000 Mb/s data rates, full-duplex and half-duplex.
- The integrated LEDs provide at-a-glance feedback on link status, network activity, and connection speed.
- 88E1512 Gigabit Ethernet PHY Address is 0x01.

2.2.3. PS-GTR Transceiver Lane Allocation (4 Lanes)

The four GTR transceivers on the Processing System (PS) side are allocated to dedicated, high-speed peripherals. The GTR transceivers functionality is given in Table 3.

Table 3: GTR Transceiver Functionality

GTR Lane	Signal Type	Destination Interface
Lane 0	PCIe	Multiplexed: PS PCIe (x1) - Endpoint or Root Complex
Lane 1	DisplayPort	Dedicated: DisplayPort 1.2a output
Lane 2	USB 3.0	Dedicated: upstream port for the 4-port USB 3.0 hub
Lane 3	SATA	Dedicated: M.2 SATA slot

2.2.4. PL-GTH Transceiver Lane Allocation (4 Lanes)

The four GTH transceivers on the Programmable Logic (PL) side are multiplexed to provide maximum flexibility for PCIe, FMC, and SFP+ connectivity. The GTR transceivers functionality is given in Table 4.

Table 4: GTH Transceiver Functionality

GTH Lane	Signal Type	Destination Interface
Lane 0-1	PCIe	PL PCIe (x2) - Endpoint or Root Complex
Lane 2-3	High-Speed	LPC FMC connector or dual SFP+ Cages

2.2.5. PCIe Operational Modes

The AMD Kria SoM PCIe Development Kit offers user-configurable operational modes to adapt to different application requirements. The board is designed with a mutually exclusive PCIe configuration between the PS and PL sides. This architecture allows the board to operate in one of two primary PCIe modes, selectable by the user. This selection is made using the SW1 slide switch as detailed in Table 5.

Note

The PCIe Endpoint function is always x1, regardless of whether it is implemented on the PS or PL side.

Note

To ensure system stability and prevent potential damage to components, all configuration switches must be set while the board is powered off. The selected configuration will take effect on the next power-on cycle.

Table 5: PCIe Mode

Switch Label	Position	PCIe Configuration
SW1	PL PCIE RC	PL Port: x2 Gen3 Root Complex
	PS PCIE EP	PS Port: x1 Gen3 Endpoint
	PL PCIE EP	PS Port: x1 Gen3 Root Complex
	PS PCIE RC	PL Port: x1 Gen3 Endpoint

2.2.5.1. Mode 1: PL as x2 Root Complex and PS x1 Endpoint

In this mode, the board acts as a host system capable of accepting a PCIe endpoint card. Detailed pinout for PCIe Root Complex is provided in Table 6. Detailed pinout for PCIe Endpoint is provided in Table 7.

- PL PCIe Port: configured as an x2 PCIe Gen3 Root Complex.
- PS PCIe Port: configured as an x1 PCIe Gen3 Endpoint.

Table 6: Pinout of PCIe Root Complex for Mode 1

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
GTH_DP0_M2C_P	J2-D9	W4	PCIe_RC_TX0_P	PCIe RC Lane 0 Data Transmit Positive
GTH_DP0_M2C_N	J2-D10	W3	PCIe_RC_TX0_N	PCIe RC Lane 0 Data Transmit Negative
GTH_DP1_M2C_P	J2-C7	U4	PCIe_RC_TX1_P	PCIe RC Lane 1 Data Transmit Positive
GTH_DP1_M2C_N	J2-C8	U3	PCIe_RC_TX1_N	PCIe RC Lane 1 Data Transmit Negative
GTH_DP0_C2M_P	J2-B9	Y2	PCIe_RC_RX0_P	PCIe RC Lane 0 Data Receive Positive
GTH_DP0_C2M_N	J2-B10	Y1	PCIe_RC_RX0_N	PCIe RC Lane 0 Data Receive Negative
GTH_DP1_C2M_P	J2-D1	V2	PCIe_RC_RX1_P	PCIe RC Lane 1 Data Receive Positive
GTH_DP1_C2M_N	J2-D2	V1	PCIe_RC_RX1_N	PCIe RC Lane 1 Data Receive Negative
GTH_REFCLK0_C2M_P	J2-C3	Y6	PCIe_RC_PL_CLK_P	PCIe RC Reference Clock Positive
GTH_REFCLK0_C2M_N	J2-C4	Y5	PCIe_RC_PL_CLK_N	PCIe RC Reference Clock Negative
HDC00_CC	J2-D52	AD15	PCIe_RC_SMCLK	PCIe RC SM Xlock
HDC08_CC	J2-C56	AC14	PCIe_RC_SMDAT	PCIe RC SM Data
HDB12	J2-B44	AD11	PCIe_RC_PERSTn	PCIe RC Reset (Active Low)
HDB14	J2-B46	AA11	PCIe_RC_WAKEn	PCIe RC Wake Signal
HDB13	J2-B45	AD10	PCIe_PRSNT2_X1	PCIe RC Present Signal

Table 7: Pinout of PCIe Endpoint for Mode 1

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
GTR_DP0_M2C_P	J1-B57	E25	PCIe_EP_TX0_P	PCIe EP Lane 0 Data Transmit Positive
GTR_DP0_M2C_N	J1-B58	E26	PCIe_EP_TX0_N	PCIe EP Lane 0 Data Transmit Negative
GTR_DP0_C2M_P	J1-A55	F27	PCIe_EP_RX0_P	PCIe EP Lane 0 Data Receive Positive
GTR_DP0_C2M_N	J1-A56	F28	PCIe_EP_RX0_N	PCIe EP Lane 0 Data Receive Negative
GTR_REFCLK3_C2M_P	J1-A51	A21	PCIe_EP_PS_CLK_P	PCIe EP Reference Clock Positive
GTR_REFCLK3_C2M_N	J1-A52	A22	PCIe_EP_PS_CLK_N	PCIe EP Reference Clock Negative
MIO24_I2C_SCK	J1-C26	AB19	PCIe_EP_SCK	PCIe EP SM Clock
MIO25_I2C_SDA	J1-C27	AB21	PCIe_EP_SDA	PCIe EP SM Data
MIO37	J1-B30	J17	PCIe_EP_PERST	PCIe EP Reset (Active Low)
MIO39	J1-B33	H19	PCIe_EP_WAKEn	PCIe EP Wake Signal
MIO36	J1-B20	K17	PRSNT_EP	PCIe EP Present Signal

2.2.5.2. Mode 2: PS as x1 Root Complex

In this mode, the board can host a smaller peripheral while exposing its main PL resources as a powerful endpoint to a host PC. Detailed pinout for PCIe Root Complex is provided in Table 8. Detailed pinout for PCIe Endpoint is provided in Table 9.

- PL PCIe Port: Configured as an x1 PCIe Gen3 Endpoint.
- PS PCIe Port: Configured as an x1 PCIe Gen3 Root Complex.

Table 8: Pinout of PCIe Root Complex for Mode 2

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
GTR_DP0_M2C_P	J1-B57	E25	PCIe_RC_TX0_P	PCIe RC Lane 0 Data Transmit Positive
GTR_DP0_M2C_N	J1-B58	E26	PCIe_RC_TX0_N	PCIe RC Lane 0 Data Transmit Negative
GTR_DP0_C2M_P	J1-A55	F27	PCIe_RC_RX0_P	PCIe RC Lane 0 Data Receive Positive
GTR_DP0_C2M_N	J1-A56	F28	PCIe_RC_RX0_N	PCIe RC Lane 0 Data Receive Negative
GTR_REFCLK3_C2M_P	J1-A51	A21	PCIe_RC_PS_CLK_P	PCIe RC Reference Clock Positive
GTR_REFCLK3_C2M_N	J1-A52	A22	PCIe_RC_PS_CLK_N	PCIe RC Reference Clock Negative
HDC00_CC	J2-D52	AD15	PCIe_RC_SMCLK	PCIe RC SM Clock
HDC08_CC	J2-C56	AC14	PCIe_RC_SMDAT	PCIe RC SM Data
MIO37	J1-B30	J17	PCIe_RC_PERSTn	PCIe RC Reset (Active Low)
MIO39	J1-B33	H19	PCIe_RC_WAKEn	PCIe RC Wake Signal
MIO36	J1-B20	K17	PRSNT_RC	PCIe RC Present Signal

Table 9: Pinout of PCIe Endpoint for Mode 2

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
GTH_DP0_M2C_P	J2-D9	W4	PCIe_EP_TX0_P	PCIe EP Lane 0 Data Transmit Positive
GTH_DP0_M2C_N	J2-D10	W3	PCIe_EP_TX0_N	PCIe EP Lane 0 Data Transmit Negative
GTH_DP0_C2M_P	J2-B9	Y2	PCIe_EP_RX0_P	PCIe EP Lane 0 Data Receive Positive
GTH_DP0_C2M_N	J2-B10	Y1	PCIe_EP_RX0_N	PCIe EP Lane 0 Data Receive Negative
GTH_REFCLK0_C2M_P	J2-C3	Y6	PCIe_EP_PL_CLK_P	PCIe EP Reference Clock Positive
GTH_REFCLK0_C2M_N	J2-C4	Y5	PCIe_EP_PL_CLK_N	PCIe EP Reference Clock Negative
MIO24_I2C_SCK	J1-C26	AB19	PCIe_EP_SCK	PCIe EP SM Clock
MIO25_I2C_SDA	J1-C27	AB21	PCIe_EP_SDA	PCIe EP SM Data
HDB12	J2-B44	AD11	PCIe_EP_PERST	PCIe EP Reset (Active Low)
HDB14	J2-B46	AA11	PCIe_EP_WAKEn	PCIe EP Wake Signal
HDB13	J2-B45	AD10	PRSNT_EP	PCIe EP Present Signal

2.2.6. FMC and SFP+ Transceiver Operational Mode

To provide maximum I/O flexibility in a compact form factor, the carrier board implements a shared architecture for two of the Kria K26 SoM's Programmable Logic (PL) high-speed transceivers. The PL-GTH transceiver lanes 2 and 3 are multiplexed between the LPC FMC connector and the dual SFP+ cages. This architecture creates a mutually exclusive configuration, meaning the user can leverage these high-speed serial lanes for either FMC-based expansion or for SFP+ networking, but not for both simultaneously. This selection is made using the SW2 slide switch as detailed in Table 10.

Table 10: FMC/SFP+ Mode

Switch Label	Position	PCIe Configuration
SW2	GTH FMC	GTH Lanes 2 & 3 are routed to the dual SFP+ cages
	GTH SFP	GTH Lanes 2 is routed to the high-speed serial pins of the LPC FMC connector

Note

To ensure system stability and prevent potential damage to components, all configuration switches must be set while the board is powered off. The selected configuration will take effect on the next power-on cycle.

2.2.7. SFP+ Mode

When selected, GTH lanes 2 and 3 are routed to the two SFP+ cages. This configuration is designed for direct fibre optic or copper-based networking applications, allowing for the implementation of protocols like 10G ethernet, Aurora, or other custom high-speed serial links. In this mode, the FMC connector's high-speed serial lanes are not available. Block diagram of SFP+ Interface is shown in Figure 4. Detailed pinout for SFP+ Interface is provided in Table 11.

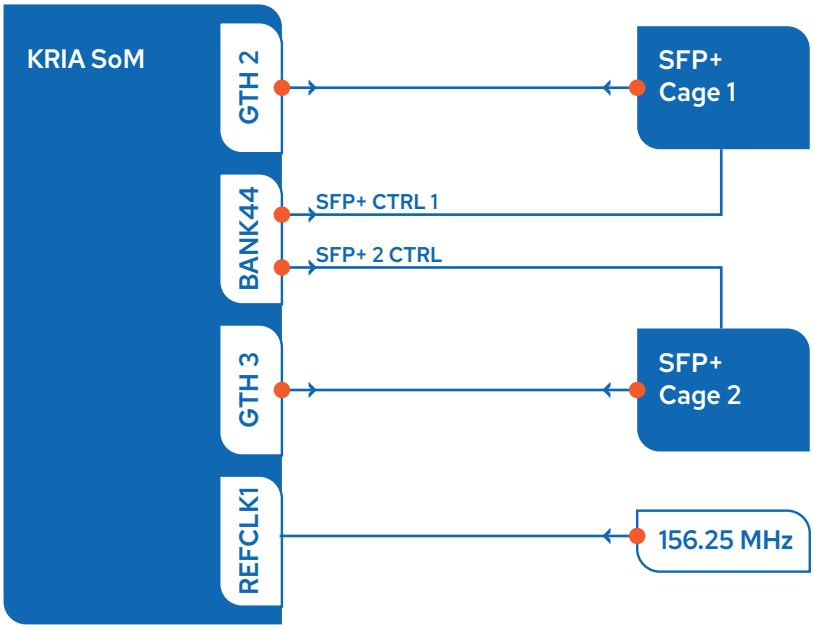


Figure 4: Block Diagram of SFP+ Interface

Table 11: Pinout of SPF+ Interface

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
GTH_DP2_M2C_P	J2-B5	R4	SFP1_TX_P	SFP+ 1 Data Transmit Positive
GTH_DP2_M2C_N	J2-B6	R3	SFP1_TX_N	SFP+ 1 Data Transmit Negative
GTH_DP2_C2M_P	J2-B1	T2	SFP1_RX_P	SFP+ 1 Data Receive Positive
GTH_DP2_C2M_N	J2-B2	T1	SFP1_RX_N	SFP+ 1 Data Receive Negative
HDC14	J2-B54	W14	SFP1_DIS	SFP+ 1 Transmit Disable
HDC15	J2-B56	W13	SFP1_LOS	SFP+ 1 Loss of Signal
HDC16_CC	J2-B57	AB15	SFP1_FLT	SFP+ 1 Transmit Fault
HDC17	J2-B58	AB14	SFP1_SCL	SFP+ 1 Serial Interface Clock
HDC18	J2-A54	Y14	SFP1_SDA	SFP+ 1 Serial Interface Data
GTH_DP3_M2C_P	J2-A3	N4	SFP2_TX_P	SFP+ 2 Data Transmit Positive
GTH_DP3_M2C_N	J2-A4	N3	SFP2_TX_N	SFP+ 2 Data Transmit Negative
GTH_DP3_C2M_P	J2-D5	P2	SFP2_RX_P	SFP+ 2 Data Receive Positive
GTH_DP3_C2M_N	J2-D6	P1	SFP2_RX_N	SFP+ 2 Data Receive Negative
HDC19	J2-A55	Y13	SFP2_DIS	SFP+ 2 Transmit Disable
HDC20	J2-A56	W12	SFP2_LOS	SFP+ 2 Loss of Signal
HDC21	J2-A58	W11	SFP2_FLT	SFP+ 2 Transmit Fault
HDC22	J2-A59	Y12	SFP2_SCL	SFP+ 2 Serial Interface Clock
HDC23	J2-A60	AA12	SFP2_SDA	SFP+ 2 Serial Interface Data
GTH_REFCLK1_C2M_P	J2-A7	V6	GTH_SFP_ REFCLK_P	SFP+ Clock Reference Positive
GTH_REFCLK1_C2M_N	J2-A8	V5	GTH_SFP_ REFCLK_N	SFP+ Clock Reference Negative

2.2.8. FMC Mode

To provide maximum system flexibility and enable a wide range of application-specific I/O, the carrier board is equipped with a standard FPGA Mezzanine Card (FMC) connector. This allows users to extend the functionality of the Kria K26 SoM by adding commercially available or custom-designed FMC boards for tasks such as high-speed data acquisition, advanced video processing, or specialized industrial interfacing. Detailed pinout of FMC is provided in Table 12.

Table 12: Pinout of FMC Mode

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name
GTH_DP2_M2C_P	J2-B5	R4	FMC_DP0_C2M_P
GTH_DP2_M2C_N	J2-B6	R3	FMC_DP0_C2M_N
GTH_DP2_C2M_P	J2-B1	T2	FMC_DP0_M2C_P
GTH_DP2_C2M_N	J2-B2	T1	FMC_DP0_M2C_N
GTH_REFCLK1_C2M_P	J2-A7	V6	FMC_GBTCLK0_M2C_P
GTH_REFCLK1_C2M_N	J2-A8	V5	FMC_GBTCLK0_M2C_N
HPB11_P	J2-B21	M6	FMC_CLK0_M2C_P
HPB11_N	J2-B22	L5	FMC_CLK0_M2C_N
HPC11_P	J2-C32	AC4	FMC_CLK1_M2C_P
HPC11_N	J2-C33	AC3	FMC_CLK1_M2C_N
HPC09_P	J2-D22	AF7	FMC_LA00_P_CC
HPC09_N	J2-D28	AF6	FMC_LA00_N_CC
HPC10_CC_P	J2-C29	AD5	FMC_LA01_P_CC
HPC10_CC_N	J2-C30	AD4	FMC_LA01_N_CC
HPC04_P	J2-D39	AB7	FMC_LA02_P
HPC04_N	J2-D40	AC7	FMC_LA02_N
HPC03_P	J2-A41	AD7	FMC_LA03_P
HPC03_N	J2-A42	AE7	FMC_LA03_N
HPC15_CC_P	J2-A38	AG4	FMC_LA04_P
HPC15_CC_N	J2-A39	AH4	FMC_LA04_N
HPC07_P	J2-B36	AH8	FMC_LA05_P
HPC07_N	J2-B37	AH7	FMC_LA05_N
HPC05_CC_P	J2-C38	AG9	FMC_LA06_P
HPC05_CC_N	J2-C39	AH9	FMC_LA06_N
HPC00_CC_P	J2-D33	AC9	FMC_LA07_P
HPC00_CC_N	J2-D34	AD9	FMC_LA07_N
HPC12_P	J2-C35	AB4	FMC_LA08_P
HPC12_N	J2-C36	AB3	FMC_LA08_N
HPC13_P	J2-B30	AD2	FMC_LA09_P
HPC13_N	J2-B31	AD1	FMC_LA09_N
HPC14_P	J2-A35	AB2	FMC_LA10_P

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name
HPC14_N	J2-A36	AC2	FMC_LA10_N
HPC08_P	J2-A29	AG6	FMC_LA11_P
HPC08_N	J2-A30	AG5	FMC_LA11_N
HPC16_P	J2-B33	AG3	FMC_LA12_P
HPC16_N	J2-B34	AH3	FMC_LA12_N
HPC06_P	J2-B27	AF8	FMC_LA13_P
HPC06_N	J2-B28	AG8	FMC_LA13_N
HPC01_P	J2-D30	AE9	FMC_LA14_P
HPC01_N	J2-D31	AE8	FMC_LA14_N
HPC17_P	J2-C26	AE3	FMC_LA15_P
HPC17_N	J2-C27	AF3	FMC_LA15_N
HPC19_P	J2-A32	AH2	FMC_LA16_P
HPC19_N	J2-A33	AH1	FMC_LA16_N
HPB_CLK0_P	J2-D18	L3	FMC_LA17_P_CC
HPB_CLK0_N	J2-D19	L2	FMC_LA17_N_CC
HPB09_P	J2-C11	K4	FMC_LA18_P_CC
HPB09_N	J2-C12	K3	FMC_LA18_N_CC
HPB16_P	J2-A23	J7	FMC_LA19_P
HPB16_N	J2-A24	H7	FMC_LA19_N
HPB03_P	J2-B24	R8	FMC_LA20_P
HPB03_N	J2-B25	T8	FMC_LA20_N
HPB13_P	J2-C20	P7	FMC_LA21_P
HPB13_N	J2-C21	P6	FMC_LA21_N
HPB06_P	J2-A20	J1	FMC_LA22_P
HPB06_N	J2-A21	H1	FMC_LA22_N
HPB04_P	J2-D21	R7	FMC_LA23_P
HPB04_N	J2-D22	T7	FMC_LA23_N
HPB00_CC_P	J2-D15	W8	FMC_LA24_P
HPB00_CC_N	J2-D16	Y8	FMC_LA24_N
HPB14_P	J2-C14	N9	FMC_LA25_P
HPB14_N	J2-C15	N8	FMC_LA25_N
HPB05_CC_P	J2-B18	L1	FMC_LA26_P
HPB05_CC_N	J2-B19	K1	FMC_LA26_N
HPB02_P	J2-C17	U8	FMC_LA27_P
HPB02_N	J2-C18	V8	FMC_LA27_N
HPB07_P	J2-B15	K2	FMC_LA28_P
HPB07_N	J2-B16	J2	FMC_LA28_N
HPB12_P	J2-A17	N7	FMC_LA29_P

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name
HPB12_N	J2-A18	N6	FMC_LA29_N
HPB01_P	J2-D12	U9	FMC_LA30_P
HPB01_N	J2-D11	V9	FMC_LA30_N
HPB08_P	J2-A14	H4	FMC_LA31_P
HPB08_N	J2-A15	H3	FMC_LA31_N
HPB15_CC_P	J2-A11	J5	FMC_LA32_P
HPB15_CC_N	J2-A12	J4	FMC_LA32_N
HPB10_CC_P	J2-B12	L7	FMC_LA33_P
HPB10_CC_N	J2-B13	L6	FMC_LA33_N
HDB18	J2-A46	W10	FMC_SCL
HDB19	J2-A47	Y10	FMC_SDA

2.2.8.1. Implementation and Key Specifications

- The connector adheres to the VITA 57.1 FPGA Mezzanine Card standard.
- The board features a Low Pin Count (LPC) connector, providing access to a substantial number of the Kria SoM's programmable logic I/O pins.
- The VADJ power rail, which supplies the I/O voltage for the FMC card's logic levels, is fixed at 1.8 V on the carrier board. This determines the electrical compatibility for any connected mezzanine card.
- 34 LVDS differential pairs (LA00-LA33) are available for general-purpose use.
- The connector provides one high-speed serial differential pair (DP0), which is routed to the Kria SoM's PL-GTH lane 2.
- Standard FMC power rails, including +12 V and +3.3 V, are supplied to the connector to power the mezzanine card.

Note

The FMC interface on this board is designed exclusively for use with mezzanine cards that support 1.8 V I/O logic levels. The VADJ voltage is not user-configurable. Attempting to use an FMC designed for a different I/O voltage (e.g., 2.5 V) may result in damage to the FMC, the carrier board, or the Kria SoM.

2.2.9. USB 3.0 Interface

To provide extensive connectivity for peripherals such as keyboards, mice, storage devices, and cameras, the carrier board features a quad-port USB 3.0 hub. This allows multiple devices to be connected simultaneously to the Kria K26 SoM, making it a versatile platform for a wide range of applications. Block diagram of USB 3.0 Interface is shown in Figure 5. Detailed pinout for USB 3.0 is provided in Table 13.

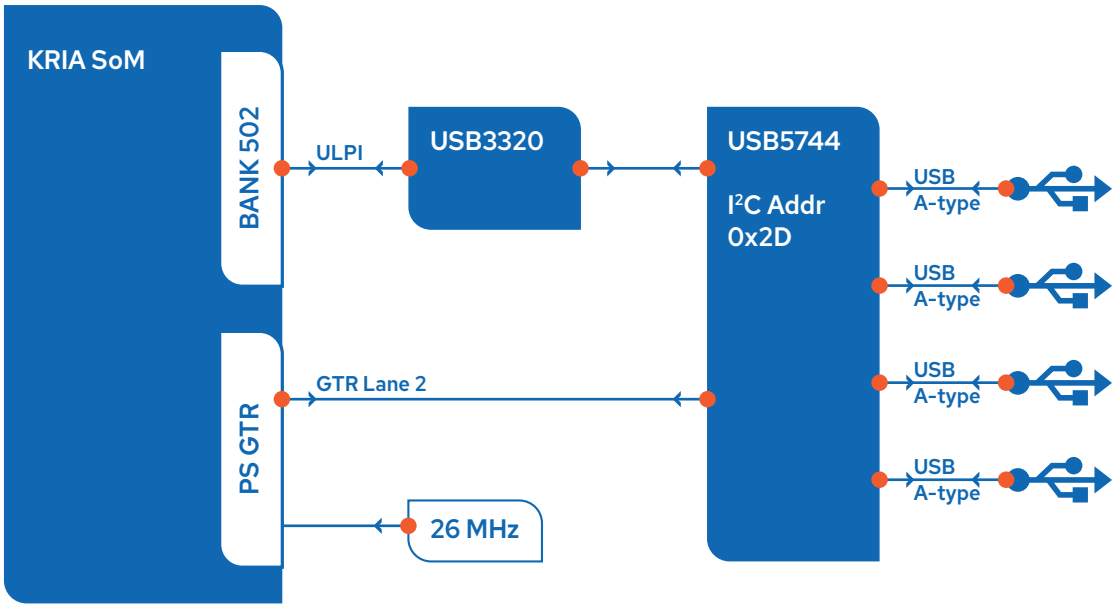


Figure 5: Block Diagram of USB Interface

Table 13: Pinout of USB Interface

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
MIO52	J1-D36	G18	OTG_CLK	USB 2.0 clock
MIO56	J1-C39	C16	OTG_DATA0	USB 2.0 data 0
MIO57	J1-C40	A16	OTG_DATA1	USB 2.0 data 1
MIO54	J1-D38	F17	OTG_DATA2	USB 2.0 data 2
MIO59	J1-B41	E17	OTG_DATA3	USB 2.0 data 3
MIO60	J1-B42	C17	OTG_DATA4	USB 2.0 data 4
MIO61	J1-A38	D17	OTG_DATA5	USB 2.0 data 5
MIO62	J1-A39	A17	OTG_DATA6	USB 2.0 data 6
MIO63	J1-A40	E18	OTG_DATA7	USB 2.0 data 7
MIO53	J1-D37	D16	OTG_DIR	USB 2.0 data direction
MIO55	J1-C38	B16	OTG_NXT	USB 2.0 next data
MIO58	J1-B40	F18	OTG_STP	USB 2.0 stop
MIO44	J1-D32	J20	OTG_RSTn	USB reset (active low)
GTR_DP2_C2M_P	J1-B53	B27	USB_3_UP_TX_P	USB 3.0 data transmit positive
GTR_DP2_C2M_N	J1-B54	B28	USB_3_UP_TX_N	USB 3.0 data transmit negative
GTR_DP2_M2C_P	J1-D57	C25	USB_3_UP_RX_P	USB 3.0 data receive positive
GTR_DP2_M2C_N	J1-D58	C26	USB_3_UP_RX_N	USB 3.0 data receive negative
GTR_REFCLK1_C2M_P	J1-B49	E21	USB_3_REF_CLK_P	USB 3.0 reference clock positive
GTR_REFCLK1_C2M_N	J1-B50	E22	USB_3_REF_CLK_N	USB 3.0 reference clock negative

2.2.9.1. Implementation and Circuitry

- The hub is implemented using the Microchip USB5744/2G, a robust 4-port SuperSpeed/High-Speed hub controller.
- The high-speed data path, responsible for 5 Gb/s SuperSpeed traffic, is connected directly to the Kria K26 SoM's Processing System PS-GTR Lane 2. This dedicated, high-performance serial link ensures maximum data throughput for USB 3.0 devices.
- For backward compatibility with USB 2.0 and 1.1 devices, the legacy data path is handled by a dedicated physical layer (PHY). The K26 SoM's integrated USB controller outputs signals via a ULPI (UTMI+ Low Pin Interface). These logic-level signals are then converted to standard USB 2.0 D+/D- electrical levels by an on-board Microchip USB3320 USB 2.0 PHY. The output of this PHY is connected to the USB5744 hub's upstream USB 2.0 port. This two-chip solution ensures reliable communication with all USB standards.
- Four standard USB Type-A connectors provide the downstream ports for peripheral connection. Each port is equipped with over-current protection to safeguard both the carrier board and the connected devices from electrical faults.
- USB5744 USB HUB I²C address is 0x2D.

2.2.10. DisplayPort Output

The carrier board is equipped with a full-size DisplayPort connector to provide high-resolution digital video output directly from the Kria K26 SoM's integrated display controller. This allows for a seamless, single-cable connection to modern monitors, industrial displays, and human-machine interfaces (HMIs). Block diagram of DisplayPort output is shown in Figure 6. Detailed pinout for DisplayPort output is provided in Table 14.

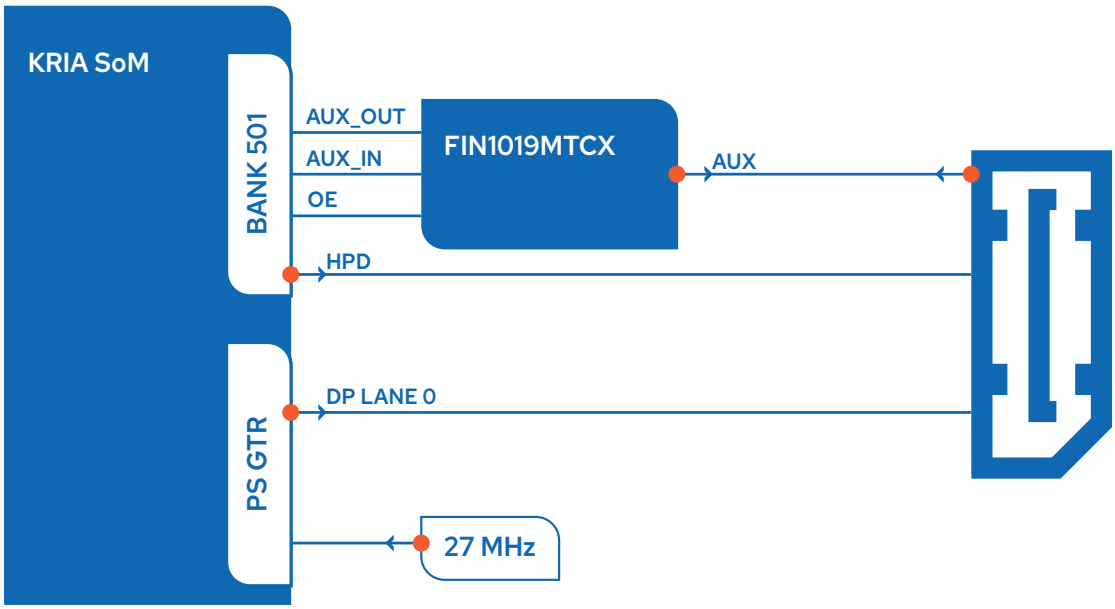


Figure 6: Block Diagram of DisplayPort Output

Table 14: Pinout of DisplayPort

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
GTR_DP1_M2C_P	J1-A47	D23	DP_LN0_P	DisplayPort Lane 0 Data Positive
GTR_DP1_M2C_N	J1-A48	D24	DP_LN0_N	DisplayPort Lane 0 Data Negative
GTR_REFCLK0_C2M_P	J1-C47	F23	DP_REF_CLK_P	DisplayPort Reference Clock Positive
GTR_REFCLK0_C2M_N	J1-C48	F24	DP_REF_CLK_N	DisplayPort Reference Clock Negative
MIO27	J1-D29	J15	DP_AUX_OUT	DisplayPort Auxiliary Data Out
MIO30	J1-C31	F16	DP_AUX_IN	DisplayPort Auxiliary Data Negative
MIO28	J1-D30	K15	DP_HPD	DisplayPort Insertion Detection
MIO29	J1-C30	G16	DP_OE	DisplayPort Auxiliary Output Enable

2.2.10.1. Implementation and Key Specifications

- A standard, full-size DisplayPort connector is provided for robust and universal connectivity.
- The interface is compliant with the DisplayPort 1.2a standard, capable of supporting resolutions such as 4K UHD (3840x2160) at 30 Hz.
- The output is configured as a single-lane (x1) DisplayPort link.
- The high-speed differential signals are driven directly by the Kria K26 SoM's Processing System PS-GTR Lane 1. This dedicated link ensures optimal signal integrity for high-quality video output.

2.2.11. M.2 SATA Interface

To accommodate high-speed, high-capacity storage, the carrier board is equipped with a standard M.2 connector. This interface is ideal for installing a solid-state drive (SSD) to host a full operating system, store large application files, or perform high-speed data logging, offering a significant performance advantage over MicroSD card storage. Block diagram of M.2 SATA is shown in Figure 7. Detailed pinout for M.2 SATA is provided in Table 15.

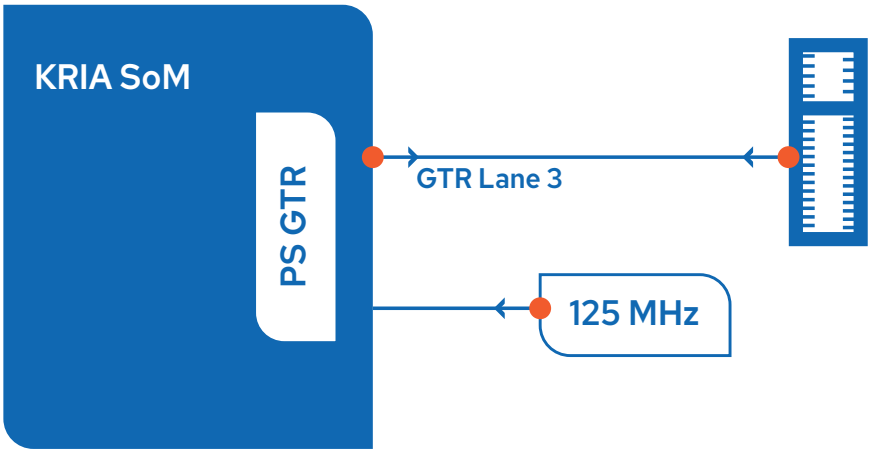


Figure 7: Block Diagram of M.2 SATA

Table 15: Pinout of M.2 SATA

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
GTR_DP3_M2C_P	J1-C51	B23	SATA_A_TX_P	SATA Data Transmit Positive
GTR_DP3_M2C_N	J1-C52	B24	SATA_A_TX_N	SATA Data Transmit Negative
GTR_DP3_C2M_P	J1-D49	A25	SATA_B_RX_P	SATA Data Receive Positive
GTR_DP3_C2M_N	J1-D50	A26	SATA_B_RX_N	SATA Data Receive Negative
GTR_REFCLK2_C2M_P	J1-D53	C21	SATA_REF_CLK_P	SATA Reference Clock Positive
GTR_REFCLK2_C2M_N	J1-D54	C22	SATA_REF_CLK_N	SATA Reference Clock Negative

2.2.11.1. Implementation and Key Specifications

- The board features a standard M.2 slot with M-Key physical keying. It provides mounting support for common 2280, 2260, and 2242 form factor modules.
- The interface is designed exclusively for the SATA III (6 Gb/s) protocol.
- The SATA signals are routed directly from the Kria K26 SoM's Processing System PS-GTR Lane 3. This provides a dedicated, high-performance serial link between the Zynq UltraScale+ MPSoC and the M.2 storage device.

2.2.12. MIPI CSI-2 Interface

To facilitate versatile computer vision and edge AI applications, the carrier board is equipped with dual MIPI CSI-2 interfaces. The first interface allows for compatibility with standard Raspberry Pi cameras, enabling prototyping with a vast ecosystem of affordable imaging sensors. The second interface allows the connection of IAS (Imager Access System) camera modules, catering to professional-grade industrial and automotive vision requirements. Both interfaces connect directly to the Kria K26 SoM's video processing pipeline, making this platform ideal for stereo vision, robotics, and real-time surveillance systems. Block diagram of MIPI CSI-2 is shown in Figure 8. Detailed pinout for Raspberry Pi Camera is provided in Table 16. Detailed pinout for IAS Camera is provided in Table 17.

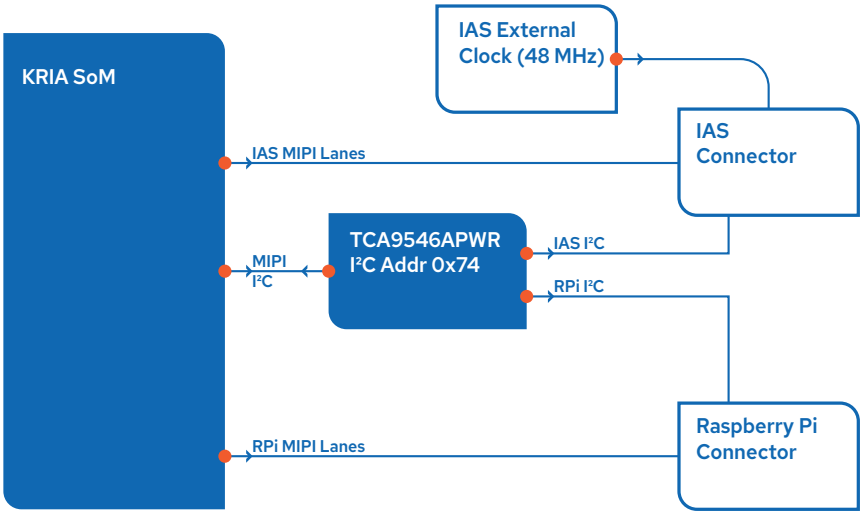


Figure 8: Block Diagram of MIPI CSI-2

Table 16: Pinout of Raspberry Pi Camera

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
HPA11_P	J1-B10	E5	MIPI_RPI0_P	RPi MIPI CSI-2 Lane 0 Data Positive
HPA11_N	J1-B11	D5	MIPI_RPI0_N	RPi MIPI CSI-2 Lane 0 Data Negative
HPA12_P	J1-A9	G6	MIPI_RPI1_P	RPi MIPI CSI-2 Lane 1 Data Positive
HPA12_N	J1-A10	F6	MIPI_RPI1_N	RPi MIPI CSI-2 Lane 1 Data Negative
HPA10_CC_P	J1-C12	D7	MIPI_RPI_CLK_P	RPi MIPI CSI-2 Clock Positive
HPA10_CC_N	J1-C13	D6	MIPI_RPI_CLK_N	RPi MIPI CSI-2 Clock Negative
HDA09	J1-A15	F11	RPI_GPIO_0	RPi General Purpose Input/Output 0
HDA10	J1-A16	J12	RPI_GPIO_1	RPi General Purpose Input/Output 1

Table 17: Pinout of IAS Camera

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
HPA06_P	J1-A3	A2	MIPI_IAS0_P	IAS MIPI CSI-2 Lane 0 Data Positive
HPA06_N	J1-A4	A1	MIPI_IAS0_N	IAS MIPI CSI-2 Lane 0 Data Negative
HPA09_P	J1-D10	D4	MIPI_IAS1_P	IAS MIPI CSI-2 Lane 1 Data Positive
HPA09_N	J1-D11	C4	MIPI_IAS1_N	IAS MIPI CSI-2 Lane 1 Data Negative
HPA07_P	J1-B7	B3	MIPI_IAS2_P	IAS MIPI CSI-2 Lane 2 Data Positive
HPA07_N	J1-B8	A3	MIPI_IAS2_N	IAS MIPI CSI-2 Lane 2 Data Negative
HPA08_P	J1-C9	B4	MIPI_IAS3_P	IAS MIPI CSI-2 Lane 3 Data Positive
HPA08_N	J1-C10	A4	MIPI_IAS3_N	IAS MIPI CSI-2 Lane 3 Data Negative
HPA05_CC_P	J1-B1	C1	MIPI_IAS_CLK_P	IAS MIPI CSI-2 Clock Positive
HPA05_CC_N	J1-B2	B1	MIPI_IAS_CLK_N	IAS MIPI CSI-2 Clock Negative
HDA02	J1-D18	J11	IAS_RESET	IAS Reset (Active Low)

2.2.12.1. Implementation and Key Specifications

- The board features dual camera inputs to support a wide range of imaging sensors: a standard 15-pin FPC connector (1.0 mm pitch) for Raspberry Pi camera compatibility, and a dedicated high-density connector compliant with the ON Semiconductor IAS module standard.
- Both interfaces are designed for the MIPI CSI-2 protocol utilizing the D-PHY physical layer. The IAS interface supports up to 4 data lanes for high-bandwidth sensors, while the Raspberry Pi interface is configured for 2 data lanes (typical) to match standard camera modules.
- The high-speed differential MIPI signals are routed directly to the Kria K26 SoM's Programmable Logic (PL) HP banks. This connection allows the implementation of the MIPI CSI-2 Receiver Subsystem (Rx) IP within the FPGA fabric for low-latency video processing.
- Dedicated I²C buses and GPIO signals (enable/reset) are provided for each interface, ensuring full support for Camera Control Interface (CCI) transactions and sensor power management.

2.2.13. MicroSD Card Slot

For system booting and secondary data storage, the carrier board is equipped with a MicroSD card slot. This interface is primarily used to host the bootloader, operating system kernel, and file system for the Kria K26 SoM. The interface is designed for reliability and compatibility with standard SD and SDHC (High Capacity) media. The block diagram of the MicroSD interface is shown in Figure 9. Detailed pinout for the MicroSD interface is provided in Table 18.

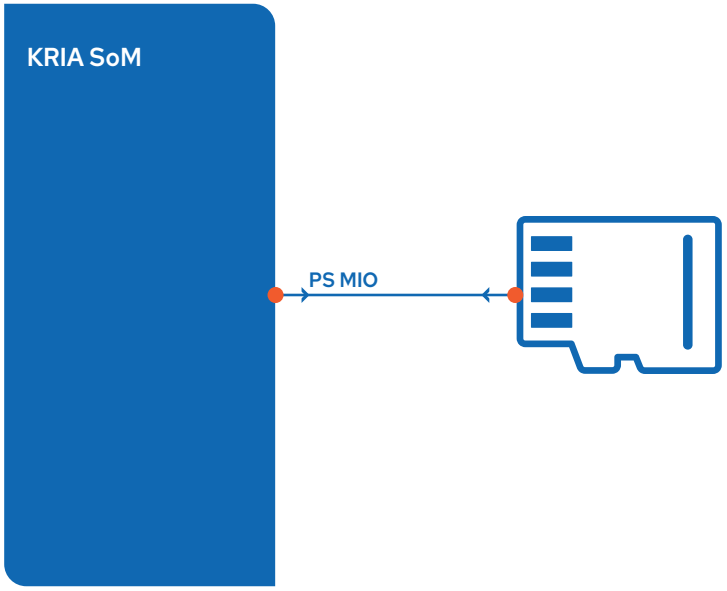


Figure 9: Block diagram of the MicroSD

Table 18: Pinout of MicroSD Card

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
MIO51	J1-B37	L21	SD_CLK	SD Card Serial Clock
MIO50	J1-B36	M19	SD_CMD	SD Card Command/Response
MIO45	J1-D33	K20	SD_CD	Card Detect (Active Low)
MIO46	J1-D34	L20	SD_DAT0	SD Card Data 0
MIO47	J1-C34	H21	SD_DAT1	SD Card Data 1
MIO48	J1-C35	J21	SD_DAT2	SD Card Data 2
MIO49	J1-C36	M18	SD_DAT3	SD Card Data 3

2.2.13.1. Implementation and Key Specifications

- The interface complies with the SD 2.0 specification and provides full support for Standard Capacity (SD) and High Capacity (SDHC) storage media with data transfer rates up to 25 MB/s.
- The circuitry is routed to the SD1 controller of the Processing System, enabling the MicroSD card to function as the primary boot source for the operating system and firmware.
- A physical Card Detect (CD) signal is connected to the SoM to provide real-time hardware notification to the software when a card is inserted or removed.

2.2.14. UART to USB Interface

The carrier board features two independent UART-to-USB bridge interfaces to facilitate system monitoring and custom logic communication. The first interface is dedicated to the Processing System (PS) and serves as the primary system console for boot-level debugging and Linux terminal access. The second interface is routed to the Programmable Logic (PL), allowing for dedicated serial communication with custom IP cores or soft-processor designs implemented within the FPGA fabric. These interfaces enable a direct connection to a host PC via USB for real-time debugging and data exchange. The block diagram of the dual UART interface is shown in Figure 10. Detailed pinout information is provided in Table 19.

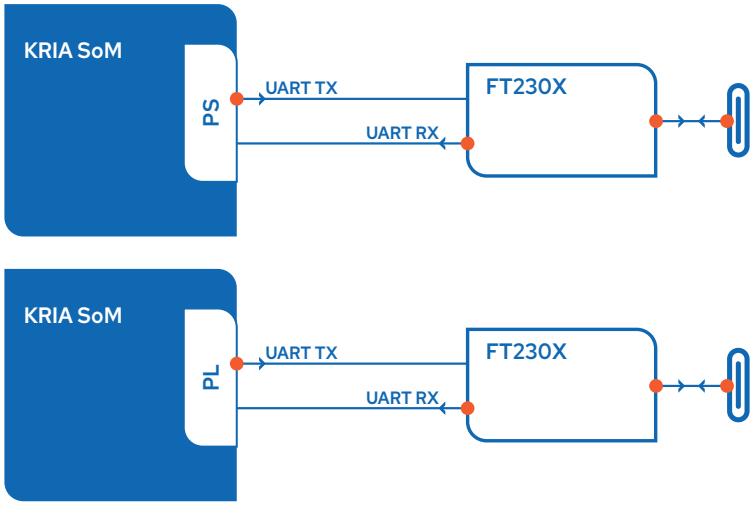


Figure 10: Block Diagram of UART to USB

Table 19: Pinout of UART to USB Interface

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
MIO43	J1-A36	K19	PS_UART_TX	PS UART Transmit
MIO42	J1-A35	L18	PS_UART_RX	PS UART Receive
HDB22	J2-A51	AB10	PL_UART_TX	PL UART Transmit
HDB23	J2-A52	AB9	PL_UART_RX	PL UART Receive

2.2.14.1. Implementation and Key Specifications

- The board utilizes high-performance UART-to-USB bridge controllers to provide serial communication over a standard USB interface.
- The PS UART interface is hard-wired to the Zynq UltraScale+ MPSoC MIO pins and is configured as the primary system console for monitoring the First Stage Bootloader (FSBL), U-Boot, and PetaLinux logs.
- The PL UART interface is connected to the High-Density (HD) I/O banks, providing a flexible serial communication channel for user-defined logic, sensor interfacing, or secondary debug ports.
- Both UART channels operate independently, allowing simultaneous access to the system console and custom PL data streams through a single or dual USB connection.
- Dedicated LED indicators are placed on the carrier board to provide visual feedback for Transmit (TX) and Receive (RX) activity on both the PS and PL channels.

2.2.15. RS-485 Serial Interface

The carrier board provides two independent RS-485 interfaces connected to the Programmable Logic (PL) via High Density (HD) I/O pins for robust, long-distance industrial communication. These ports are specifically designed for half-duplex operation, allowing the system to interface with industrial networks such as Modbus or custom multi-drop serial buses. External connections are facilitated through a high-quality 1546551-5 terminal block, ensuring secure and vibration-resistant wiring in industrial environments. The block diagram of the dual RS-485 interface is shown in Figure 11. Detailed pinout and signal mapping are provided in Table 20 and Table 21.

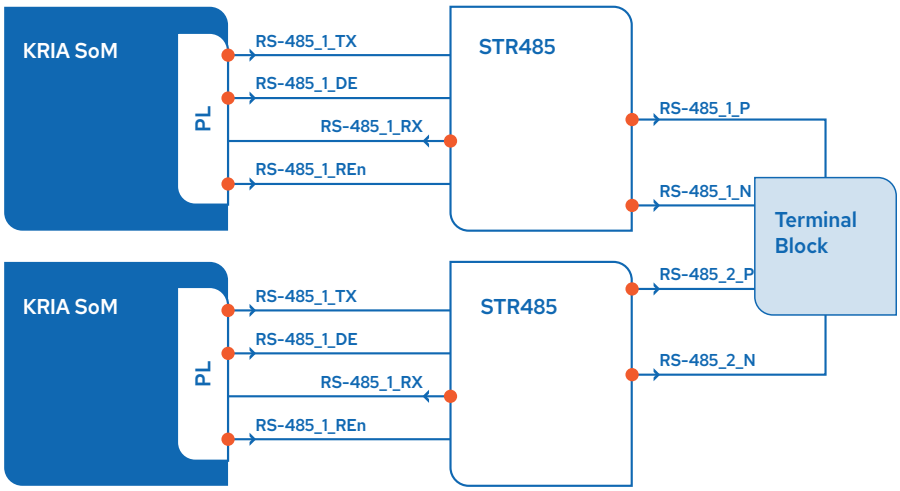


Figure 11: Block diagram of RS-485

Table 20: Pinout of RS-485

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
HDA05	J1-B18	K11	RS485_1_TX	Channel 1 Transmit
HDA06	J1-C18	H11	RS485_1_DE	Channel 1 Transmit Enable
HDA03	J1-B16	J10	RS485_1_RX	Channel 1 Receive
HDA04	J1-B17	K13	RS485_1_REn	Channel 1 Receive Enable
HDB04	J2-D49	AF11	RS485_2_TX	Channel 2 Transmit
HDA08_CC	J1-C20	F12	RS485_2_DE	Channel 2 Transmit Enable
HDA07	J1-C19	G10	RS485_2_RX	Channel 2 Receive
HDB03	J1-D48	AH10	RS485_2_REn	Channel 2 Receive Enable

Table 21: Pinout of RS-485 Connector

Terminal Pin	Signal Name	Description
1	RS485_1_N	Channel 1 Inverting Signal
2	RS485_1_P	Channel 1 Non-Inverting Signal
3	RS485_2_N	Channel 2 Inverting Signal
4	RS485_2_P	Channel 2 Non-Inverting Signal
5	GND	Ground

2.2.15.1. Implementation and Key Specifications

- Directional control for half-duplex communication is managed via dedicated Driver Enable (DE) and Receiver Enable (REn) signals, allowing the PL logic to precisely time the transition between transmitting and receiving states.
- All RS-485 signals are routed through the High Density (HD) I/O pins of the Kria K26 SoM, which are optimized for 3.3 V industrial logic standards and offer robust I/O performance.
- Each channel features an integrated 120 Ω termination resistor across the differential pair to prevent signal reflections and ensure data integrity over long cable runs.

2.2.16. CAN Bus Interface

The carrier board features a Controller Area Network (CAN) interface directly managed by the Processing System (PS) of the Kria K26 SoM. This interface is designed for high-reliability, real-time communication in industrial and automotive environments, supporting the ISO 11898 standard. By utilizing the integrated CAN controller within the Zynq UltraScale+ MPSoC, the system provides a robust communication link that is natively supported by the Linux SocketCAN framework. The block diagram of the CAN interface is shown in Figure 12. Detailed pinout and signal mapping are provided in Table 22 and Table 23.

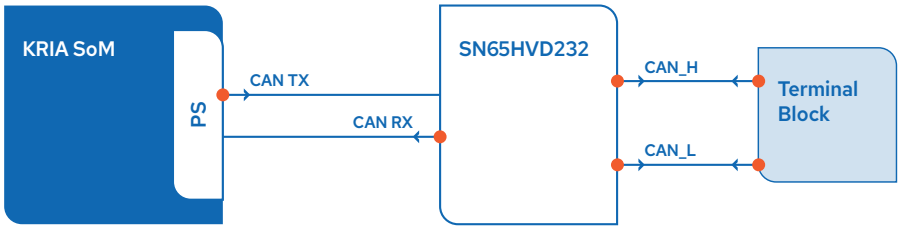


Figure 12: Block Diagram of CAN Bus

Table 22: Pinout of CAN Bus

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
MIO40	J1-B34	K18	CAN_TX	CAN Transmit Data
MIO41	J1-A34	J19	CAN_RX	CAN Receive Data

Table 23: Pinout of CAN Bus Connector

Terminal Pin	Signal Name	Description
1	CAN_H	CAN High-Level Signal
2	CAN_L	CAN Low-Level Signal
3	GND	Ground

2.2.16.1. Implementation and Key Specifications

- The interface is fully compliant with the ISO 11898 standard, providing reliable differential signaling for high-noise industrial and automotive environments.
- An onboard CAN transceiver is utilized to convert the 1.8 V MIO logic levels from the Kria K26 SoM to the differential CAN high (CAN_H) and CAN low (CAN_L) signals.
- The interface is routed to the CAN1 controller of the MPSoC's Processing System, ensuring native driver support within PetaLinux and other real-time operating systems.
- A standard 120 Ω termination resistor is integrated across the CAN_H and CAN_L lines to maintain signal integrity and prevent data corruption caused by signal reflections.
- The hardware design supports high-speed CAN communication rates up to 1 Mb/s, meeting the requirements of demanding industrial control applications.

2.2.17. PMOD Expansion Interface

To allow for modular hardware expansion, the carrier board is equipped with independent PMOD (Peripheral Module) connectors. These interfaces follow the standard 2x6 pin configuration, providing a total of 8 digital I/O pins per connector, along with dedicated power and ground rails. These ports enable the integration of a wide range of off-the-shelf modules, such as sensors, data converters, wireless transceivers, and small displays. Detailed pinout and signal mapping are provided in Table 24 and Table 25.

Table 24: Pinout of PMOD1

PMOD Pin	SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
1	HDC03	J2-D56	AE14	PMOD1_1	PMOD I/O 1
2	HDC04	J2-D57	AG14	PMOD1_2	PMOD I/O 2
3	HDC05	J2-D58	AH14	PMOD1_3	PMOD I/O 3
4	HDC09	J2-C58	AC13	PMOD1_4	PMOD I/O 4
5	–	–	–	GND	Ground
6	–	–	–	PWR_3V3	3.3V Supply Voltage
7	HDC06	J2-C54	AG13	PMOD1_5	PMOD I/O 5
8	HDC02	J2-D54	AE15	PMOD1_6	PMOD I/O 6
9	HDC01	J2-D53	AD14	PMOD1_7	PMOD I/O 7
10	HDC07	J2-C55	AH13	PMOD1_8	PMOD I/O 8
11	–	–	–	GND	Ground
12	–	–	–	PWR_3V3	3.3V Supply Voltage

Table 25: Pinout of PMOD2

Pmod Pin	SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
1	HDB16_CC	J2-B49	AB11	PMOD2_1	PMOD I/O 1
2	HDB15	J2-B48	AA10	PMOD2_2	PMOD I/O 2
3	HDB08_CC	J2-C48	AC12	PMOD2_3	PMOD I/O 3
4	HDB06	J2-C46	AH12	PMOD2_4	PMOD I/O 4
5	–	–	–	GND	Ground
6	–	–	–	PWR_3V3	3.3V Supply Voltage
7	HDB11	J2-C52	AF10	PMOD2_5	PMOD I/O 5
8	HDB10	J2-C51	AE10	PMOD2_6	PMOD I/O 6
9	HDB07	J2-C47	AH11	PMOD2_7	PMOD I/O 7
10	HDB09	J2-C50	AD12	PMOD2_8	PMOD I/O 8
11	–	–	–	GND	Ground
12	–	–	–	PWR_3V3	3.3V Supply Voltage

2.2.17.1. Implementation and Key Specifications

- The interfaces are fully compliant with the Digilent PMOD interface specification, utilizing standard 2x6 right-angle or straight female headers with 100-mil (2.54 mm) pitch.
- Each PMOD connector provides 8 individual digital I/O lines routed directly to the High-Density (HD) I/O banks of the Kria K26 SoM, supporting a wide range of user-defined logic functions.
- The I/O pins operate at a fixed 3.3 V logic level, ensuring compatibility with the vast majority of commercially available PMOD modules without the need for additional level translation.
- Dedicated 3.3 V power pins on each connector are capable of supplying current to low-power peripherals and modules directly from the carrier board's power rail.

2.2.18. Health Monitoring

The carrier board incorporates an LTC2990IMS system monitor, primarily serving as a dedicated target for I²C protocol development and bus validation. By providing a reliable 14-bit ADC interface on the I²C bus, it allows developers to exercise I²C drivers, test software polling routines. While serving as a development tool, it also provides real-time telemetry for four voltage rails and internal board temperature. Detailed pinout information is provided in Table 26. The monitored parameters are detailed in Table 27.

Table 26: Pinout of Health Monitoring

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
HDC10	J2-C59	AE13	HEALTH_SCL	Health IC Serial Clock
HDC11	J2-C60	AF13	HEALTH_SDA	Health IC Serial Data

Table 27: Monitored Parameters

Terminal Pin	Signal Name	Description
1	PWR_2V75	Power 2.75 V
2	PWR_1V8	Power 1.8 V
3	PWR_1V2	Power 1.2 V
4	PWR_3V3	Power 3.3 V
Internal	T_Internal	

2.2.18.1. Implementation and Key Specifications

- The LTC2990IMS is integrated as a functional I²C slave device to facilitate the development and testing of I²C communication stacks within U-Boot, PetaLinux, or bare-metal environments.
- To provide a consistent and predictable development target, the I²C address pins (ADR0 and ADR1) are tied to ground via pull-down resistors, fixing the device's 7-bit slave address to 0x4C.
- The inclusion of an internal temperature sensor provides an additional data point for exercising I²C read commands and testing multi-byte data transmission protocols.

2.2.19. General Purpose I²C EEPROM

The carrier board includes an 8 kbit (1024 bytes) non-volatile I²C EEPROM to provide persistent storage for critical system parameters. This memory is ideal for storing board-specific information such as serial numbers, hardware revision data, MAC addresses, and user-defined configuration settings. The EEPROM is connected to the same I²C bus as the platform management bus*, ensuring easy access from the Kria K26 Processing System (PS). Detailed pinout is provided in Table 28.

Table 28: Pinout of EEPROM

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
MIO24_I2C_SCK	J1-C26	AB19	MIO24_I2C_SCK	PS I²C Clock Output
MIO25_I2C_SDA	J1-C27	AB21	MIO25_I2C_SDA	PS I²C Serial Data

2.2.20. System Watchdog Timer

To enhance system reliability and provide automatic recovery from software hangs or processor lockups, the carrier board features a dedicated hardware watchdog timer based on the TPS3430WDRCR. This high-accuracy programmable timer monitors a "heartbeat" signal from the Kria K26 SoM; if the signal is not received within a predefined window, the watchdog triggers a system-wide reset. The block diagram of the watchdog circuit is shown in Figure 13. Detailed signal mapping is provided in Table 29.

*For more information, please refer to the Kria K26 SoM Datasheet (DS987).

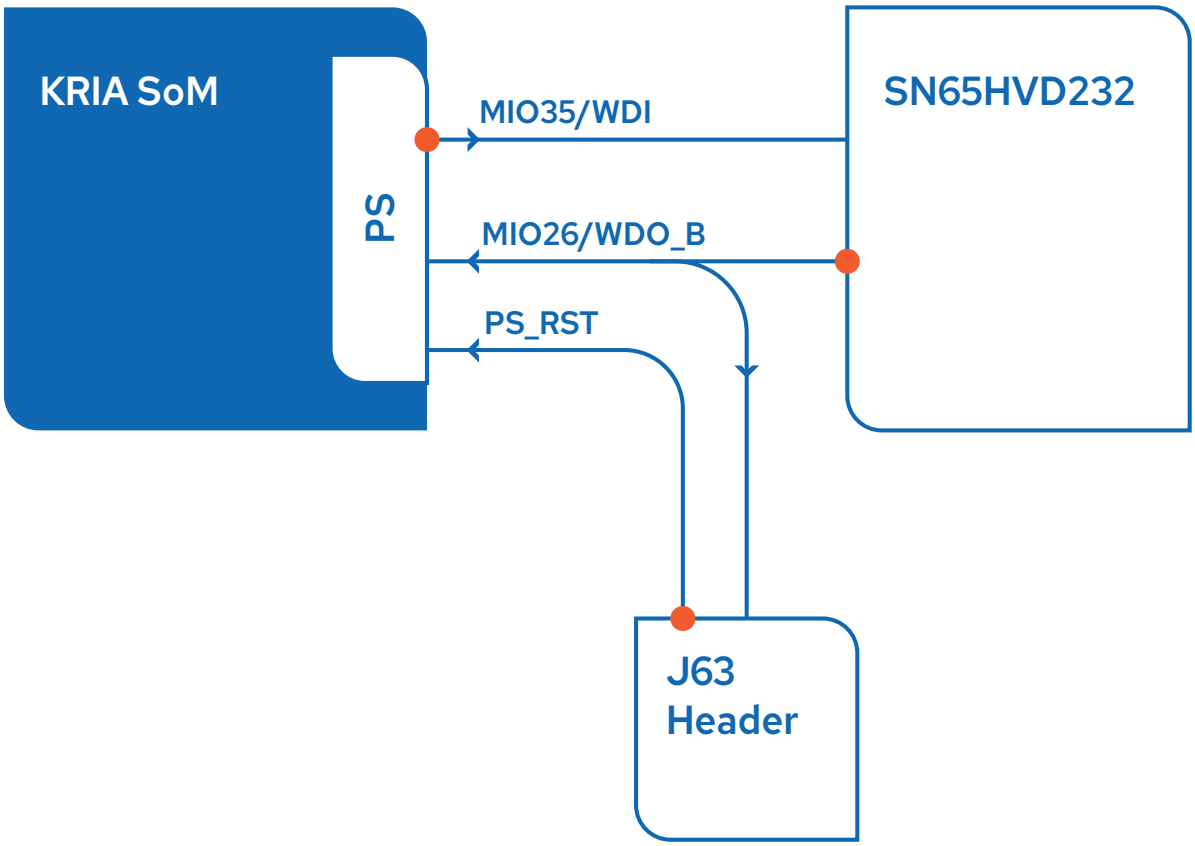


Figure 13: Block Diagram of WDT

Table 29: Pinout of Watchdog Timer

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
MIO35	J1-B28	H17	MIO35_WD_OUT	Watchdog Input (WDI) - Heartbeat from PS
MIO26	J1-D28	L15	MIO26	Watchdog Status / Monitor Pin
PS_SRST_C2M_L	J1-C16	N19	PS_SRST_C2M_L	System Soft Reset (Active Low)

2.2.20.1. Implementation and Key Specifications

- The system utilizes a high-precision TPS3430WDRCR hardware watchdog timer to ensure automatic recovery and high availability in the event of processor hangs or software lockups.
- A dedicated heartbeat signal is routed from MIO35 of the Processing System to the WDI pin of the watchdog, requiring periodic software toggling to prevent a system-wide reset.
- The active-low watchdog output (WDO_B) is linked to the PS_SRST_C2M_L line, enabling the circuit to initiate a hardware-level soft reset if the heartbeat signal is not received within the defined window.
- The design incorporates a 3-pin debug header (J63) that allows for physical isolation of the reset signal, enabling developers to disable the watchdog's reset capability during software debugging or firmware updates.
- Real-time status monitoring of the watchdog output is provided through MIO26, allowing the Kria K26 SoM to perform internal diagnostics and log reset events for predictive maintenance.

2.2.21. Fan Control Interface

To maintain optimal operating temperatures for the Kria K26 SoM under heavy workloads, the carrier board includes a dedicated 12 V fan control circuit. This interface allows the Programmable Logic (PL) to dynamically manage cooling through a low-side switching architecture. Detailed pinout is provided in Table 30.

Table 30: Pinout of Fan Control Interface

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
HPC02_P	J2-D36	AB8	HPC02_P	FAN PWM/Enable Control

2.2.22. User Interface (LEDs, Button and Switch)

To facilitate user interaction and system status monitoring, the carrier board is equipped with two general-purpose LEDs, one tactile push button, and one slide switch. These components are routed directly to the Programmable Logic (PL) section of the Kria K26 SoM, allowing for user-defined functionality such as status indication, mode selection, or manual triggers. Detailed signal mapping is provided in Table 31.

Table 31: Pinout of User Interface

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
HDB02	J2-D46	AG10	HDB02	User LED 1 Control
HDB05	J2-D50	AG11	HDB05	User LED 2 Control
HPB17_P	J2-D24	K8	HPB17_P	User Slide Switch Input
HPB17_N	J2-D35	K7	HPB17_N	User Push Button Input

2.2.23. Boot Modes

The carrier board provides a user-configurable boot mode interface to determine the primary boot source for the Kria K26 SoM. This is implemented via a 4-position DIP switch connected to the PS_MODE[0:3] pins of the Zynq UltraScale+ MPSoC. By adjusting the switch positions, developers can toggle between different boot targets such as SD card, QSPI flash, or JTAG for debugging. Detailed switch mapping and boot mode settings* are provided in Table 32.

Table 32: Boot Mode Settings

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
JTAG Mode	Low (0)	Low (0)	Low (0)	Low (0)
QSPI Mode	High (1)	Low (0)	Low (0)	Low (0)
SD0	High (1)	High (1)	Low (0)	Low (0)
SD1	High (1)	Low (0)	High (1)	Low (0)
eMMC	Low (0)	High (1)	High (1)	Low (0)

2.2.24. Electrical Specifications

2.2.24.1. Power Supply Requirements

The carrier board is powered through a high-current Molex 0457320001 vertical connector, designed to provide a secure and stable 12 V DC input. Front view of the power connector is provided in Figure 14. Detailed pinout of power connector is provided on Table 33.

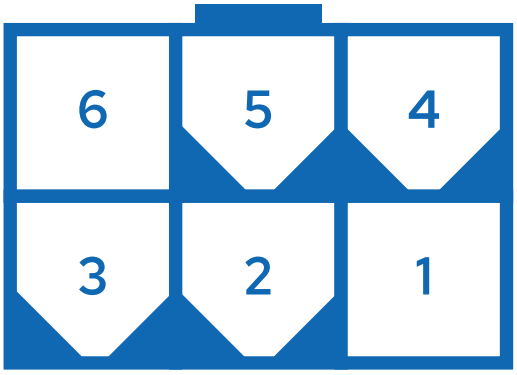


Figure 14: Front View of Power Connector

Table 33: Pinout of Power Connector

Pin Number	Signal Name
1	ATX_12V
2	ATX_12V
3	ATX_12V
4	GND
5	GND
6	GND

*For more information, please refer to the Zynq Ultrascale+ Device Technical Reference Manual (UG1085).

For primary circuit protection, a 15 A fuse is integrated at the input stage to safeguard the Kria K26 SOM and onboard peripherals against overcurrent conditions. System power is controlled via a physical DIP switch, which serves as the main power-on/off mechanism for the entire board infrastructure. The power supply requirements of the DE160100 are given in Table 34.

Table 34: Electrical Specifications

Specification	Min	Typical	Max	Units
Supply Voltage (PWR_12V)	11.4	12	12.6	V
Supply Current (PWR_12V)	–	–	10	A

Note

Refer to Kria K26 SoM Datasheet (DS987) for more information about K26 SoM Power management and electrical characteristics.

2.2.25. Physical Specifications

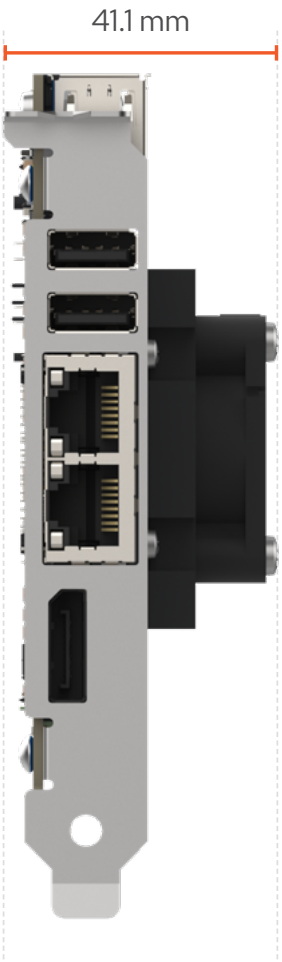


Figure 15: Dimensions of Front Panel

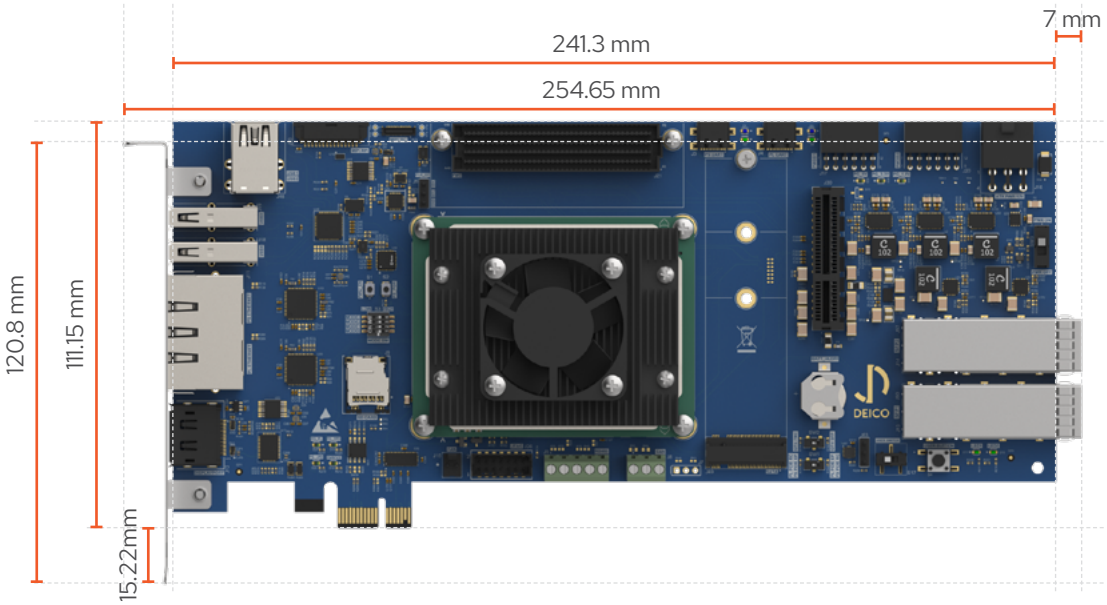


Figure 16: Dimensions of Board

2.2.26. Environmental Specifications

DE160100 environmental specifications are given in Table 35.

Table 35: Environmental Specifications

Parameter	Condition	Value
Operating Humidity	Relative, non-condensing	10% - 90%
Storage Humidity	Relative, non-condensing	5% - 95%
Operating Temperature	Forced-air cooling from chassis	0 °C - +55 °C
Storage Temperature	–	0 °C - +70 °C

3. Interface Connections and Locations

The following figure and table provide an overview of the physical layout and the locations of the key connectors, switches, and interface components on the carrier board. This guide serves as a quick reference for board setup and hardware integration.

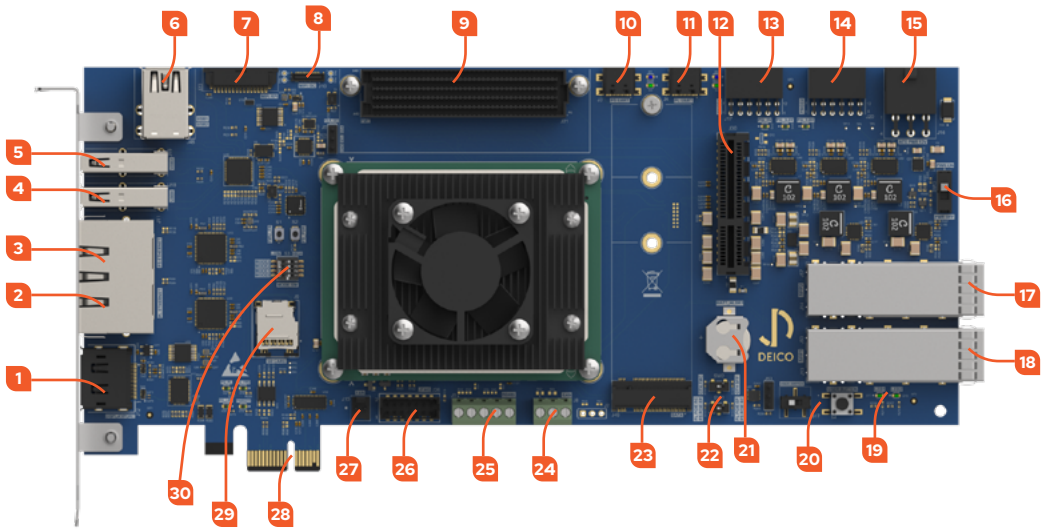


Figure 17: Interface Connections and Locations of DE160100

Table 36: Interface Connections and Locations of DE160100

1	DisplayPort Connector	16	Power Switch
2	PL Ethernet	17	SFP+ Cage 2
3	PS Ethernet	18	SFP+ Cage 1
4	USB 3.0 Port 4	19	User LEDs
5	USB 3.0 Port 3	20	User Switches
6	USB 3.0 Port 1-2	21	RTC Battery
7	MIPI RPi Connector	22	GT Configuration Switches
8	MIPI IAS Connector	23	M.2 SATA Connector
9	FMC	24	CAN Bus Connector
10	PS UART	25	RS-485 Connector
11	PL UART	26	JTAG Connector
12	PCIe Root Complex	27	Fan Connector
13	PMOD1	28	PCIe Endpoint
14	PMOD2	29	MicroSD Card Slot
15	ATX Power Connector	30	Mode Switches

4. Safety Guidelines

The DE160100 shall not be operated in any manner not specified in this document. Misuse of the product may result in a hazard. Safety protection features may be compromised if the product is damaged. In the event of damage, the product shall be returned for repair.

5. Compatibility Guidelines

This product has been tested and found to comply with the applicable regulatory requirements and limits for electromagnetic compatibility (EMC). These requirements and limits are intended to provide reasonable protection against harmful interference when the product is operated within the specified electromagnetic environment.

This product is intended for use in industrial locations. However, harmful interference may occur in certain installations if the product is connected to peripheral devices or test objects, or if it is used in residential or commercial areas. To minimize interference with radio and television reception and to prevent unacceptable performance degradation, the product shall be installed and operated in strict accordance with the instructions specified in the product documentation.

Any changes or modifications to the product not expressly approved by DEICO may void the user's authority to operate the equipment under local regulatory rules.

To ensure the specified EMC performance, the product shall be operated only with shielded cables and accessories.

To ensure the specified EMC performance, the length of any cable attached to the front connectors shall not exceed 3 m (10 ft.).