MIXED SIGNAL FRONT END

ULTRA-LOW POWER 64 GSPS DUAL CHANNEL 0.1 - 32 GHZ

The FMC JARIET is an FMC per VITA 57.1 specification in LF (Long-Form) form factor. The FMC JARIET has a single Electra MX Device from Jariet Technologies which provides Dual DAC at 64 GSPS/10-bit and Dual ADC at 64 GSPS/10-bit. The ADC has 32 GHz Analog Input full power bandwidth (-3db). The DAC has a useable Analog bandwidth of 32GHz.

The FMC JARIET interfaces via 16 lanes of JESD204B/JESD204C to the host carrier (note for max performance JESD204C with speed of 32 Gbps is utilized). The module has a direct RF sampling clock option up to 32 GHz clock input. The module has 6 SMPM Connectors for its ADC/DACs and Sampling Clock Input.

These features facilitate the development of complex RF solutions and applications such as:

- Satellite Communications
- Phased Array Antennas
- EW/EA Systems
- Wideband RF Record and Playback
- Spectrum Monitoring
- 5G/6G Wireless
- Test & Measurement

www.depelsys.it
info@depelsys.it
Office: +39 0694015099
Direct: +39 3664443303

Viale Balilla 9/10/11 00044
Frascati (Rome) - Italy

REGIONE LAZIO

LAZIO INNOVA

Product Specifications

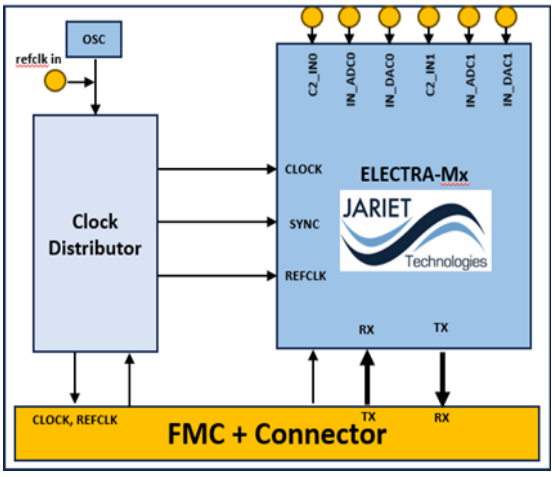
Architecture		
Physical	**Dimensions**	Single Module
		Width: 4.475" × 2.716" (113.69mm × 69 mm)
		Depth: 0.0798" (2.02mm)
Type	**FMC**	Dual ADC/DAC
Configuration		
Power	**FMC JARIET**	13W
Environmental	**Temperature**	Industrial: -40°C to +85°C
	Altitude	40,000 ft non-operating
	Relative Humidity	10 to 90% non-condensing
Front Panel	**Interface Connectors**	Six 50Ω RF SMPM
Software Support	**Operating System**	Agnostic
Other		
Warranty		Two (2) years

RF TX/RX Specifications

RF RECEIVER SPECIFICATIONS	
Sampling Rate (Fs)	40 to 64 GS/s
No. Of Receivers	2
Analog Bandwidth	Up to 32 GHz
Broad instantaneous bandwidth	Up to 6.4 GHz
Decimation	From 8 to 1024
Resolution	10 Bits in Full Nyquist

RF TRANSMITTER SPECIFICATIONS	
Sampling Rate (Fs)	40 to 64 GS/s
No. Of Transmitters	2
Output Frequency	Up to Fs/2 GHz in 1st Nyquist Zone
	From Fs/2 to 32 GHz in 2nd Nyquist Zone
Interpolation	From 8 to 1024
Resolution	10 Bits in full-Nyquist

Block Diagram

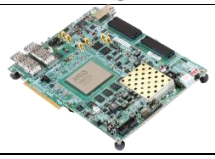
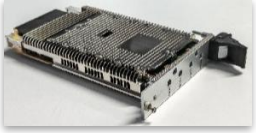


Clocking Options

CLOCKING OPTIONS
Software-selectable ADC/DAC clock source
External/Internal Reference Clock
External/Internal Sampling Clock
Internal PLL Option

All ADCs and DACs across multiple mezzanine cards can be synchronized using an external Clock Distribution Boards (Under Development).

Supported Hardware

	AMD VCK190 Evaluation Board
	AMD VCU128 HBM Evaluation Board
	AMD VCU118 Evaluation Board
	D&P FPGA Carrier with VC1502 Versal Device

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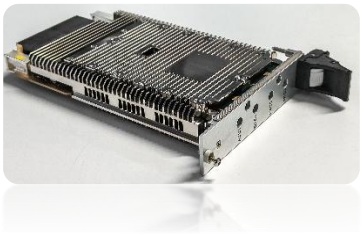
Related Products



- FPGA Carrier with VC1502 Versal Device & FMC JARIET Board
- Air Cooled and Conduction Cooled Mechanical Frames Options

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Direct: +39 3664443303

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