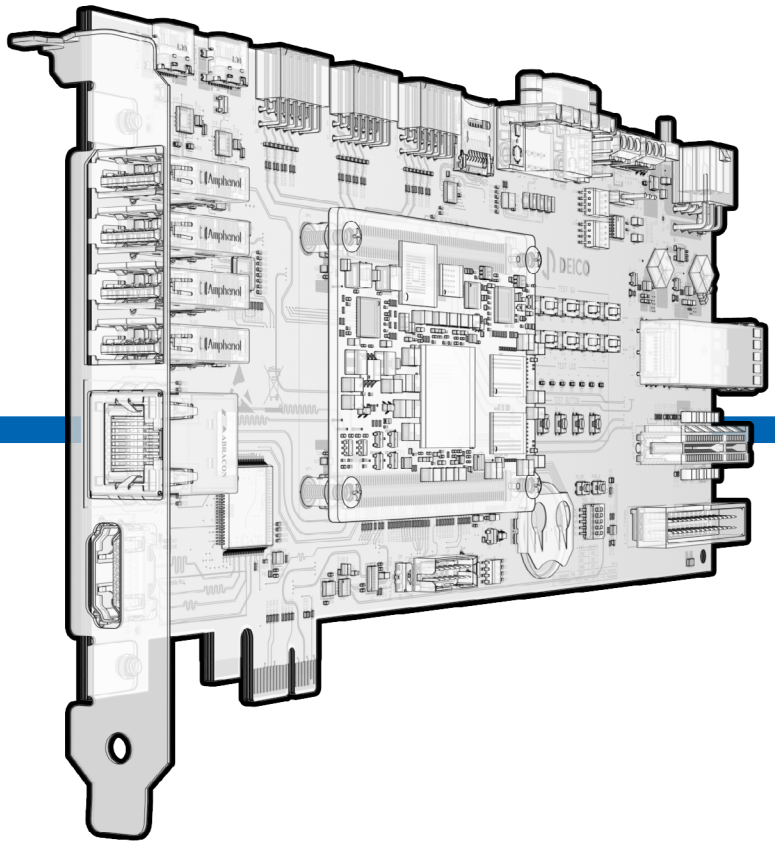
Datasheet



DE13310

Zynq SoM Carrier Board

DEICO

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1. Description

The DE13310 Zynq SoM Carrier Board is designed for integration with the DE13210 Zynq-7015 System on Module (SoM). It provides a comprehensive set of peripherals and high-speed interfaces for embedded control and data acquisition applications.

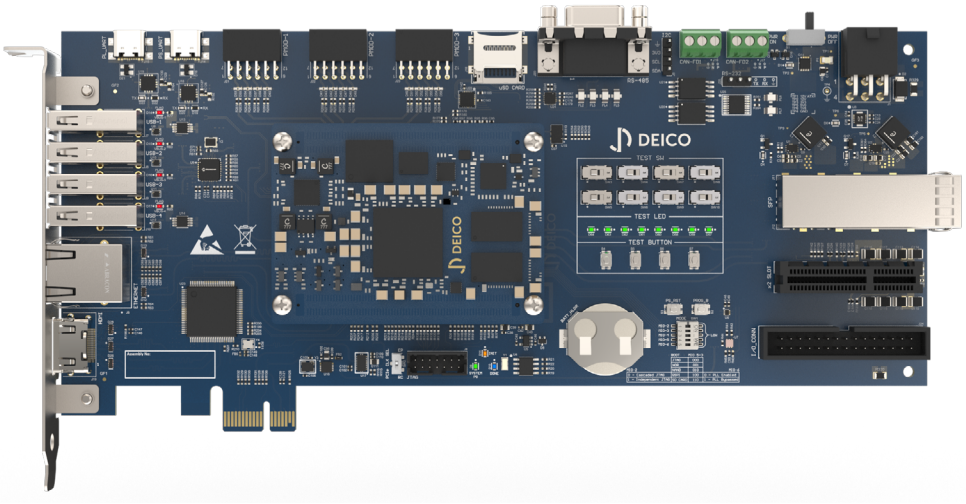


Figure 1: General View of the DE13310 Board

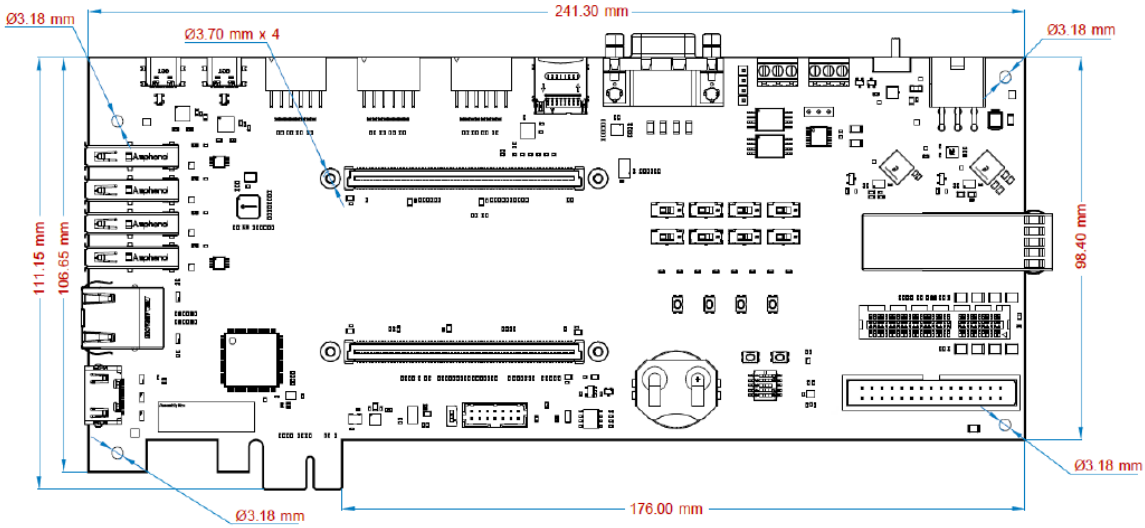


Figure 2: Controller Board Dimensions

2. Hardware Overview

2.1. Processing

The carrier board hosts a Xilinx Zynq-7015 SoC, which integrates a dual-core ARM Cortex-A9 processor and programmable FPGA logic. The processor runs at 667 MHz and supports real-time control and parallel processing tasks.

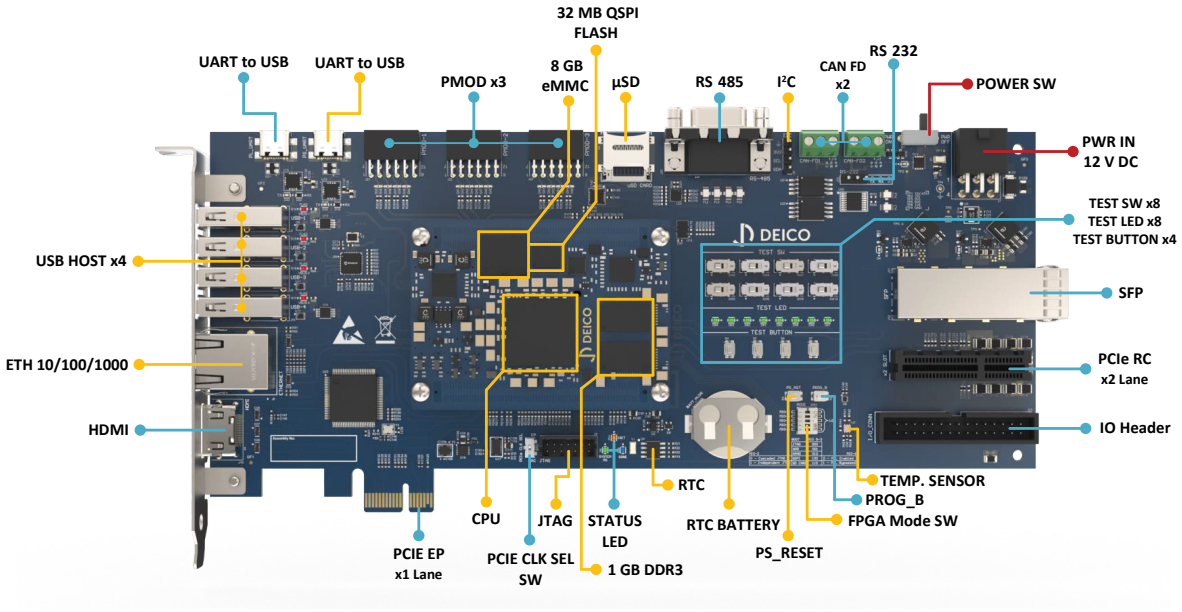


Figure 3: Full Component Layout of the DE13310

2.2. Memory & Storage

- 1 GB DDR SDRAM (2 x 512 MB, 32-bit interface)
- 8 GB eMMC flash
- 32 MB QSPI flash
- 1 x µSD card socket

2.3. Communication Interfaces

- 1 x 10/100/1000 Mb/s ethernet
- 4 x USB 2.0 host
- 2 x CAN FD
- 1 x UART-to-USB (Type-C)
- 1 x RS-232 (2.54 mm, 3-pin header)
- 1 x RS-485 (DSUB-9)
- 1 x I²C header (2.54 mm, 4-pin)

2.4. Video & Display

- 1 x HDMI interface (with support for HDMI 1.4 features)
- Audio Return Channel (ARC)
- 3D video support
- 12-bit deep color @ 1080p
- RGB, YCbCr, and DDR formats

2.5. Expansion & I/O

- 3 x PMOD connectors
- 1 x SFP transceiver cage
- 2 x PCIe interface:
  - x2 Lane Root Complex
  - x1 Lane Endpoint
- 1 x 30-pin GPIO header (2.54 mm pitch)
- 2 x 140-pin board-to-board connectors (0.8 mm pitch)

2.6. User Interface & Debug

- 8 x test LEDs
- 8 x test switches
- 4 x test buttons
- 2 x user buttons: PS_RST, PROG_B
- 3 x status LEDs: FPGA_DONE, FPGA_INIT, PG
- 1 x 14-pin JTAG header (2.00 mm pitch)
- DIP switches for boot mode and PCIe configuration

2.7. Power & Thermal

- Input voltage: 12 V (via 3 x 2 pin ATX connector)
- PCB: 10-layer, 1.6 mm thickness
- Operating temperature: 0 °C - +40 °C

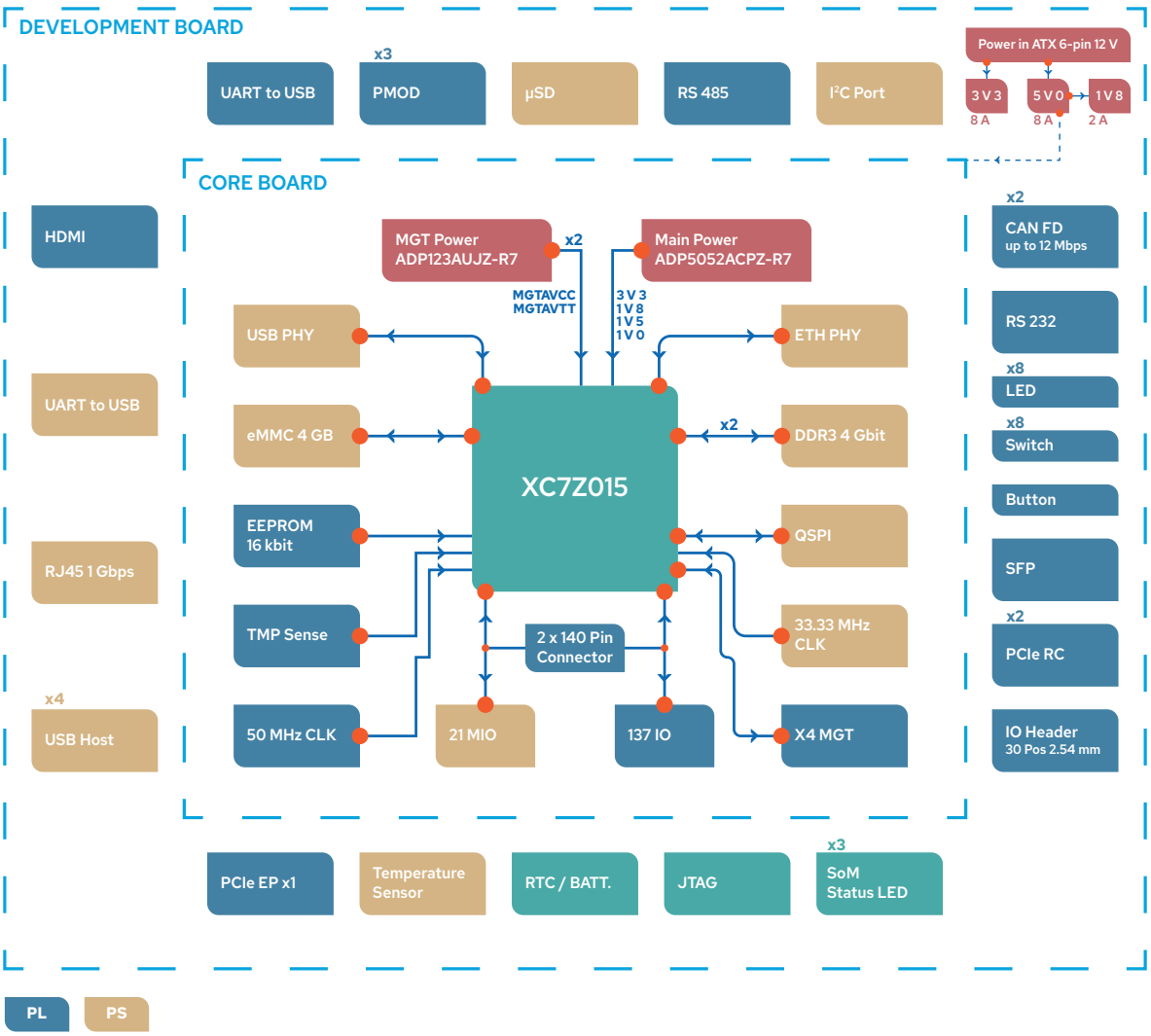


Figure 4: Controller Board Function Block Diagram

Table 1: Controller Board Pin Map

Function	SoC Pin Name	Bank	Ball	Net Name	J2		Net Name	Ball	Bank	SoC Pin Name	Function
5V DC Input				VCC_5V0	1	2	VCC_5V0				5V DC Input
5V DC Input				VCC_5V0	3	4	VCC_5V0				5V DC Input
Ground				GND	5	6	GND				Ground
Ethernet Data 0 Positive				ETH_MD0_P	7	8	GND				Ground
Ethernet Data 0 Negative				ETH_MD0_N	9	10	ETH_MD1_P				Ethernet Data 1 Positive
Ground				GND	11	12	ETH_MD1_N				Ethernet Data 1 Negative
Ethernet Data 2 Positive				ETH_MD2_P	13	14	GND				Ground
Ethernet Data 2 Negative				ETH_MD2_N	15	16	ETH_MD3_P				Ethernet Data 3 Positive

Function	SoC Pin Name	Bank	Ball	Net Name	J2		Net Name	Ball	Bank	SoC Pin Name	Function
Ground				GND	17	18	ETH_MD3_N				Ethernet Data 3 Negative
USB Data +				OTG_D_P	19	20	GND				Ground
USB Data -				OTG_D_N	21	22	PS_MIO52	D13	BANK501	PS_MIO52_501	Unused
Ground				GND	23	24	PS_MIO53	C11	BANK501	PS_MIO53_501	Unused
USB OTG ID				OTG_ID	25	26	ETH_LED0				Ethernet Link LED
USB VBUS				OTG_VBUS	27	28	ETH_LED1				Ethernet Status LED
HDMI_HD_SPDIF	IO_0_35	BANK35	H6	IO_B35_0	29	30	OTG_CPEN				Unused
HDMI_HD_VSYNC	IO_L3P_T0_DQS_AD1P_35	BANK35	E8	IO_B35_L3_P	31	32	GND				Ground
HDMI_HD_HSYNC	IO_L3N_T0_DQS_AD1N_35	BANK35	D8	IO_B35_L3_N	33	34	IO_B35_L4_P	G8	BANK35	IO_L4P_T0_35	HDMI_DATA16
HDMI_HD_DE	IO_L7P_T1_AD2P_35	BANK35	C8	IO_B35_L7_P	35	36	IO_B35_L4_N	G7	BANK35	IO_L4N_T0_35	HDMI_DATA18
HDMI_DATA14	IO_L7N_T1_AD2N_35	BANK35	B8	IO_B35_L7_N	37	38	IO_B35_L1_P	F7	BANK35	IO_L1P_T0_AD0P_35	HDMI_DATA20
HDMI_DATA12	IO_L6P_T0_35	BANK35	G6	IO_B35_L6_P	39	40	IO_B35_L1_N	E7	BANK35	IO_L1N_T0_AD0N_35	HDMI_DATA22
HDMI_DATA10	IO_L6N_T0_VREF_35	BANK35	F6	IO_B35_L6_N	41	42	IO_B35_L12_P	D5	BANK35	IO_L12P_T1_MRCC_35	HDMI_CLK
Ground				GND	43	44	IO_B35_L12_N	C4	BANK35	IO_L12N_T1_MRCC_35	HDMI_OUT_SDA
HDMI_DATA5	IO_L10P_T1_AD11P_35	BANK35	A5	IO_B35_L10_P	45	46	GND				Ground
HDMI_DATA7	IO_L10N_T1_AD11N_35	BANK35	A4	IO_B35_L10_N	47	48	IO_B35_L13_P	B4	BANK35	IO_L13P_T2_MRCC_35	HDMI_OUT_SCL
HDMI_DATA9	IO_L8P_T1_AD10P_35	BANK35	B7	IO_B35_L8_P	49	50	IO_B35_L13_N	B3	BANK35	IO_L13N_T2_MRCC_35	HDMI_DATA2
HDMI_DATA4	IO_L8N_T1_AD10N_35	BANK35	B6	IO_B35_L8_N	51	52	IO_B35_L14_P	D3	BANK35	IO_L14P_T2_AD4P_SRCC_35	HDMI_DATA1
Ground				GND	53	54	IO_B35_L14_N	C3	BANK35	IO_L14N_T2_AD4N_SRCC_35	HDMI_DATA0
HDMI_DATA15	IO_L11P_T1_SRCC_35	BANK35	C6	IO_B35_L11_P	55	56	IO_B35_L5_P	F5	BANK35	IO_L5P_T0_AD9P_35	HDMI_DATA17
HDMI_DATA13	IO_L11N_T1_SRCC_35	BANK35	C5	IO_B35_L11_N	57	58	IO_B35_L5_N	E5	BANK35	IO_L5N_T0_AD9N_35	HDMI_DATA19
Power Supply pins for the output drivers of BANK35	VCCO_35			VCCO_BANK35	59	60	VCCO_BANK35			VCCO_35	Power Supply pins for the output drivers of BANK35
Ground				GND	61	62	GND				Ground
HDMI_DATA11	IO_L9P_T1_DQS_AD3P_35	BANK35	A7	IO_B35_L9_P	63	64	IO_B35_L20_P	G4	BANK35	IO_L20P_T3_AD6P_35	HDMI_DATA21
HDMI_DATA6	IO_L9N_T1_DQS_AD3N_35	BANK35	A6	IO_B35_L9_N	65	66	IO_B35_L20_N	F4	BANK35	IO_L20N_T3_AD6N_35	HDMI_DATA23
HDMI_DATA8	IO_L2P_T0_AD8P_35	BANK35	D7	IO_B35_L2_P	67	68	IO_B35_L16_P	D1	BANK35	IO_L16P_T2_35	HDMI_INT
HDMI_DATA3	IO_L2N_T0_AD8N_35	BANK35	D6	IO_B35_L2_N	69	70	IO_B35_L16_N	C1	BANK35	IO_L16N_T2_35	HDMI_SPDIF_OUT
TEST SWITCH	IO_L15P_T2_DQS_AD12	BANK35	A2	IO_B35_L15_P	71	72	IO_B35_L17_P	E2	BANK35	IO_L17P_T2_AD5P_35	TEST SWITCH
TEST SWITCH	IO_L15N_T2_DQS_AD12	BANK35	A1	IO_B35_L15_N	73	74	IO_B35_L17_N	D2	BANK35	IO_L17N_T2_AD5N_35	TEST SWITCH
Ground				GND	75	76	GND				Ground
TEST SWITCH	IO_L18P_T2_AD13P_35	BANK35	B2	IO_B35_L18_P	77	78	IO_B35_L21_P	E4	BANK35	IO_L21P_T3_DQS_AD14P_35	PCIe-EP

Function	SoC Pin Name	Bank	Ball	Net Name	J2		Net Name	Ball	Bank	SoC Pin Name	Function
TEST SWITCH	IO_L18N_T2_AD13N_35	BANK35	B1	IO_B35_L18_N	79	80	IO_B35_L21_N	E3	BANK35	IO_L21N_T3_DQS_AD14N_35	PCIe-EP
Ground				GND	81	82	IO_B35_L22_P	G3	BANK35	IO_L22P_T3_AD7P_35	PCIe-EP
TEST SWITCH	IO_L23P_T3_35	BANK35	F2	IO_B35_L23_P	83	84	IO_B35_L22_N	G2	BANK35	IO_L22N_T3_AD7N_35	PCIe-EP
TEST SWITCH	IO_L23N_T3_35	BANK35	F1	IO_B35_L23_N	85	86	IO_B35_L19_P	H4	BANK35	IO_L19P_T3_35	PCIe-EP
TEST LED	IO_L24P_T3_AD15P_35	BANK35	H1	IO_B35_L24_P	87	88	IO_B35_L19_N	H3	BANK35	IO_L19N_T3_VREF_35	SFP / EP CLK SW SELECT
TEST LED	IO_L24N_T3_AD15N_35	BANK35	G1	IO_B35_L24_N	89	90	IO_B35_25	H5	BANK35	IO_25_35	Active Low : SFP / EP CLK SW Output Enable
Ground				GND	91	92	GND				Ground
Unused	VCCADC_0		K12	XADC_VCC	93	94	TCK	H11	BANK0	TCK_0	JTAG Test Clock
Unused	VP_0		L12	XADC_IN0_P	95	96	TMS	H10	BANK0	TMS_0	JTAG Test Mode Select
Unused	VN_0		M11	XADC_IN0_N	97	98	TDI	H9	BANK0	TDI_0	JTAG Test Data Input
Unused	DXP_0		N12	XADC_TMP_P	99	100	TDO	G9	BANK0	TDO_0	JTAG Test Data Output
Unused	DXN_0		N11	XADC_TMP_N	101	102	GND				Ground
Unused	GNDADC_0		K11	XADC_GND	103	104	PS_MIO40	E9	BANK501	PS_MIO40_501	CLK_SD
Ground				GND	105	106	PS_MIO41	C15	BANK501	PS_MIO41_501	CMD_SD
Unused	PS_MIO0_500	BANK500	G17	PS_MIO0	107	108	PS_MIO42	D15	BANK501	PS_MIO42_501	DATA0_SD
JTAG Mode Select Pin	PS_MIO2_500	BANK500	A21	PS_MIO2	109	110	PS_MIO43	B12	BANK501	PS_MIO43_501	DATA1_SD
Boot Mode Select Pin	PS_MIO4_500	BANK500	E19	PS_MIO4	111	112	PS_MIO44	E10	BANK501	PS_MIO44_501	DATA2_SD
Unused	PS_MIO8_500	BANK500	E18	PS_MIO8	113	114	PS_MIO45	B14	BANK501	PS_MIO45_501	DATA3_SD
Unused	PS_MIO9_500	BANK500	C19	PS_MIO9	115	116	PS_MIO46	D11	BANK501	PS_MIO46_501	Unused
Boot Mode Select Pin	PS_MIO3_500	BANK500	F17	PS_MIO3	117	118	PS_MIO47	B13	BANK501	PS_MIO47_501	Unused
Boot Mode Select Pin	PS_MIO5_500	BANK500	A20	PS_MIO5	119	120	GND				Ground
PLL Mode Pin	PS_MIO6_500	BANK500	A19	PS_MIO6	121	122	PS_MIO48	D12	BANK501	PS_MIO48_501	UART_PS_Transmit
					123	124	PS_MIO49	C9	BANK501	PS_MIO49_501	UART_PS_Receive
					125	126	PS_MIO50	D10	BANK501	PS_MIO50_501	I²C_SCL
					127	128	PS_MIO51	C13	BANK501	PS_MIO51_501	I²C_SDA
Ground				GND	129	130	FPGA_INIT	T8	BANK0	INIT_B_0	Active Low: Indicates initialization of configuration
System Power Good				System_PG	131	132	PROGRAM_B_0	V10	BANK0	PROGRAM_B_0	Active Low: Input to reset and restart FPGA configuration
Unused	PS_MIO7_500	BANK500	D18	PS_MIO7	133	134	FPGA_DONE	T10	BANK0	DONE_0	Active High: DONE goes high when configuration completes successfully

Function	SoC Pin Name	Bank	Ball	Net Name	J2		Net Name	Ball	Bank	SoC Pin Name	Function
Processing System Reset / Active Low	PS_SRST_B_501	BANK501	C14	PS_RST	135	136	VCCBATT	G14	BANK0	VCCBATT_0	Backup power for RTC during power loss
					137	138	VCCO_501			VCCO_MIO1_501	Power Supply pins for the output drivers of BANK501
Power Supply pins for the output drivers of BANK500	VCCO_MIO0_500			VCCO_500	139	140	GND				Ground

Function	SoC Pin Name	Bank	Ball	Net Name	J3		Net Name	Ball	Bank	SoC Pin Name	Function
5V DC Input				VCC_5V0	1	2	VCC_5V0				5V DC Input
5V DC Input				VCC_5V0	3	4	VCC_5V0				5V DC Input
Ground				GND	5	6	GND				Ground
TEST BUTTON	IO_25_34	BANK34	R8	IO_B34_25	7	8	IO_B34_0	H8	BANK34	IO_0_34	USB HUB_RESETn
PMOD	IO_L16P_T2_34	BANK34	N1	IO_B34_L16_P	9	10	IO_B34_L1_P	J8	BANK34	IO_L1P_T0_34	PMOD
PMOD	IO_L16N_T2_34	BANK34	P1	IO_B34_L16_N	11	12	IO_B34_L1_N	K8	BANK34	IO_L1N_T0_34	PMOD
PMOD	IO_L19P_T3_34	BANK34	N6	IO_B34_L19_P	13	14	IO_B34_L3_P	K7	BANK34	IO_L3P_T0_DQS_PUDC_B_34	PMOD
PMOD	IO_L19N_T3_VREF_34	BANK34	N5	IO_B34_L19_N	15	16	IO_B34_L3_N	L7	BANK34	IO_L3N_T0_DQS_34	PMOD
PMOD	IO_L12P_T1_MRCC_34	BANK34	L5	IO_B34_L12_P	17	18	IO_B34_L2_P	J7	BANK34	IO_L2P_T0_34	PMOD
PMOD	IO_L12N_T1_MRCC_34	BANK34	L4	IO_B34_L12_N	19	20	IO_B34_L2_N	J6	BANK34	IO_L2N_T0_34	PMOD
Ground				GND	21	22	GND				Ground
PMOD	IO_L18P_T2_34	BANK34	P3	IO_B34_L18_P	23	24	IO_B34_L7_P	J5	BANK34	IO_L7P_T1_34	PMOD
PMOD	IO_L18N_T2_34	BANK34	P2	IO_B34_L18_N	25	26	IO_B34_L7_N	K5	BANK34	IO_L7N_T1_34	PMOD
PMOD	IO_L11P_T1_SRCC_34	BANK34	K4	IO_B34_L11_P	27	28	IO_B34_L6_P	M8	BANK34	IO_L6P_T0_34	PMOD
PMOD	IO_L11N_T1_SRCC_34	BANK34	K3	IO_B34_L11_N	29	30	IO_B34_L6_N	M7	BANK34	IO_L6N_T0_VREF_34	PMOD
PMOD	IO_L13P_T2_MRCC_34	BANK34	T2	IO_B34_L13_P	31	32	IO_B34_L5_P	N8	BANK34	IO_L5P_T0_34	PMOD
PMOD	IO_L13N_T2_MRCC_34	BANK34	T1	IO_B34_L13_N	33	34	IO_B34_L5_N	P8	BANK34	IO_L5N_T0_34	PMOD
Power Supply pins for the output drivers of BANK34	VCCO_34			VCCO_BANK34	35	36	VCCO_BANK34			VCCO_34	Power Supply pins for the output drivers of BANK34
Ground				GND	37	38	GND				Ground
TEST BUTTON	IO_L10P_T1_34	BANK34	L2	IO_B34_L10_P	39	40	IO_B34_L24_P	P7	BANK34	IO_L24P_T3_34	USB HUB_HS_IND
TEST BUTTON	IO_L10N_T1_34	BANK34	L1	IO_B34_L10_N	41	42	IO_B34_L24_N	R7	BANK34	IO_L24N_T3_34	USB HUB_SUSP_IND
TEST BUTTON	IO_L15P_T2_DQS_34	BANK34	M2	IO_B34_L15_P	43	44	IO_B34_L23_P	R5	BANK34	IO_L23P_T3_34	USB HUB_SCL
TEST LED	IO_L15N_T2_DQS_34	BANK34	M1	IO_B34_L15_N	45	46	IO_B34_L23_N	R4	BANK34	IO_L23N_T3_34	USB HUB_SDA
TEST LED	IO_L8P_T1_34	BANK34	J2	IO_B34_L8_P	47	48	IO_B34_L20_P	P6	BANK34	IO_L20P_T3_34	UART_PL_Transmit
TEST LED	IO_L8N_T1_34	BANK34	J1	IO_B34_L8_N	49	50	IO_B34_L20_N	P5	BANK34	IO_L20N_T3_34	UART_PL_Receive

Function	SoC Pin Name	Bank	Ball	Net Name	J3		Net Name	Ball	Bank	SoC Pin Name	Function
Ground				GND	51	52	GND				Ground
TEST LED	IO_L22P_T3_34	BANK34	M4	IO_B34_L22_P	53	54	IO_B34_L17_P	R3	BANK34	IO_L17P_T2_34	IO_Header
TEST LED	IO_L22N_T3_34	BANK34	M3	IO_B34_L22_N	55	56	IO_B34_L17_N	R2	BANK34	IO_L17N_T2_34	IO_Header
IO_Header	IO_L9P_T1_DQS_34	BANK34	J3	IO_B34_L9_P	57	58	IO_B34_L21_P	N4	BANK34	IO_L21P_T3_DQS_34	IO_Header
IO_Header	IO_L9N_T1_DQS_34	BANK34	K2	IO_B34_L9_N	59	60	IO_B34_L21_N	N3	BANK34	IO_L21N_T3_DQS_34	IO_Header
IO_Header	IO_L4P_T0_34	BANK34	L6	IO_B34_L4_P	61	62	IO_B34_L14_P	U2	BANK34	IO_L14P_T2_SRCC_34	IO_Header
IO_Header	IO_L4N_T0_34	BANK34	M6	IO_B34_L4_N	63	64	IO_B34_L14_N	U1	BANK34	IO_L14N_T2_SRCC_34	IO_Header
Ground				GND	65	66	GND				Ground
IO_Header	IO_L15P_T2_DQS_13	BANK13	AB21	IO_B13_L15_P	67	68	IO_B13_L13_P	Y18	BANK13	IO_L13P_T2_MRCC_13	IO_Header
IO_Header	IO_L15N_T2_DQS_13	BANK13	AB22	IO_B13_L15_N	69	70	IO_B13_L13_N	Y19	BANK13	IO_L13N_T2_MRCC_13	IO_Header
IO_Header	IO_L16P_T2_13	BANK13	AB18	IO_B13_L16_P	71	72	IO_B13_L21_P	V18	BANK13	IO_L21P_T3_DQS_13	IO_Header
IO_Header	IO_L16N_T2_13	BANK13	AB19	IO_B13_L16_N	73	74	IO_B13_L21_N	W18	BANK13	IO_L21N_T3_DQS_13	IO_Header
IO_Header	IO_L18P_T2_13	BANK13	AA19	IO_B13_L18_P	75	76	IO_B13_L14_P	AA16	BANK13	IO_L14P_T2_SRCC_13	RS232-SER0_Receive
IO_Header	IO_L18N_T2_13	BANK13	AA20	IO_B13_L18_N	77	78	IO_B13_L14_N	AA17	BANK13	IO_L14N_T2_SRCC_13	RS232-SER0_Transmit
Ground				GND	79	80	GND				Ground
Power Supply pins for the output drivers of BANK13	VCCO_13			VCCO_BANK13	81	82	VCCO_BANK13			VCCO_13	Power Supply pins for the output drivers of BANK13
CAN_PL1_Transmit	IO_L17P_T2_13	BANK13	AB16	IO_B13_L17_P	83	84	IO_B13_0	T16	BANK13	IO_0_13	SFP
CAN_PL1_Receive	IO_L17N_T2_13	BANK13	AB17	IO_B13_L17_N	85	86	IO_B13_L20_P	U19	BANK13	IO_L20P_T3_13	SFP
TEST LED	IO_L22P_T3_13	BANK13	U17	IO_B13_L22_P	87	88	IO_B13_L20_N	V19	BANK13	IO_L20N_T3_13	SFP
RS485 FPGA RX	IO_L22N_T3_13	BANK13	U18	IO_B13_L22_N	89	90	IO_B13_L11_P	AA14	BANK13	IO_L11P_T1_SRCC_13	SFP
RS485 RX EN	IO_L23P_T3_13	BANK13	V16	IO_B13_L23_P	91	92	IO_B13_L11_N	AA15	BANK13	IO_L11N_T1_SRCC_13	SFP
RS485 TX EN	IO_L23N_T3_13	BANK13	W16	IO_B13_L23_N	93	94	IO_B13_L9_P	AB13	BANK13	IO_L9P_T1_DQS_13	SFP
Ground				GND	95	96	IO_B13_L9_N	AB14	BANK13	IO_L9P_T1_DQS_13	SFP
RS485 FPGA TX	IO_L19P_T3_13	BANK13	R17	IO_B13_L19_P	97	98	GND				Ground
RS485 TX TERM	IO_L19N_T3_VREF_13	BANK13	T17	IO_B13_L19_N	99	100	IO_B13_L7_P	AA11	BANK13	IO_L7P_T1_13	SFP
RS485 RX TERM	IO_L3P_T0_DQS_13	BANK13	W12	IO_B13_L3_P	101	102	IO_B13_L7_N	AB11	BANK13	IO_L7N_T1_13	PCI-e RC
RS485 SLEWRATE	IO_L3N_T0_DQS_13	BANK13	W13	IO_B13_L3_N	103	104	IO_B13_L5_P	U11	BANK13	IO_L5P_T0_13	PCI-e RC
CAN_PL2_Receive	IO_L8P_T1_13	BANK13	AA12	IO_B13_L8_P	105	106	IO_B13_L5_N	U12	BANK13	IO_L5N_T0_13	PCI-e RC
CAN_PL2_Transmit	IO_L8N_T1_13	BANK13	AB12	IO_B13_L8_N	107	108	IO_B13_L4_P	V11	BANK13	IO_L4P_T0_13	PCI-e RC
Ground				GND	109	110	IO_B13_L4_N	W11	BANK13	IO_L4N_T0_13	PCI-e RC

Function	SoC Pin Name	Bank	Ball	Net Name	J3		Net Name	Ball	Bank	SoC Pin Name	Function
SFP	MGTPTXP0	BANK112	AA3	MGTP_TX0_P	111	112	GND				Ground
SFP	MGTPTXN0	BANK112	AB3	MGTP_TX0_N	113	114	MGTP_TX2_P	AA5	BANK112	MGTPTXP2	PCI-e RC
Ground				GND	115	116	MGTP_TX2_N	AB5	BANK112	MGTPTXN2	PCI-e RC
SFP	MGTPRXP0	BANK112	AA7	MGTP_RX0_P	117	118	GND				Ground
SFP	MGTPRXN0	BANK112	AB7	MGTP_RX0_N	119	120	MGTP_RX2_P	AA9	BANK112	MGTPRXP2	PCI-e RC
Ground				GND	121	122	MGTP_RX2_N	AB9	BANK112	MGTPRXN2	PCI-e RC
PCI-e EP	MGTPTXP1	BANK112	W4	MGTP_TX1_P	123	124	GND				Ground
PCI-e EP	MGTPTXN1	BANK112	Y4	MGTP_TX1_N	125	126	MGTP_TX3_P	W2	BANK112	MGTPTXP3	PCI-e RC
Ground				GND	127	128	MGTP_TX3_N	Y2	BANK112	MGTPTXN3	PCI-e RC
PCI-e EP	MGTPRXP1	BANK112	W8	MGTP_RX1_P	129	130	GND				Ground
PCI-e EP	MGTPRXN1	BANK112	Y8	MGTP_RX1_N	131	132	MGTP_RX3_P	W6	BANK112	MGTPRXP3	PCI-e RC
Ground				GND	133	134	MGTP_RX3_N	Y6	BANK112	MGTPRXN3	PCI-e RC
SFP	MGTREFCLKP0	BANK112	U9	MGTREF_ CLK0_P	135	136	GND				Ground
SFP	MGTREFCLKN0	BANK112	V9	MGTREF_ CLK0_N	137	138	MGTREF_ CLK1_P	U5	BANK112	MGTREFCLKP1	PCI-e
Ground				GND	139	140	MGTREF_ CLK1_N	V5	BANK112	MGTREFCLKN1	PCI-e

3. Signal Connections

The board provides access to both PS (Processing System) and PL (Programmable Logic) I/Os through headers and dedicated connectors. These include UART, I²C, CAN, GPIO, PCIe, and memory interfaces.

4. Configuration

FPGA configuration can be selected via DIP switches. The onboard RTC is battery-backed for non-volatile timekeeping. LED indicators provide real-time status of FPGA initialization and board power.

5. Safety Guidelines



Caution

The DE13310 shall not be operated in any manner not specified in this document. Misuse of the product may result in a hazard. Safety protection features may be compromised if the product is damaged. In the event of damage, the product shall be returned for repair.

6. Compatibility Guidelines

This product has been tested and found to comply with the applicable regulatory requirements and limits for electromagnetic compatibility (EMC). These requirements and limits are designed to provide reasonable protection against harmful interference when the product is operated within its intended electromagnetic environment.

The product is intended to be used in industrial locations. However, harmful interference may still be caused in certain installations, particularly when connected to peripheral devices or test objects, or when operated in residential or commercial environments. To reduce the potential for radio and television interference and to avoid unacceptable degradation in performance, the product must be installed and used strictly in accordance with the instructions provided in the documentation.

In addition, any changes or modifications to the product that are not expressly approved by DEICO are not permitted and could void the user's authority to operate the equipment under applicable regulatory provisions.



Caution

To ensure the specified EMC performance, the product shall be operated only with shielded cables and accessories.



Caution

To ensure the specified EMC performance, the length of any cable attached to the front connectors shall not exceed 3 m (10 ft.).