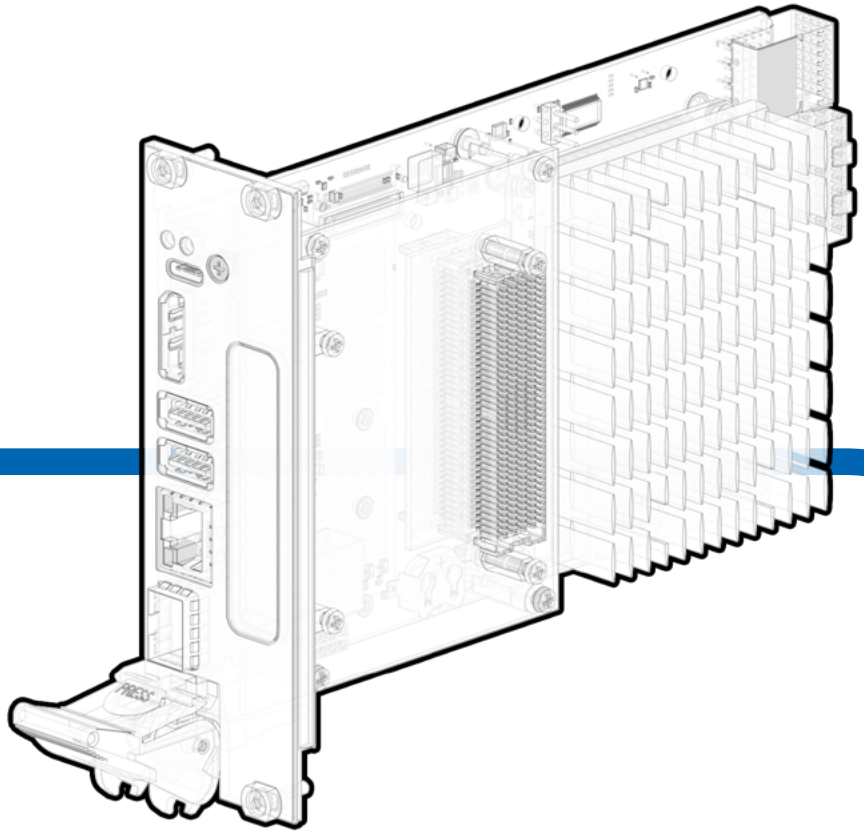
Datasheet



DE160203

PXIe Kria Module

DEICO

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1. Description

DE160203 PXIe Kria Module is a high-performance, adaptable processing platform designed to bring the full potential of the AMD Kria™ K26 System-on-Module (SoM) to the modular PXIe ecosystem. By integrating the AMD Zynq™ UltraScale+™ MPSoC at its core, this module masterfully combines the flexibility of programmable logic (FPGA) with the processing power of ARM®-based cores. This synergy makes it an ideal solution for the most demanding applications requiring real-time control, hardware acceleration, and complex algorithm processing within a synchronized, scalable test and measurement environment.

This module leverages the PXIe form factor to extend the Kria K26 SoM's capabilities with a rich set of industry-standard interfaces, facilitating rapid prototyping and deployment of complex embedded systems. The front panel offers essential high-speed connectivity, including a 2-port USB 3.0 hub, a DisplayPort, an SFP+ cage for optical networking, and a 1G PS Ethernet port. The module's architecture ensures robust data throughput via a high-speed 2-lane PXIe connection implemented in the programmable logic (PL).

Designed for customization and expandability, the PXIe Kria Module features an LPC FMC connector and a PMOD connector, allowing users to integrate specialized I/O, custom sensor interfaces, or additional peripherals. Storage solutions are versatile, with an M.2 slot for a 2-lane NVMe drive and a microSD card interface for flexible OS booting. This adaptability makes the PXIe Kria Module a powerful building block for next-generation systems in aerospace, automotive, and industrial control.

1.1. Key Features

- **AMD Kria K26 SoM Integration:** Powered by the AMD Zynq™ UltraScale+™ MPSoC, which combines a processing system (PS) with programmable logic (PL) to deliver exceptional performance for sophisticated embedded workloads.
- **PXIe Form Factor:** Modular design fits into PXIe chassis. It leverages the PXIe backplane for a 2-lane Gen3 PCIe connection routed through the Programmable Logic (PL), enabling precise synchronization and easy integration into larger test systems.
- **High-Speed Connectivity:** Features a versatile set of front-panel I/O, including a 2-port USB 3.0 hub, one DisplayPort output, one SFP+ cage for 10G optical links, and a 1G PS Ethernet port for network communication.
- **Flexible Storage and Boot:** Equipped with an M.2 slot supporting a 2-lane NVMe PCIe interface (PS), a microSD card interface, and an 8 Kbit I²C EEPROM for configuration data, offering robust options for the operating system and data storage.
- **Customizable and Expandable Architecture:** The inclusion of an LPC FMC connector and a PMOD connector enables users to attach custom mezzanine cards. A shared GT clock resource between the SFP+ and FMC provides enhanced design flexibility.
- **Streamlined Development:** Features onboard JTAG for direct debugging and a UART-to-USB converter for easy console access, significantly simplifying the development and verification process.
- **System Reliability and Monitoring:** Includes an onboard hardware watchdog timer for autonomous system recovery and a dedicated system health monitor IC for real-time tracking of critical voltages and temperatures.

2. Hardware Overview

2.1. Circuitry

DE160203 PXIe Kria Module integrates the AMD Kria K26 SoM, which includes a high-performance Zynq UltraScale+ MPSoC featuring a multi-core ARM CPU and adaptable programmable logic (FPGA). The system is designed to run complex embedded applications, real-time control loops, and hardware-accelerated algorithms directly at the edge. Additionally, the carrier board supports modular I/O expansion via FMC and PMOD connectors, enabling custom hardware additions for specific application needs. The carrier board also integrates key support components, including an I²C EEPROM for non-volatile data storage, a hardware watchdog timer for system reliability, and a health monitor IC to track critical operating parameters.

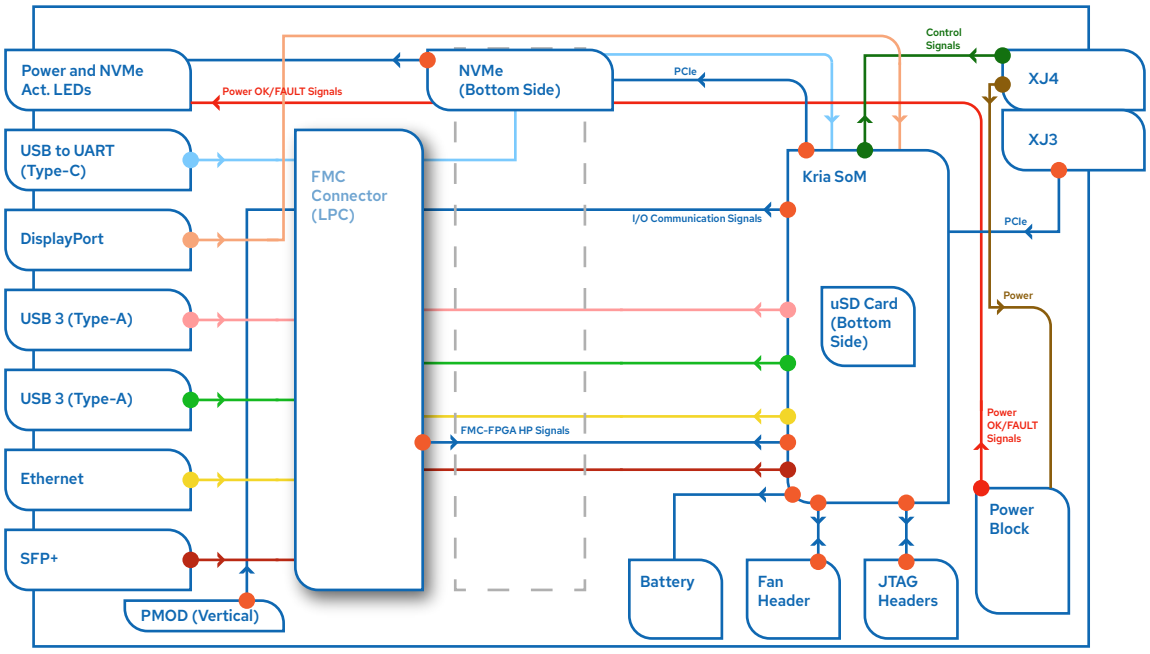


Figure 1: Block Diagram of the Carrier Board

2.2. Hardware Specifications

- **Processor:** AMD Kria K26 SoM with Zynq UltraScale+ MPSoC (Quad-core ARM® Cortex®-A53 MPCore™ and Dual-core ARM Cortex-R5F MPCore™)
- **Memory:** 4 GB 64-bit DDR4 (non-ECC) and 16 GB eMMC
- **Storage:** Supports NVMe (via M.2, 2-lane PS PCIe) and MicroSD card
- **PXIe Interface:** 2-lane PCIe Gen3 (via PL) for high-speed data communication.
- **Video Outputs:** Supports DisplayPort on the front panel
- **I/O Connectivity:** 2-port USB 3.0, Gigabit Ethernet, DisplayPort, SFP+, LPC FMC, and PMOD connector

2.2.1. USB Ports

The carrier board supports 2 USB Type-A (J8-J9) connectors through a USB 3.0 Hub. This allows multiple devices to be connected simultaneously to the Kria K26 SoM. The part number of the Hub is USB5744/2G and its I²C address is 0x2D. The block diagram and pinout table for the USB 3.0 are shown below.

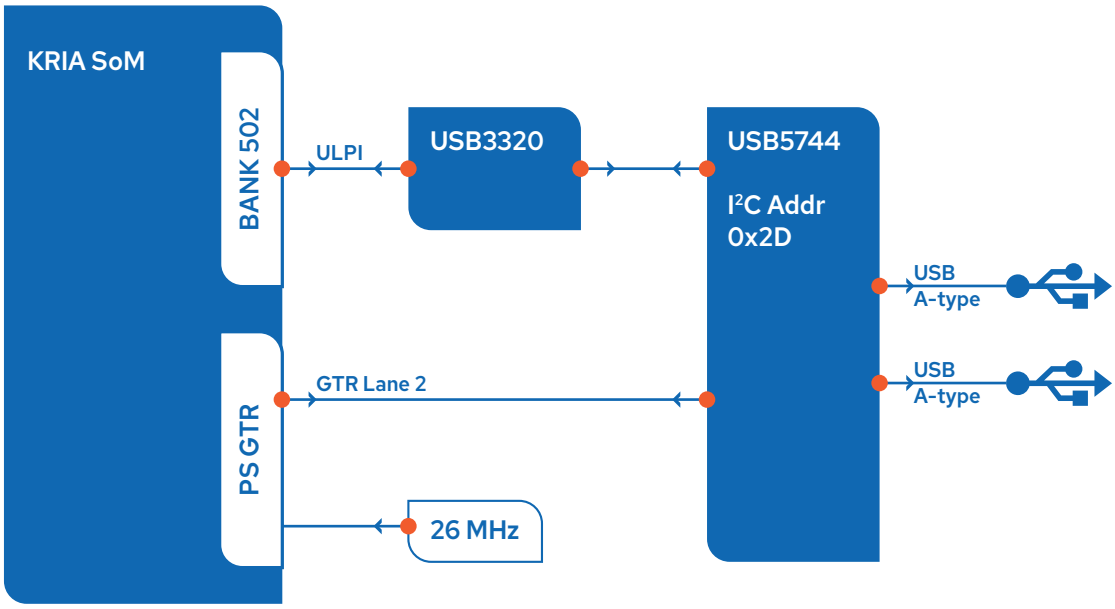


Figure 2: Block Diagram of USB Interface

Table 1: Pinout of USB Interface

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
MIO52	J1-D36	G18	OTG_CLK	USB2.0 Clock
MIO56	J1-C39	C16	OTG_DATA0	USB2.0 Data 0
MIO57	J1-C40	A16	OTG_DATA1	USB2.0 Data 1
MIO54	J1-D38	F17	OTG_DATA2	USB2.0 Data 2
MIO59	J1-B41	E17	OTG_DATA3	USB2.0 Data 3
MIO60	J1-B42	C17	OTG_DATA4	USB2.0 Data 4
MIO61	J1-A38	D17	OTG_DATA5	USB2.0 Data 5
MIO62	J1-A39	A17	OTG_DATA6	USB2.0 Data 6
MIO63	J1-A40	E18	OTG_DATA7	USB2.0 Data 7
MIO53	J1-D37	D16	OTG_DIR	USB2.0 Data Direction
MIO55	J1-C38	B16	OTG_NXT	USB2.0 Next Data
MIO58	J1-B40	F18	OTG_STP	USB2.0 Stop
MIO44	J1-D32	J20	OTG_RSTn	USB Reset (Active Low)
GTR_DP2_C2M_P	J1-B53	B27	USB_3_UP_TX_P	USB3.0 Data Transmit Positive
GTR_DP2_C2M_N	J1-B54	B28	USB_3_UP_TX_N	USB3.0 Data Transmit Negative
GTR_DP2_M2C_P	J1-D57	C25	USB_3_UP_RX_P	USB3.0 Data Receive Positive
GTR_DP2_M2C_N	J1-D58	C26	USB_3_UP_RX_N	USB3.0 Data Receive Negative
GTR_REFCLK1_C2M_P	J1-B49	E21	GTR_REFCLK1_C2M_P	USB3.0 Reference Clock Positive
GTR_REFCLK1_C2M_N	J1-B50	E22	GTR_REFCLK1_C2M_N	USB3.0 Reference Clock Negative

2.2.2. Gigabit Ethernet

The carrier board implements a Gigabit Ethernet connector (J7) along with the necessary magnetics device and it is connected to the Processing System (PS) of the Kria K26 SoM. This interface leverages the Zynq UltraScale+ MPSoC's hardened Gigabit Ethernet MAC (GEM) controller, providing a high-performance, low-latency network connection ideal for the primary operating system, management access, and data-intensive applications. The block diagram and the pinout table for the 1G Ethernet are shown below.

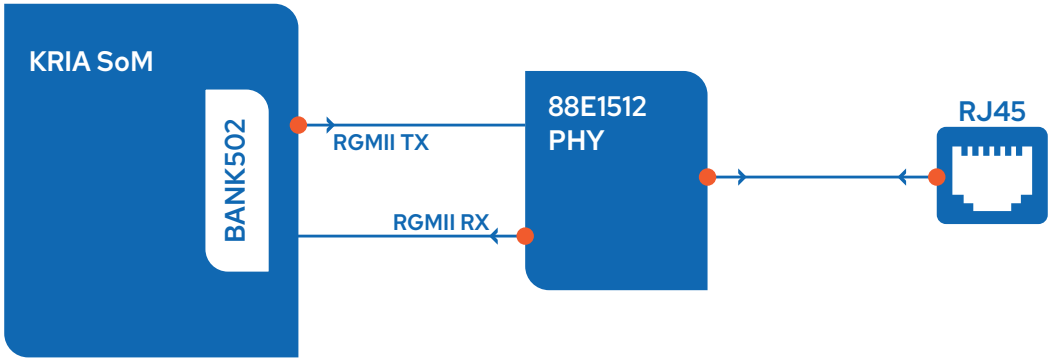


Figure 3: Block Diagram of 1G Ethernet

Table 2: Pinout of PS Ethernet

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
MIO64	J1-D40	E19	ETH_PS_TX_CLK	PS Ethernet RGMII Transmit Clock
MIO65	J1-D41	A18	ETH_PS_TXD0	PS Ethernet Transmit Data 0
MIO66	J1-D42	G19	ETH_PS_TXD1	PS Ethernet Transmit Data 1
MIO67	J1-C42	B18	ETH_PS_TXD2	PS Ethernet Transmit Data 2
MIO68	J1-C43	C18	ETH_PS_TXD3	PS Ethernet Transmit Data 3
MIO69	J1-C44	D19	ETH_PS_TX_CTRL	PS Ethernet RGMII Transmit Enable
MIO70	J1-B44	C19	ETH_PS_RX_CLK	PS Ethernet RGMII Receive Clock
MIO71	J1-B45	B19	ETH_PS_RXD0	PS Ethernet Receive Data 0
MIO72	J1-B46	G20	ETH_PS_RXD1	PS Ethernet Receive Data 1
MIO73	J1-A42	G21	ETH_PS_RXD2	PS Ethernet Receive Data 2
MIO74	J1-A43	D20	ETH_PS_RXD3	PS Ethernet Receive Data 3
MIO75	J1-A44	A19	ETH_PS_RX_CTRL	PS Ethernet RGMII Receive Enable
MIO76	J1-D44	B20	ETH_PS_MDC	PS Ethernet MDIO Clock
MIO77	J1-D45	F20	ETH_PS_MDIO	PS Ethernet MDIO Data
MIO38	J1-B32	H18	ETH_PS_RSTn	PS Ethernet Reset (Active Low)

2.2.3. DisplayPort

The carrier board is equipped with a full-size DisplayPort (J10) connector to provide high-resolution digital video output directly from the Kria K26 SoM's integrated display controller. This allows for a seamless, single-cable connection to modern monitors, industrial displays, and human-machine interfaces (HMIs). The block diagram and pinout table for the DisplayPort are shown below.

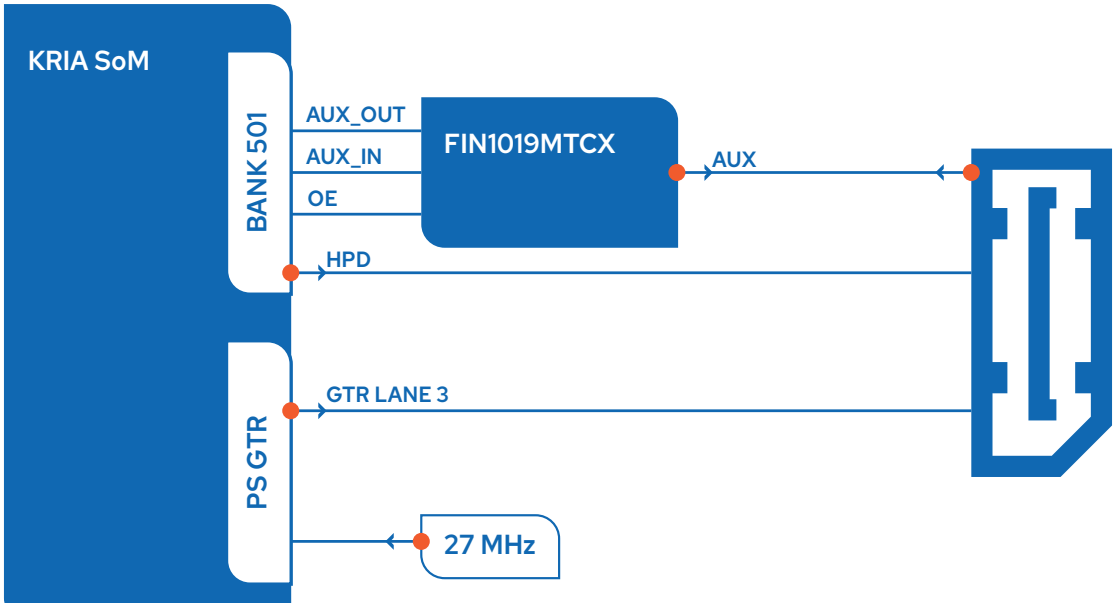


Figure 4: Block Diagram of DisplayPort Interface

Table 3: Pinout of DisplayPort Interface

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
GTR_DP3_M2C_P	J1-C51	B23	DP_LN0_P	DisplayPort Lane 0 Data Positive
GTR_DP3_M2C_N	J1-C52	B24	DP_LN0_N	DisplayPort Lane 0 Data Negative
GTR_REFCLK0_C2M_P	J1-C47	F23	GTR_REFCLK0_C2M_P	DisplayPort Reference Clock Positive
GTR_REFCLK0_C2M_N	J1-C48	F24	GTR_REFCLK0_C2M_N	DisplayPort Reference Clock Negative
MIO27	J1-D29	J15	DP_AUX_OUT	DisplayPort Auxiliary Data Out
MIO30	J1-C31	F16	DP_AUX_IN	DisplayPort Auxiliary Data In
MIO28	J1-D30	K15	DP_HPD	DisplayPort Insertion Detection
MIO29	J1-C30	G16	DP_OE	DisplayPort Auxiliary Output Enable

2.2.4. SFP+ Mode

The carrier board supports an SFP+ (J12) interface. This interface is implemented for direct fibre optic or copper-based networking applications, allowing for the implementation of protocols like 10G Ethernet. The lane 2 of the PL GTH transceiver is connected to the SFP+. However, the associated reference clock is not dedicated; it is shared with the FMC connector and is selectable via the SW0801 DIP switch. When the SW0801 is "ON" position, the clock is routed for SFP+ operation.

Note

To ensure system stability and prevent potential damage to components, all configuration switches must be set while the board is powered off. The selected configuration will take effect on the next power-on cycle.

The block diagram and pinout table for the SFP+ interface are shown below.

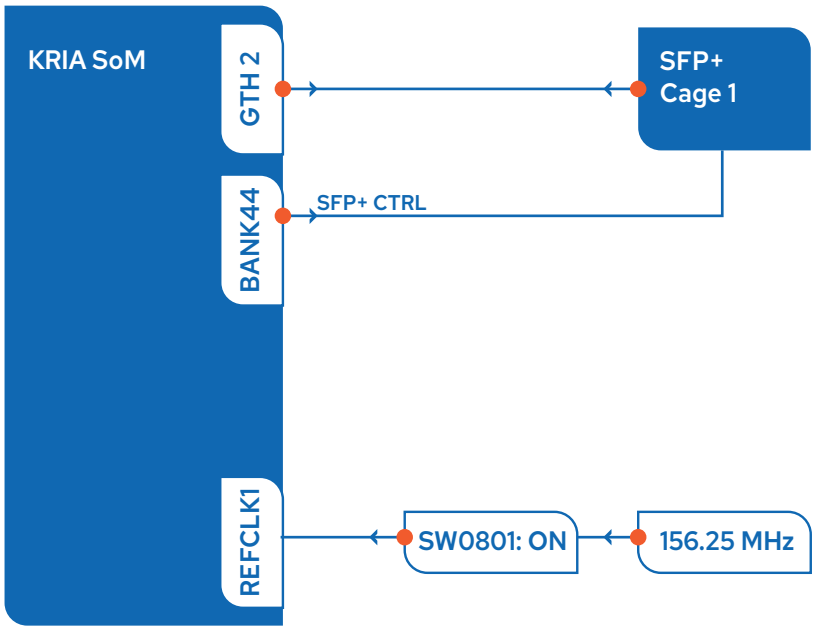


Figure 5: Block Diagram of SFP+ Interface

Table 4: Pinout of SFP+ Interface

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
GTH_DP2_M2C_P	J2-B5	R4	SFP1_TX_P	SFP+ 1 Data Transmit Positive
GTH_DP2_M2C_N	J2-B6	R3	SFP1_TX_N	SFP+ 1 Data Transmit Negative
GTH_DP2_C2M_P	J2-B1	T2	SFP1_RX_P	SFP+ 1 Data Receive Positive
GTH_DP2_C2M_N	J2-B2	T1	SFP1_RX_N	SFP+ 1 Data Receive Negative
HDC14	J2-B54	W14	SFP1_DIS	SFP+ 1 Transmit Disable
HDC15	J2-B56	W13	SFP1_LOS	SFP+ 1 Loss of Signal
HDC16_CC	J2-B57	AB15	SFP1_FLT	SFP+ 1 Transmit Fault
HDC17	J2-B58	AB14	SFP1_SCL	SFP+ 1 Serial Interface Clock
HDC18	J2-A54	Y14	SFP1_SDA	SFP+ 1 Serial Interface Data
GTH_REFCLK1_C2M_P	J2-A7	V6	SFP_REFCLK_P (SW0801: ON)	SFP+ Clock Reference Positive
GTH_REFCLK1_C2M_N	J2-A8	V5	SFP_REFCLK_N (SW0801: ON)	SFP+ Clock Reference Negative

2.2.5. FMC Connector

To provide maximum system flexibility and enable a wide range of application-specific I/O, the carrier board is equipped with a standard FPGA Mezzanine Card (FMC) connector (J3). This allows users to extend the functionality of the Kria K26 SoM by adding commercially available or custom-designed LPC FMC boards for tasks such as high-speed data acquisition, advanced video processing, or specialized industrial interfacing. The lane 3 of the PL GTH transceiver is connected to the FMC. However, its reference clock is shared with the SFP+ interface and is controlled by the SW0801 DIP switch. When SW0801 is in the "OFF" position, the clock is routed to the FMC connector.

The connector adheres to the VITA 57.1 FPGA Mezzanine Card standard. The board features a Low Pin Count (LPC) connector, providing access to a substantial number of the Kria SoM's programmable logic I/O pins. The VADJ power rail, which supplies the I/O voltage for the FMC card's logic levels, is fixed at 1.8V on the carrier board. This determines the electrical compatibility for any connected mezzanine card.

Note

To ensure system stability and prevent potential damage to components, all configuration switches must be set while the board is powered off. The selected configuration will take effect on the next power-on cycle.

Note

The FMC interface on this board is designed exclusively for use with mezzanine cards that support 1.8 V I/O logic levels. The VADJ voltage is not user-configurable. Attempting to use an FMC card designed for a different I/O voltage (e.g., 2.5 V) may result in damage to the FMC card, the carrier board, or the Kria SoM.

The pinout table for the FMC interface is shown below.

Table 5: Pinout of FMC (LPC) Interface

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name
GTH_DP3_M2C_P	J2-A3	N4	FMC_DP0_C2M_P
GTH_DP3_M2C_N	J2-A4	N3	FMC_DP0_C2M_N
GTH_DP3_C2M_P	J2-D5	P2	FMC_DP0_M2C_P
GTH_DP3_C2M_N	J2-D6	P1	FMC_DP0_M2C_N
GTH_REFCLK1_C2M_P	J2-A7	V6	FMC_GBTCLK0_M2C_P (SW0801: OFF)
GTH_REFCLK1_C2M_N	J2-A8	V5	FMC_GBTCLK0_M2C_N (SW0801: OFF)
HPB11_P	J2-B21	M6	FMC_CLK0_M2C_P
HPB11_N	J2-B22	L5	FMC_CLK0_M2C_N
HPC11_P	J2-C32	AC4	FMC_CLK1_M2C_P
HPC11_N	J2-C33	AC3	FMC_CLK1_M2C_N
HPC09_P	J2-D27	AF7	FMC_LA00_P_CC
HPC09_N	J2-D28	AF6	FMC_LA00_N_CC
HPC10_CC_P	J2-C29	AD5	FMC_LA01_P_CC
HPC10_CC_N	J2-C30	AD4	FMC_LA01_N_CC

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name
HPC04_P	J2-D39	AB7	FMC_LA02_P
HPC04_N	J2-D40	AC7	FMC_LA02_N
HPC03_P	J2-A41	AD7	FMC_LA03_P
HPC03_N	J2-A42	AE7	FMC_LA03_N
HPC15_CC_P	J2-A38	AG4	FMC_LA04_P
HPC15_CC_N	J2-A39	AH4	FMC_LA04_N
HPC07_P	J2-B36	AH8	FMC_LA05_P
HPC07_N	J2-B37	AH7	FMC_LA05_N
HPC05_CC_P	J2-C38	AG9	FMC_LA06_P
HPC05_CC_N	J2-C39	AH9	FMC_LA06_N
HPC00_CC_P	J2-D33	AC9	FMC_LA07_P
HPC00_CC_N	J2-D34	AD9	FMC_LA07_N
HPC12_P	J2-C35	AB4	FMC_LA08_P
HPC12_N	J2-C36	AB3	FMC_LA08_N
HPC13_P	J2-B30	AD2	FMC_LA09_P
HPC13_N	J2-B31	AD1	FMC_LA09_N
HPC14_P	J2-A35	AB2	FMC_LA10_P
HPC14_N	J2-A36	AC2	FMC_LA10_N
HPC08_P	J2-A29	AG6	FMC_LA11_P
HPC08_N	J2-A30	AG5	FMC_LA11_N
HPC16_P	J2-B33	AG3	FMC_LA12_P
HPC16_N	J2-B34	AH3	FMC_LA12_N
HPC06_P	J2-B27	AF8	FMC_LA13_P
HPC06_N	J2-B28	AG8	FMC_LA13_N
HPC01_P	J2-D30	AE9	FMC_LA14_P
HPC01_N	J2-D31	AE8	FMC_LA14_N
HPC17_P	J2-C26	AE3	FMC_LA15_P
HPC17_N	J2-C27	AF3	FMC_LA15_N
HPC19_P	J2-A32	AH2	FMC_LA16_P
HPC19_N	J2-A33	AH1	FMC_LA16_N
HPB_CLK0_P	J2-D18	L3	FMC_LA17_P_CC
HPB_CLK0_N	J2-D19	L2	FMC_LA17_N_CC
HPB09_P	J2-C11	K4	FMC_LA18_P_CC

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name
HPB09_N	J2-C12	K3	FMC_LA18_N_CC
HPB16_P	J2-A23	J7	FMC_LA19_P
HPB16_N	J2-A24	H7	FMC_LA19_N
HPB03_P	J2-B24	R8	FMC_LA20_P
HPB03_N	J2-B25	T8	FMC_LA20_N
HPB13_P	J2-C20	P7	FMC_LA21_P
HPB13_N	J2-C21	P6	FMC_LA21_N
HPB06_P	J2-A20	J1	FMC_LA22_P
HPB06_N	J2-A21	H1	FMC_LA22_N
HPB04_P	J2-D21	R7	FMC_LA23_P
HPB04_N	J2-D22	T7	FMC_LA23_N
HPB00_CC_P	J2-D15	W8	FMC_LA24_P
HPB00_CC_N	J2-D16	Y8	FMC_LA24_N
HPB14_P	J2-C14	N9	FMC_LA25_P
HPB14_N	J2-C15	N8	FMC_LA25_N
HPB05_CC_P	J2-B18	L1	FMC_LA26_P
HPB05_CC_N	J2-B19	K1	FMC_LA26_N
HPB02_P	J2-C17	U8	FMC_LA27_P
HPB02_N	J2-C18	V8	FMC_LA27_N
HPB07_P	J2-B15	K2	FMC_LA28_P
HPB07_N	J2-B16	J2	FMC_LA28_N
HPB12_P	J2-A17	N7	FMC_LA29_P
HPB12_N	J2-A18	N6	FMC_LA29_N
HPB01_P	J2-D12	U9	FMC_LA30_P
HPB01_N	J2-D11	V9	FMC_LA30_N
HPB08_P	J2-A14	H4	FMC_LA31_P
HPB08_N	J2-A15	H3	FMC_LA31_N
HPB15_CC_P	J2-A11	J5	FMC_LA32_P
HPB15_CC_N	J2-A12	J4	FMC_LA32_N
HPB10_CC_P	J2-B12	L7	FMC_LA33_P
HPB10_CC_N	J2-B13	L6	FMC_LA33_N
HDB18	J2-A46	W10	FMC_SCL
HDB19	J2-A47	Y10	FMC_SDA

2.2.6. M.2 Key M NVMe Slot

The carrier board includes a M.2, Key M Slot for NVMe storage (J6). The M.2, Key M Slot supports PCIe (x2) and it is connected to the Processing System (PS) of the Kria K26 SoM. To accommodate high-speed, high-capacity storage, the carrier board is equipped with a standard M.2 connector. This interface is ideal for installing a solid-state drive (SSD) to host a full operating system, store large application files, or perform high-speed data logging, offering a significant performance advantage over MicroSD card storage. The block diagram and the pinout for NVMe interface are shown below.

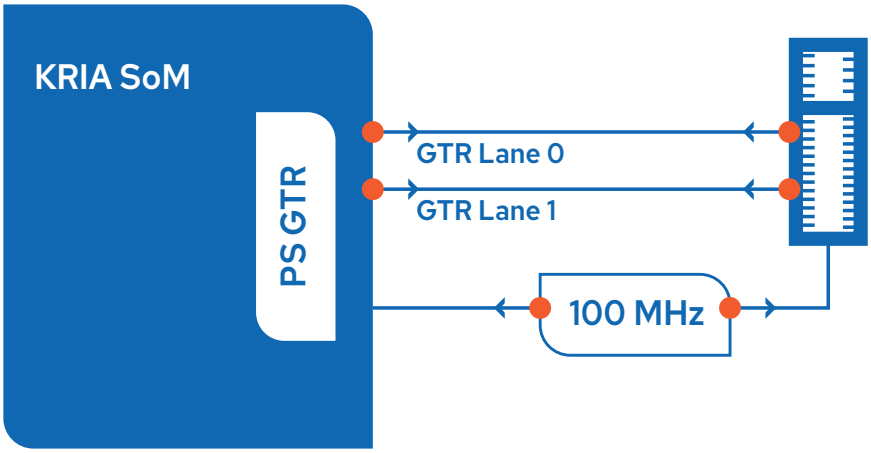


Figure 6: Block Diagram of NVMe Interface

Table 6: Pinout of M.2 Key M NVMe Slot

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
GTR_DP0_M2C_P	J1-B57	E25	NVME_TX0_P	NVMe Data Transmit 0 Positive
GTR_DP0_M2C_N	J1-B58	E26	NVME_TX0_N	NVMe Data Transmit 0 Negative
GTR_DP0_C2M_P	J1-A55	F27	NVME_RX0_P	NVMe Data Receive 0 Positive
GTR_DP0_C2M_N	J1-A56	F28	NVME_RX0_N	NVMe Data Receive 0 Negative
GTR_DP1_M2C_P	J1-A47	D23	NVME_TX1_P	NVMe Data Transmit 1 Positive
GTR_DP1_M2C_N	J1-A48	D24	NVME_TX1_N	NVMe Data Transmit 1 Negative
GTR_DP1_C2M_P	J1-C55	D27	NVME_RX1_P	NVMe Data Receive 1 Positive
GTR_DP1_C2M_N	J1-C56	D28	NVME_RX1_N	NVMe Data Receive 1 Negative
GTR_REFCLK3_C2M_P	J1-A51	A21	NVME_REFCLK_P	NVMe Reference Clock Positive
GTR_REFCLK3_C2M_N	J1-A52	A22	NVME_REFCLK_N	NVMe Reference Clock Negative

2.2.7. PXIe Interface

The module utilizes a high-bandwidth 2-lane PCIe Gen3 interface to ensure rapid data communication between the Kria K26 SoM and the PXIe backplane.

Table 7: Pinout of PXIe Connector

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
GTH_DP0_M2C_P	J2-D9	W4	1PET0_P	PCIe Lane 0 Data Transmit Positive
GTH_DP0_M2C_N	J2-D10	W3	1PET0_N	PCIe Lane 0 Data Transmit Negative
GTH_DP1_M2C_P	J2-C7	U4	1PET1_P	PCIe Lane 1 Data Transmit Positive
GTH_DP1_M2C_N	J2-C8	U3	1PET1_N	PCIe Lane 1 Data Transmit Negative
GTH_DP0_C2M_P	J2-B9	Y2	1PER0_P	PCIe Lane 0 Data Receive Positive
GTH_DP0_C2M_N	J2-B10	Y1	1PER0_N	PCIe Lane 0 Data Receive Negative
GTH_DP1_C2M_P	J2-D1	V2	1PER1_P	PCIe Lane 1 Data Receive Positive
GTH_DP1_C2M_N	J2-D2	V1	1PER1_N	PCIe Lane 1 Data Receive Negative
GTH_REFCLK0_C2M_P	J2-C3	Y6	1RefClk_P	PCIe Reference Clock Positive
GTH_REFCLK0_C2M_N	J2-C4	Y5	1RefClk_N	PCIe Reference Clock Negative
HDA10	J1-A16	J12	SMBCLK	PCIe SM Clock
HDA11	J1-A17	H12	SMBDAT	PCIe SM Data
HDB12	J2-B44	AD11	PERST#	PCIe Reset (Active Low)
HDB14	J2-B46	AA11	WAKE#	PCIe Wake Signal
HDB13	J2-B45	AD10	PRSNT#	PCIe Present Signal

2.2.8. MicroSD Card Slot

For system booting and secondary data storage, the carrier board is equipped with a MicroSD card slot (J5). This interface is primarily used to host the bootloader, operating system kernel, and file system for the Kria K26 SoM. The interface is designed for reliability and compatibility with standard SD and SDHC (High Capacity) media. The block diagram and the pinout for the MicroSD interface are shown below.

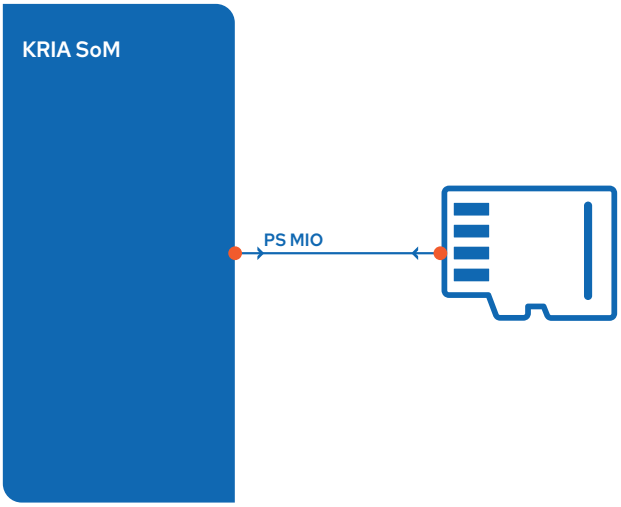


Figure 7: Block Diagram of the MicroSD Card

Table 8: Pinout of MicroSD Card

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
MIO51	J1-B37	L21	SD_CLK	SD Card Serial Clock
MIO50	J1-B36	M19	SD_CMD	SD Card Command/Response
MIO45	J1-D33	K20	SD_CD	Card Detect (Active Low)
MIO46	J1-D34	L20	SD_DAT0	SD Card Data 0
MIO47	J1-C34	H21	SD_DAT1	SD Card Data 1
MIO48	J1-C35	J21	SD_DAT2	SD Card Data 2
MIO49	J1-C36	M18	SD_DAT3	SD Card Data 3

2.2.9. UART to USB Interface

The carrier board features an UART to USB bridge interface to facilitate system monitoring. It is dedicated to the Processing System (PS) and serves as the system console for boot-level debugging and Linux terminal access. The pinout for the UART interface is shown below.

Table 9: Pinout of UART to USB Interface

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
MIO43	J1-A36	K19	PS_UART_TX	PS UART Transmit
MIO42	J1-A35	L18	PS_UART_RX	PS UART Receive

2.2.10. PMOD Expansion Interface

To allow for modular hardware expansion, the carrier board is equipped with independent PMOD (Peripheral Module) vertical connector (J14). This interface follows the standard 2x6 pin configuration, providing a total of 8 I/O pins, along with dedicated power and ground rails. The pinout for PMOD is shown below.

Table 10: Pinout of PMOD

PMOD Pin	SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
1	**HDC04**	J2-D57	AG14	PMOD_1	PMOD I/O 1
2	**HDC09**	J2-C58	AC13	PMOD_5	PMOD I/O 5
3	**HDC03**	J2-D56	AE14	PMOD_2	PMOD I/O 2
4	**HDC08_CC**	J2-C56	AC14	PMOD_6	PMOD I/O 6
5	**HDC02**	J2-D54	AE15	PMOD_3	PMOD I/O 3
6	**HDC07**	J2-C55	AH13	PMOD_7	PMOD I/O 7
7	**HDC01**	J2-D53	AD14	PMOD_4	PMOD I/O 4
8	**HDC06**	J2-C54	AG13	PMOD_8	PMOD I/O 8
9	—	—	—	GND	Ground
10	—	—	—	GND	Ground
11	—	—	—	PWR_3V3	3.3 V Supply Voltage
12	—	—	—	PWR_3V3	3.3 V Supply Voltage

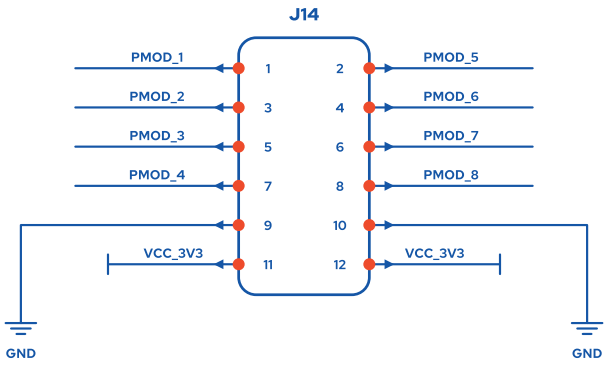


Figure 8: Connector Pinout of PMOD Interface (J14)

2.2.11. Health Monitoring

The carrier board incorporates an LTC2990IMS system monitor to provide real-time telemetry. This allows for the monitoring of critical voltage rails and the internal board temperature via the I²C bus, enhancing system reliability. By providing a reliable 14-bit ADC interface on the I²C bus, it allows developers to exercise I²C drivers, test software polling routines. While serving as a development tool, it also provides real-time telemetry for two voltage rails and internal board temperature. The I²C address of the LTC2990 is 0x4C. The pinout and the monitored parameters are shown below.

Table 11: Pinout of Health Monitoring

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
HDB03	J2-C59	AE13	PL_I²C_SENSOR_SCL	Health IC Serial Clock
HDB04	J2-C60	AF13	PL_I²C_SENSOR_SDA	Health IC Serial Data

Table 12: Monitored Parameters

LTC2990 Channel	Monitored Rail	Description
1	VCC_3V3	Power 3.3 V
2	VCC_1V8	Power 1.8 V
Internal	T_Internal	—

2.2.12. General Purpose I²C EEPROM

The carrier board includes an 8 Kbit (1024 bytes) non-volatile I²C EEPROM to provide persistent storage for critical system parameters. This memory is ideal for storing board-specific information such as serial numbers, hardware revision data, MAC addresses, and user-defined configuration settings. The EEPROM is connected to the same I²C bus as the platform management bus*, ensuring easy access from the Kria K26 Processing System (PS). The I²C address of the EEPROM is 0x51. The pinout for the EEPROM is shown below.

*For more information, the Kria K26 SoM Datasheet (DS987) shall be referred to.

Table 13: Pinout of EEPROM

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
MIO24_I²C_SCK	J1-C26	AB19	PS_I²C_SCK	PS I²C Clock Output
MIO25_I²C_SDA	J1-C27	AB21	PS_I²C_SDA	PS I²C Serial Data

2.2.13. System Watchdog Timer

To enhance system reliability and provide automatic recovery from software hangs or processor lockups, the carrier board features a dedicated hardware watchdog timer based on the TPS3430WDRCR. This high-accuracy programmable timer monitors a "heartbeat" signal from the Kria K26 SoM; if the signal is not received within a predefined window, the watchdog triggers a system-wide reset. The block diagram and signal mapping of the circuit are shown below.

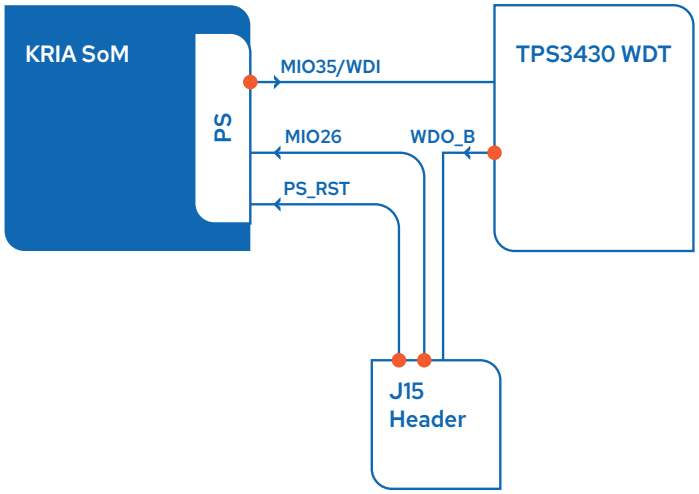


Figure 9: Block Diagram of WDT

Table 14: Pinout of Watchdog Timer

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
MIO35	J1-B28	H17	MIO35_WD_OUT	Watchdog Input (WDI) - Heartbeat from PS
MIO26	J1-D28	L15	MIO26	Watchdog Status / Monitor Pin
PS_SRST_C2M_L	J1-C16	N19	PS_SRST_C2M_L	System Soft Reset (Active Low)

2.2.14. Fan Control Interface

To maintain optimal operating temperatures for the Kria K26 SoM under heavy workloads, the carrier board includes a dedicated 12 V fan control circuit. This interface allows the Programmable Logic (PL) to dynamically manage cooling through a low-side switching architecture. The pinout for connector is shown below.

Table 15: Fan Control Signal

SoM Signal Name	SoM Pin Number	SoM Ball Number	Carrier Signal Name	Description
HPC02_P	J2-D36	AB8	HPC02_P	FAN PWM/Enable Control

2.2.15. Boot Modes

The carrier board provides a user-configurable boot mode interface to determine the primary boot source for the Kria K26 SoM. This is implemented via a 4-position DIP switch connected to the PS_MODE[0:3] pins of the Zynq UltraScale+ MPSoC. By adjusting the switch positions, developers can toggle between different boot targets such as SD Card, QSPI flash, or JTAG for debugging. The detailed switch mapping and boot mode settings* are shown in below.

Table 16: Boot Mode Settings

MODE	MODE0 (SW0701-1)	MODE1 (SW0701-2)	MODE2 (SW0701-3)	MODE3 (SW0701-4)
JTAG Mode	Low (0)	Low (0)	Low (0)	Low (0)
QSPI Mode	Low (0)	High (1)	Low (0)	Low (0)
SD0	High (1)	High (1)	Low (0)	Low (0)
SD1	High (1)	Low (0)	High (1)	Low (0)
eMMC	Low (0)	High (1)	High (1)	Low (0)

*For more information, the Zynq UltraScale+ Device Technical Reference Manual (UG1085) shall be referred to.

2.3. Electrical Specifications

The simple power diagram of the DE160203 module is given in Figure 10.

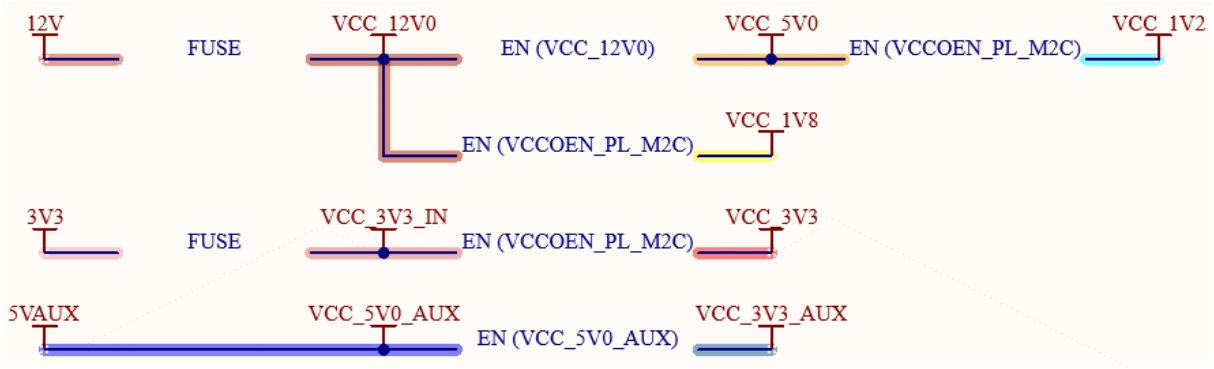


Figure 10: Power Diagram

The power supply requirements of the DE160203 module are given in below.

Table 17: Power Supply Requirements

Specification	Min	Typical	Max	Units
Power supply current of 12 V (XJ4)	–	–	4.5	A
Power supply current of 3.3 V (XJ4)	–	–	10	A
Power supply current of 5 VAUX (XJ4)	–	–	0.1	A

2.4. Physical Specifications

DE160203 is compatible with 2 slot 3U PXIe Peripheral Module.

2.5. Environmental Specifications

The environmental specifications of the module are given in below.

Table 18: Environmental Specifications

Parameter	Condition	Value
Operating Humidity	Relative, non-condensing	10% - 90%
Storage Humidity	Relative, non-condensing	5% - 95%
Operating Temperature	Forced-air cooling from chassis	0°C - +40°C
Storage Temperature	–	-40°C - +85°C

3. Safety Guidelines



The DE160203 shall not be operated in any manner not specified in this document. Misuse of the product may result in a hazard. Safety protection features may be compromised if the product is damaged. In the event of damage, the product shall be returned for repair.

4. Compatibility Guidelines

This product has been tested and found to comply with the applicable regulatory requirements and limits for electromagnetic compatibility (EMC). These requirements and limits are intended to provide reasonable protection against harmful interference when the product is operated within the specified electromagnetic environment.

This product is intended for use in industrial locations. However, harmful interference may occur in certain installations if the product is connected to peripheral devices or test objects, or if it is used in residential or commercial areas. To minimize interference with radio and television reception and to prevent unacceptable performance degradation, the product shall be installed and operated in strict accordance with the instructions specified in the product documentation.

Any changes or modifications to the product not expressly approved by DEICO may void the user's authority to operate the equipment under local regulatory rules.



To ensure the specified EMC performance, the product shall be operated only with shielded cables and accessories.



To ensure the specified EMC performance, the length of any cable attached to the front connectors shall not exceed 3 m (10 ft.).